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A Review on Embedded Systems Evaluation Based on Commercial Off-The-Shelf Devices

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ABSTRACT: The technology increasing turning towards reliable processors, which are low power, and customize these processors in terms in software and hardware to reach objectives of a low power system. Several platforms are available for embedded systems, such as microcontrollers, multiprocessors, field-programmable gate arrays, digital signal processors, and application-specific Integrated circuits etc. This paper evaluates the different low energy embedded systems in systematic way and Covers a key area of low power embedded hardware systems.

KEYWORDS: Embedded System, Energy Management and Hardware Platform.

I. INTRODUCTION

The number of functions that an average embedded mobile device executes is increasing rapidly, and the number of I/O devices that an embedded system should control increases accordingly. With rapid advances in HW and SW technologies, building a complicated mobile device isfeasible. However, one of the main challenges lies in how to manage power consumption, because mobile devices should operate with limited battery charge. From system designer's perspective, minimizing power consumption in mobile devices has become one of the most important issues. Thus, they sometimes sacrifice delay or area to reduce power consumption. With increasing demands for low power techniques, research topics on how to reduce power consumption broadly cover from the circuit/logic level to architecture, software, and system level techniques.

Among them, system-level power management techniques have been actively studied because, to reduce power consumption, management techniques are often more important than low power design techniques themselves. Specifically, two of the most commonly applied techniques are Dynamic Power Management (DPM) and Dynamic Voltage & Frequency Scaling (DVFS). To reduce power consumption of embedded processors, hardware-based DVFS techniques are widely accepted. DPM is a well-known technique that tries to shut down unused devices to reduce power consumption. To reduce power consumption of I/O devices, a Power Management Unit (PMU) with DPM capability is often employed. However, managing DVFS and DPM relies on system software such as operating systems. Software-based power-aware management has the merit of flexible control, but it has a potential problem of suffering from significant runtime overhead to decide how to manage effectively. Therefore, comprehensive power management techniques should take into account the overall hardware and software management overhead to achieve a true power reduction.

Paper is organized as follows. Section II gives the brief related work. Section III & IV relates to the Background and Methodology. Section V informs about the hardware working of the architecture proposed. Finally, Section V presents conclusion.

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II. RELATED WORK

Proposed system	Technology adopted	Remarks
Embedded Systems Based On Commercial Off-The-Shelf (Cots) Devices	• Proposed an easy-way to-implement COTS-based evaluation platform for low-energy embedded Systems. • To achieve energy saving, DVFS is provided for the whole microcontroller (including core,phase-locked loop, memory, and I/O). • The platform is equipped with accurate energy/power measurement units, debugging ports, and facilities for evaluating fault-tolerance techniques.	• Applying DVFS on the whole microcontroller provides up to 47% and 12% energy. • Approach is general and can be applied to other types of systems. • very suitable for evaluating Embedded systems with low energy consumption and fault tolerance requirements. reducing power/energy consumption compared with other power-down policies
OLYMPIC: OPTICAL PHOTONIC NETWORK FOR LOW-POWER CHIP MULTIPROCESSORS	• Proposes Olympic, an all-optical NoC architecture using a hierarchical topology made up of replicated and cascaded simple photonic building blocks (rings). • Local rings connect tiles within clusters directly and a global ring glues together local ones and enables inter-cluster communications.	• Significant energy reduction in embedded, tiled CMPs higher parallelism communications can be possible even if the required conversions in the hubs induce latency and energy overheads. • achieve energy reduction up to 65% over a fully connected 2D electrical mesh
Rapid Prototype Platform For Arm Based Embedded System	• Proposed a design of a fast prototyping platform for ARM based embedded systems, providing a low-cost solution to meet the request of Flexibility and testability in embedded system prototype development.	• Discuss the design of a fast prototyping platform for ARM based embedded systems to accommodate the requirements of flexibility and testability in the prototyping phase of an embedded system development. • Proposed idea is general and can be applied to embedded system of other types.

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III. BACKGROUND

In the current embedded technology world there is an active need for low-power designs and power-aware system management. Hardware prototype is an important in the embedded system design with any hardware platforms. The overview of embedded systems and its different ways to design and achieve low energy based embedded systems are described in this paper.

A. DESCRIPTION OF EMBEDDED SYSTEM PLATFORMS

The embedded systems are normally defined as the software realized in hardware in order to realize specified real-time functionalities. They normally used soft-core processing hardware includes controllers, processors, FPGAs, digital signal processors (DSPs), and application-specific integrated circuits (ASICs), each of which has its own properties.

B. ROCONTROLLERS AND MICROPROCESSORS

The programmable functionalities of different microcontrollers and microprocessors are the most important reason for their employment in most of the hard and soft real time embedded systems. The hardware platform of microprocessor are generally low cost but since memory and I/O has to be connected externally, the circuit becomes large. On the other hand for microcontrollers memory and I/O are present internally. Microprocessor needs external components, thus entire power consumption is high. Hence it is not suitable to use with devices running on stored power like batteries. On the contrary microcontroller's devices can runs on stored power like batteries. Microcontrollers (MCUs) are designed with memory blocks and some digital and analog peripherals integrated with a processor core on one chip. Microcontrollers may operate using 32- or even 64-bit words, be clocked at a hundred Mega Hertz range and have required computational power to realize functionality of a DSP. In almost every case, however, internal ROM and minimal amount of Random Access Memory (RAM), some timers, digital input–output circuitry are integrated into the chip.

C. FIELD-PROGRAMMABLE GATE ARRAYS (FPGAS)

A field-programmable gate array (FPGA) is an integrated circuit (IC) that can be programmed in the field after manufacture. FPGAs works on almost same principles, but have vastly wider potential application than, programmable read-only memory (PROM) chips. Figure bellows shows the system architecture for FPGA

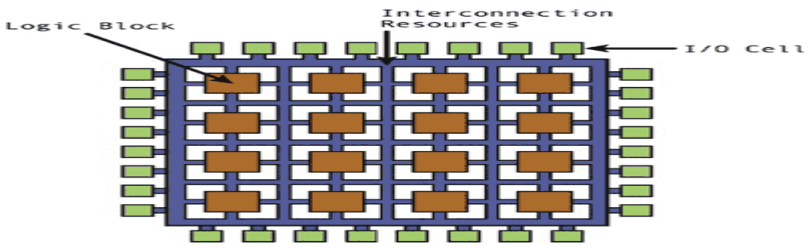

Fig.1. System Architecture of Field-Programmable Gate Arrays (FPGAS)

IV. METHODOLOGY

I. LOW-ENERGY MULTIPROCESSOR EMBEDDED SYSTEMS

A. EMBEDDED SYSTEMS BASED ON COMMERCIAL OFF-THE-SHELF (COTS) DEVICES

The hardware platform with energy management techniques such as dynamic power management and fault-tolerance techniques are proposed based on cots devices. The ARM AT91SAM7x256 microcontrollers based embedded system by using cots devices as shown in figure 2. ARM7TDMI is the most widely used COTS processor in

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contemporary embedded systems because it is a low-cost, high performance, and versatile processor. To manage the energy consumption, DVFS [11] and DPM [12] have been effectively used.

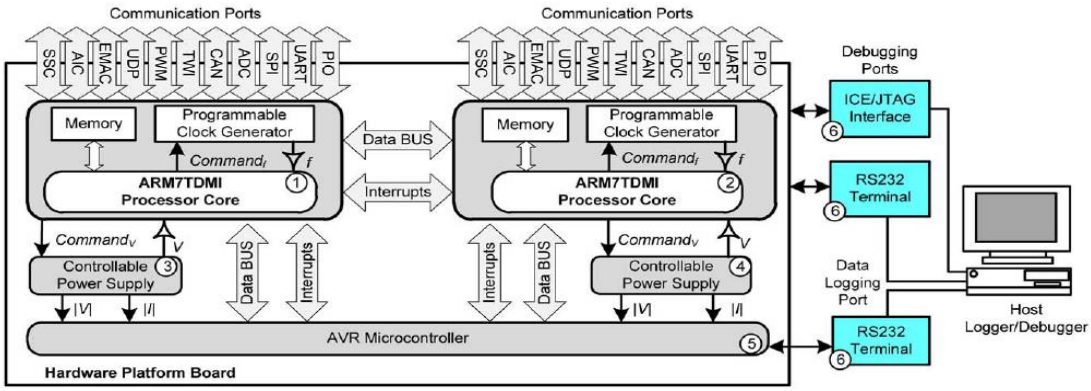

Fig. 2(a). Block diagram Hardware platform.

B. OLYMPIC: OPTICAL PHOTONIC NETWORK FOR LOW-POWER CHIP MULTIPROCESSORS

OLYMPIC is based on hierarchical topologies of replicated and cascaded simple photonic building blocks (rings). Olympic is a tiled architecture in which every tile has privateL1 caches and a slice of shared L2 cache and directory. It employs a hierarchical clustered network topology in which clusters are interconnected through a global photonic ring and tiles inside each cluster are connected through a local photonic ring. Figure 1 shows the Olympic architecture for 16 tiles and four clusters, each with four tiles.

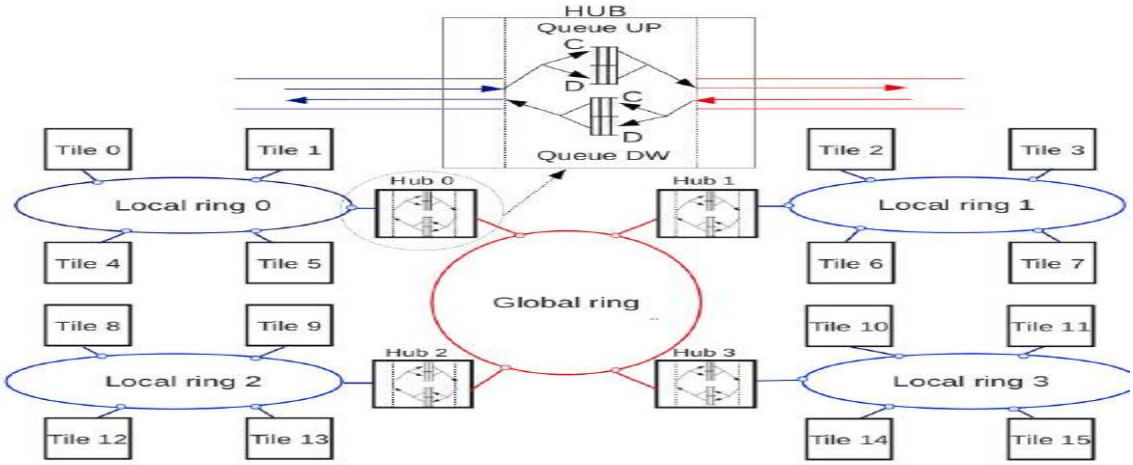

Fig. 2(b). Basic Olympic topology

The OLYMIC techniques in which one tile wishing to communicate to another in a different cluster needs to send the messages to its local hub, which receives and converts it into electronics and then sends it again in optics, through the global ring to the hub ofthe cluster containing the destination tile. The destination hubconverts the message again (O/E/O) and sends it to the final tile through its local ring.In Olympic, wavelengths in each ring (local or global) are used in mutual exclusion through a token-ring arbitration that is tightly integrated with the transmission scheme.
Once a message successfully arrives to the destination hub, it is storedinto the queue DW buffer waiting to be transmitted over the final local ring to the destination tiles. The separate separated buffers for control and data messages have been adopted in this scheme.An inter-cluster transmission can initiate as soon as the local ring serving thesource tile is free, even if the destinationlocal ring are busy.

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V. HARDWARE PROTOTYPE

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A. RAPID PROTOTYPE PLATFORM FOR ARM BASED EMBEDDED SYSTEM

A fast prototyping platform for ARM based embedded systems, providing a reliable and minimum-cost solution to achieve the request of flexibility and testability in embedded system prototype development. It also encourages concurrent development of different parts of system hardware as well as module reusing.To enable rapid prototyping, the platform should be capable of quickly assembling parts of the system into a whole through flexible interconnection. The design the Rapid Prototyping Platform is shown in Fig. 3.

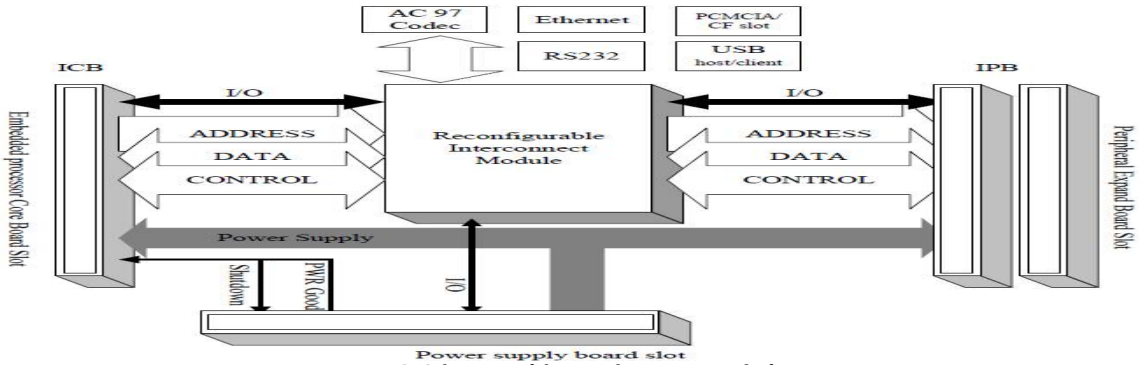

Fig.3. Schematic of the Rapid Prototyping Platform

The interface ICB between the platform and the embedded processor core board and interface IPB between the platform and peripheral boards enable to develop different parts of the target embedded system concurrently and to compose them into a prototype rapidly, and encourage module re using as well. The two interfaces are connected by a reconfigurable interconnect module. There are also some commonly used peripheral modules, e.g. RS232 transceiver module, bus extended Ethernet module, AC97 codec, PCMCIA/CompactFlash Card slot, and etc, on the platform which can be interfaced through the reconfigurable interconnect module to expedite the embedded system development.

B. DYNAMIC POWER MANAGEMENT TECHNIQUE

A novel power management technique based on a parallel programming model for multicore systems by turning off unnecessary cores, we can reduce power consumption.

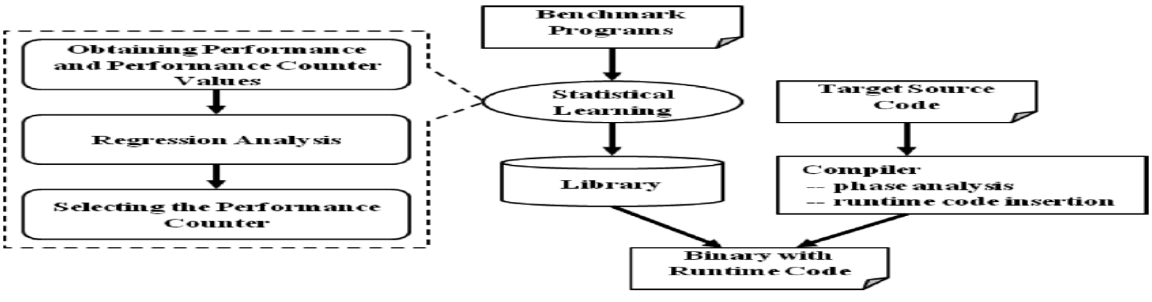

Fig.4. DVFS method based on statistical analysis

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The proposed power management technique is called MPMP. In a typical parallel programming paradigm like OpenMP, parallel library routines are invoked when preprocessing parallel processing directives. By identifying the type of library routine calls, we can tell which portion of the code is crucial for power management. Among open source OpenMP-compliant compilers, OMPi [19] was chosen to implement the proposed power management capability. OMPi was modified with changes in the OpenMP library with a set of power management library (PML) routines. For example, when the "#pragma omp parallel" directivein OpenMP is found, the start of a parallel region is marked, andthe appropriate number of active cores is determined. When we find the end of a parallel region followed by a serial region, the number of active cores is set to one (or some minimum value).The effectiveness of the proposed power management policy is based on a parallel programming model.

VI. CONCLUSION

A systematic survey on low energy embedded systems taken and methods are studied in details and presented a suitable remarks for developing low energy embedded systems based on multiprocessor and multicores. Embedded Systems Based On Commercial Off-The-Shelf (Cots) Devices very suitable for evaluating embedded systems with low energy consumption and fault tolerance requirements reducing power/energy consumption compared with other power-down policies. Also Applying DVFS on the whole microcontroller provides up to 47% and 12% energy. Olympic: Optical Photonic Network For Low-Power Chip Multiprocessors provides significant energy reduction in embedded, tiled CMPs higher parallelism communications can be possible even if the required conversions in the hubs induce latency and energy overheads. Rapid Prototype Platform For Arm Based Embedded System is fast prototyping platform for ARM based embedded systems, providing a low-cost solution to meet the request of Flexibility and testability in embedded system prototype development. At the last Dynamic Power Management TECHNIQUE is also reviewed based on a parallel programming model. Based on this literatures design, analysis, and implementation of low energy embedded systems with multiprocessor techniques is the work in progress.

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