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Design of DADDA Multiplier with CSC and Low Power Scan Based Test Using DFT

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ABSTRACT*:* A new low-power (LP) scan-based built-in self-test (BIST) technique is proposed based on weighted pseudo-random test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. Precise models and algorithms are not always suitable for efficient for use in the applications. Multiplication using DADDA multipliers has higher speed compared to conventional multipliers are also using approximate prediction technique for carry. They are quite effective for carry. This effective in terms of power dissipation, when high speed is required. In both the cases, only a small number of scan chains are activated in a single cycle. Sufficient experimental results are presented to demonstrate the performance of the proposed LP BIST approach.

KEYWORDS*:* Low-power (LP) built-in self-test (BIST), reseeding, scan-based BIST, DADDA Multiplier. Speculative Compressor.

I. INTRODUCTION

The power and ever-increasing test power. Problems, such as excessive heat that may reduce circuit reliability, formation of hot spots, difficulty in performance verification, reduction of the product yield and lifetime, and so on, have become severe [15] [16]. More details on how to provide more accurate power model can be found from [15] and [16]. fast simulation approach was proposed for low-power (LP) off-chip interconnect design in[8]. An important through silicon via (TSV) modeling/simulation technique for LP 3-D stacked IC design was presented in [62]. Furthermore, the power dissipation of scan-based built-in self-test (BIST) is much higher than power dissipation in patterns. Therefore, it is essential to propose an effective LP BIST approach.

Recent methods in aim at reducing the switching activity during scan shift cycles, whose test generator allows automatic selection of their parameters for LP pseudorandom test generation. However, many of the previous LP BIST approaches cause fault coverage loss to some extent. Therefore, achieving high fault coverage in an LP BIST scheme is also very important. deterministic scan testing due to excessive switching activities caused by random.
In this paper, we propose a new LP scan-based BIST architecture, which supports LP pseudorandom testing, LP deterministic BIST and LP reseeding. We present the major contributions of this paper in the following.

1) A new LP weighted pseudorandom test pattern generator using weighted test-enable signals is proposed using a new clock disabling scheme. The design-for-testability (DFT) architecture to implement the LP BIST scheme is presented. Our method generates a series of degraded sub circuits. The new LP BIST scheme selects weights for the test-enable signals of all scan chains in each of the degraded sub circuits, which are activated to maximize the testability.

2) A new LP deterministic BIST scheme is proposed to encode the deterministic test patterns for random-pattern-resistant faults. Only a part of flip flops are activated in each cycle of the whole process of deterministic BIST. A new procedure is proposed to select a primitive polynomial and the number of extra variables injected into the linear-feedback shift register (LFSR) that encode all deterministic patterns. The new LP reseeding scheme.

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3) Testing all the memories in these SoCs serially would take a long time. Therefore, a memory BIST design that allows two or more memories to be tested simultaneously is needed. So in case when the memories are tested in parallel (concurrently) the consumed power is the sum of the powers consumed by each memory. Hence, parallel run of memories by the same BIST scheme will consume much power.

which means that there could be a limitation on sharing multiple memories by the same BIST scheme. Total test application time of a memory BIST is also calculated under maximum power constraint [2]. Consequently, power consumption is one of the most critical constraints for SoCs. Moreover, the increasing functionality also raises complexity for specification, design and verification of SoCs. Therefore, power aware design should be introduced at early stages of SoC design where it has the highest benefits for power reduction [3].

II. RELATED WORK

Scan flip flops, especially, the ones close to the scan-in pins, are not observable in most of shift cycles. Proposed a novel BIST scheme that inserts multiple capture cycles after scan shift cycles during a test cycle. Thus, the fault coverage of the scan-based BIST can be greatly improved. An improved method of the earlier work, presented in, selects different numbers of capture cycles after the shift cycles. In this paper, a new LP scan-based BIST technique is proposed based on weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST.

Weighted pseudorandom testing schemes can effectively improve fault coverage. A weighted test-enable signal-based pseudorandom test pat-tern generation scheme was proposed for scan-based BIST, according to which the number of shift cycles and the number of capture cycles in a single test cycle are not fixed. A reconfigurable scan architecture was used for the deterministic BIST scheme in using the weighted test-enable signal-based pseudorandom test generation scheme. A low-transition test pattern generator was proposed to reduce the average and peak power of a circuit during test by reducing the transitions among patterns. Transitions are reduced in two dimensions:

1) Between consecutive patterns.
2) Between consecutive bits.

LP BIST technology that reduces shift power by eliminating the specified high-frequency parts of vectors and also reduces capture power. The approach to reduce peak power and power droop during capture cycles in scan-based logic BIST. An efficient BIST architecture was recently presented for targeting defects in dies and in the interposer interconnects. low-power BIST technology was proposed that reduces shift power by eliminating the specified high-frequency parts of vectors and also reduces capture power. Multi cycle tests support test compaction by allowing each test to detect more target faults. The ability of multi cycle broadside tests to provide test compaction depends on the ability of primary input sequences to take the circuit between pairs of states that are useful for detecting target faults. This ability can be enhanced by adding DFT logic that allows states to be complemented. Complete fault coverage can be obtained when the pseudorandom test generator is modified. A combination of a pseudorandom test generator and a combinational map-ping logic was constructed produce a given target pattern set of the hard-to-detect faults. which encoded deterministic vectors into seeds.

Memory BIST grouping methodology taking into account power domains (based on UPF): In real world it is essential to save power in parts of chip that are not in use. Chips integrate several systems on a single chip (SoC). In order to save current consumption, each Intellectual Property (IP) can move between power modes (power-off, power-on, etc.). Each SoC is divided into power domains and those power domains can be turned on and off as well, according to the power-mode. The isolation cells keep the turned off IP outputs in a previously defined value, and this is how the shut-down IP does not corrupt other active IP functionality.

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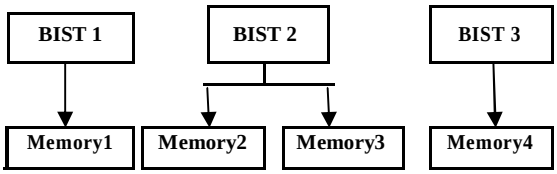

Figure 1. Memory BIST architecture.

III. CIRCUIT DESIGN

In Fig. 2, the proposed BIST circuit is depicted. It consists of a nMOS transistor pair DUT1,n and a pMOS pair DUT1,p, respectively. The gates of the two transistors of a selected pair are operated with complementary clock signals, the gates of the non-selected pair are deactivated. The pairs are operated as current sinks [10], so that in case of the pMOS pair the S/D terminals represent the input of the sink, whereas in case of the nMOS pair the well takes over this role. All other terminals are connected to voltage *Vmid*, which is typically in the range of *VDD* /2. The current sink's input is held at the same voltage through the regulation loop consisting of OP1 and M1. The charge pumping current is integrated on capacitor *Cint* (100 pF) which is pre-charged to 0 V at the beginning of a measurement cycle. The master clock used to generate the gate voltages of the DUTs also drives a counter which is stopped by comparator COMP1 once a voltage (*VDD-Vref*) is integrated on *Cint*. For each clock cycle, the selected DUT draws a charge packet *Dit* × *Wtotal* × *L* × *q* from *Cint*, so that the counter stop condition is fulfilled for

$$N - 1 < Cint\,(VDD - Vref) / (Dit \times Wtotal \times L \times q)\,\mathrm{d}\,N \quad (2)$$

with *N* being the number of counted pulses. An SPI interface is used to continuously stream out the measured value *N*. Moreover, it controls the DUT operating conditions using a small state machine. The interface can communicate thousands of A/D measurement values from the BIST structure during a few milliseconds to an external control unit e.g. during a ramp-up period of an ASIC or a SoC for a given application.

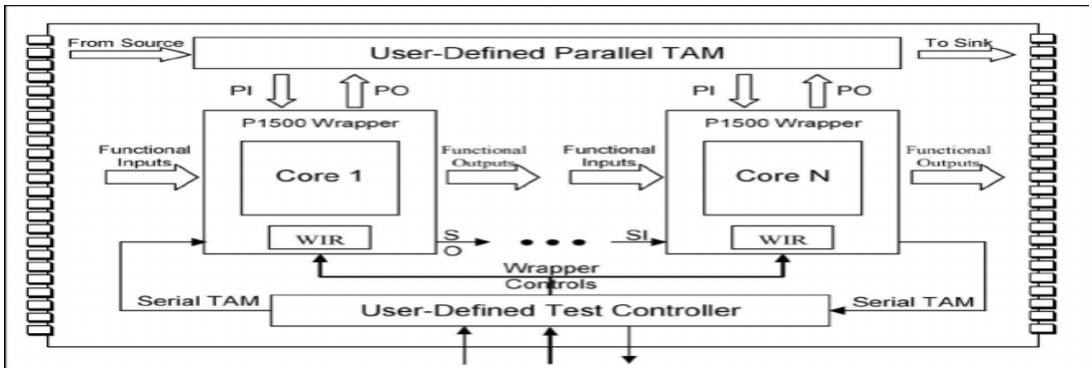

Figure 2.Circuit diagram of the core BIST structure.

The CUT are directly connected to a signature analyzer. In this scheme a test vector is applied to the CUT, and a response is captured from the CUT on each clock cycle. The second scheme is test-per -scan, in which a scan path is used to shift test patterns into a CUT. A full scan cycle requires m+1 clock cycles, where m is the number of flip-flops in the scan-chain. The response to an applied test pattern is captured into a scan-chain and scanned out in the next scan cycle in parallel with scanning in another test pattern. In these test schemes, which is widely adopted in the design of combinational circuits (test-per-clock) and the sequential circuits (test-per-scan), most of the CUT nodes undergo switching whilst applying test patterns. Hence, a substantial amount of the power dissipation occurs during this operation because of the uncorrelated patterns produced by the LFSR.

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IV. THE PROPOSED DESIGN

Design for testing or design for testability (DFT) consists of IC Design techniques that add testability features to a hardware product design. The added features make it easier to develop and apply manufacturing tests to the designed hardware. The purpose of manufacturing tests is to validate that the product hardware contains no manufacturing defects that could adversely affect the product's correct functioning. Tests are applied at several steps in the hardware manufacturing flow and, for certain products, may also be used for hardware maintenance in the customer's environment. The common understanding of DFT in the context of Electronic Design Automation (EDA) for modern microelectronics is shaped to a large extent by the capabilities of commercial DFT software tools as well as by the expertise and experience of a professional community of DFT engineers researching, developing, and using such tools. Much of the related body of DFT knowledge focuses on digital circuits while DFT for analog/mixed-signal circuits takes somewhat of a backseat.

To simplify test generation, DFT addresses the accessibility problem by removing the need for complicated state transition sequences when trying to control and/or observe what's happening at some internal circuit element. Depending on the DFT choices made during circuit design/implementation, the generation of Structural tests for complex logic circuits can be more or less automated. Approximate circuits have been considered for error-tolerant applications that can tolerate some loss of accuracy with improved performance and energy efficiency. Multipliers are key arithmetic circuits in many such applications such as digital signal processing (DSP). In this paper, a novel approximate multiplier with a lower power consumption and a shorter critical path than traditional multipliers is proposed for high-performance DSP applications.

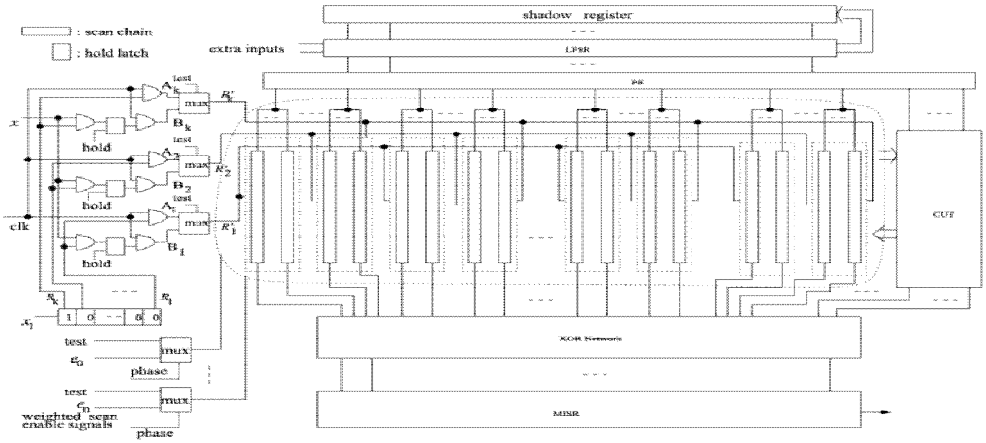

Figure 3.General DFT architecture for LP scan-based BIST.

This multiplier leverages a newly-designed approximate adder that limits its carry propagation to the nearest neighbors for fast partial product accumulation. Different levels of accuracy can be achieved through a configurable error recovery by using different numbers of most significant bits (MSBs) for error reduction. The approximate multiplier has a low mean error distance, i.e., most of the errors are not significant in magnitude. Compared to the Wallace multiplier, a 16-bit approximate multiplier implemented in a 28nm CMOS process shows a reduction in delay and power of 20% and up to 69%, respectively. It is shown that by utilizing an appropriate Error recovery, the proposed approximate multiplier achieves similar processing accuracy as traditional exact multipliers but with significant improvements in power and performance.

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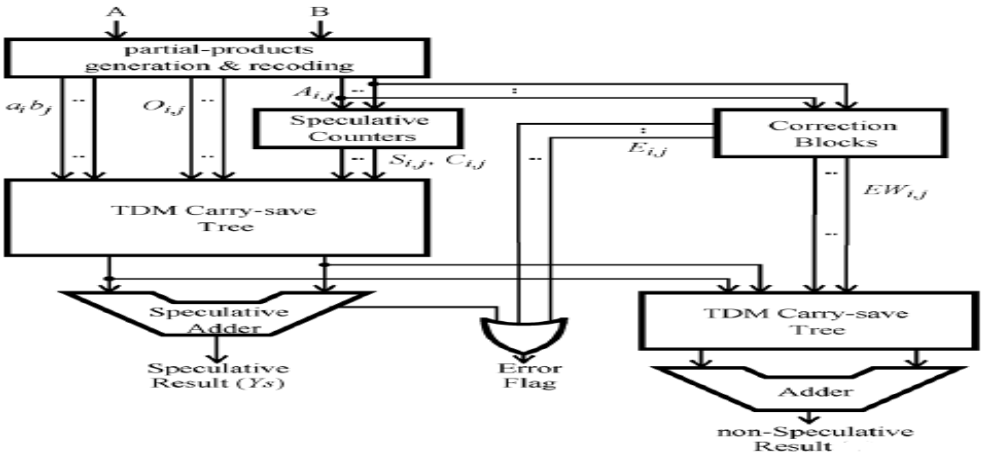

Figure 4. architecture of approximate multiplier.

V.RESULTS

Given the complete approach presented above, one can easily observe that the number of test clusters depends linearly on a deterministic pattern count targeting random-resistant faults. Moreover, the children pattern count for each test cluster initially matches the size of the longest scan chain (or the number of scan shift cycles). Needless to say, a random pattern resistant fault list may easily contain millions of faults. The implications of these facts become apparent as we begin to consider relevant memory and CPU time requirements. Clearly, with the increasing size of designs, the presented flow may turn out to be less practical as the memory footprint and time needed to complete the ordering process can be prohibitive for large circuits. Consequently, to alleviate these problems, we propose below a more pragmatic and scalable solution.

	Gates	Scan cells	Scan architecture	EDT size	Input injectors	Test coverage
D1	220K	13K	122 x 138	17	1	98.87%
D2	450K	45K	226 x 200	32	4	98.67%
D3	1.5M	145K	700 x 207	42	8	97.81%
D4	1.2M	85K	427 x 200	32	4	92.30%
D5	600K	20K	35 x 686	32	1	91.22%
D6	840K	34K	84 x 416	32	1	92.30%

Table 1 Circuit characteristics.

The multiplier have been simulated using Model sim 6.2c and synthesized using ISE design suite 14.5 and are shown in fig.no.3,4 and figure.no.5.

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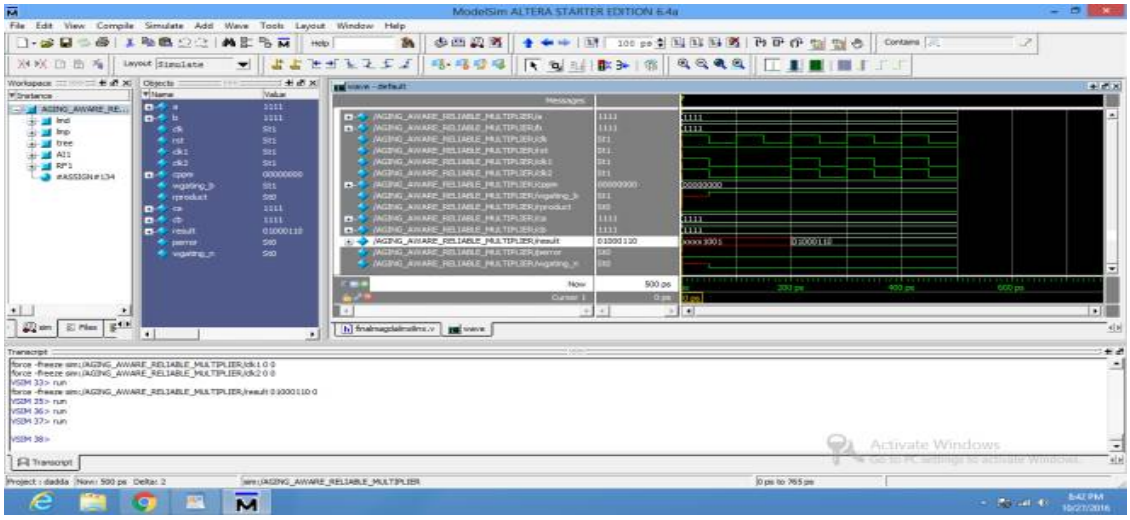

Figure 5. Simulation Results.

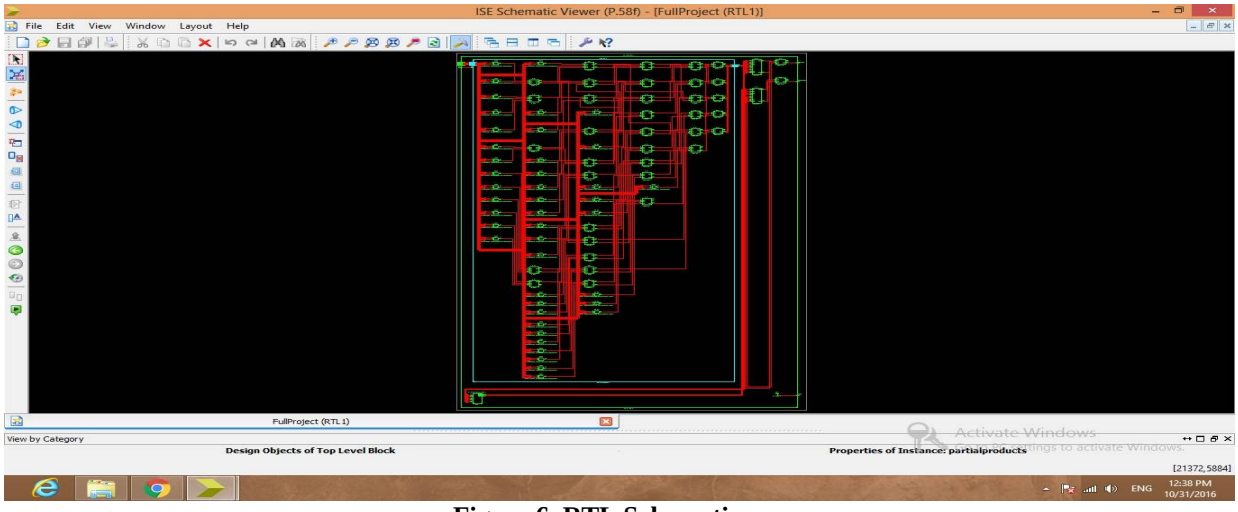

Figure 6. RTL Schematic.

In [10] we have presented a fast power consumption estimation methodology for BIST architecture of embedded memories. Power consumption depends on functional and scalability parameters of memory BIST[10]. Power consumption consists of two main components static power and dynamic power. The impact of changes due to static power is small hence we explore only the impact of changes by dynamic power. As expected, significantly lower count rates are achieved in this configuration. A normalized standard deviation (3V value) of 1.26% is achieved now.

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Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	79	29,504	1%	
Number of occupied Slices	42	14,752	1%	
Number of Slices containing only related logic	42	42	100%	
Number of Slices containing unrelated logic	0	42	0%	
Total Number of 4 input LUTs	79	29,504	1%	
Number of bonded IOBs	19	250	7%	
Average Fanout of Non-Clock Nets	2.85			

Figure 7. Tabulated parameter for area.

Xilinx XPower Analyzer - FullProject.ncd - [Table View]

Device	
Family	Spartan3e
Part	xc3s1600e
Package	fg320
Temp Grade	Commercial
Process	Typical
Speed Grade	-4
Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0
Characterization	
PRODUCTION	v1.2.06-23-09

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	79	29504	0
Signals	0.000	94	---	---
IOs	0.000	19	250	8
Leakage	0.203			
Total	0.203			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	21.1	80.7	29.3

Supply Summary				
Source	Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.200	0.069	0.000	0.069
Vccaux	2.500	0.045	0.000	0.045
Vcco25	2.500	0.003	0.000	0.003

Supply Power (W)	Total	Dynamic	Quiescent
	0.203	0.000	0.203

Figure 8. Tabulated parameter for power.

```
================================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 658 / 1
--------------------------------------------------------------------------------
Delay:               15.177ns (Levels of Logic = 10)
  Source:            a<6> (PAD)
  Destination:       speculativeresult (PAD)

  Data Path: a<6> to speculativeresult
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             10   1.218   1.057  a_6_IBUF (a_6_IBUF)
     LUT2:I0->O             2   0.704   0.622  partialproducts/p<6>_3_and00001 (partialproducts/p<6><3>)
     LUT4:I0->O             2   0.704   0.526  partialproducts/fa_91/Mxor_sum_xo<0>1 (partialproducts/s<35>)
     LUT4:I1->O             2   0.704   0.526  partialproducts/fa_92/Mxor_sum_xo<0>1 (partialproducts/s<36>)
     LUT3:I1->O             2   0.704   0.526  partialproducts/fa_94/Mxor_sum_xo<0>1 (partialproducts/s<38>)
     LUT3:I1->O             1   0.704   0.455  partialproducts/fa_95/carry1 (partialproducts/c<39>)
     LUT4:I2->O             1   0.704   0.499  partialproducts/ha_105/Mxor_sum_Result1 (ab<10>)
     LUT2:I1->O             1   0.704   0.424  ha_172/Mxor_sum_Result_SW0 (N14)
     LUT4:I3->O             1   0.704   0.420  ha_172/Mxor_sum_Result (speculativeresult_OBUF)
     OBUF:I->O                  3.272          speculativeresult_OBUF (speculativeresult)
    ----------------------------------------
    Total                      15.177ns (10.122ns logic, 5.055ns route)
                                        (66.7% logic, 33.3% route)

================================================================================
```

Figure 9. Tabulated parameter of delay.

VI.CONCLUSION

Approximate computing is an important factor for multimedia designs. These designs depend on different features of compression. The proposed method has the advantage of decreasing the number of transistors, delay, and low power consumption as compared to the existing designs. A speculative adder is used in the final carry propagate addition. The multiplier design is further optimized to have small. The designs functionality have been verified using

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Xilinx ISE design suite 14.5. The performance of the approximate multiplier can further be improved by considering don't care conditions and further by using variable latency adder.

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