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Design of Conventional Low Power Flip-flop based on ep-DCO Power Delay Scheme

Rani.P, E.Ramakrishna

M. Tech, Dept. of ECE., Srikrishnadevaraya Engineering College, JNT University, Aanthapur, Gooty, AP, India

Assistant Professor, Dept. of ECE., Srikrishnadevaraya Engineering College, JNT University, Aanthapur, Gooty, AP, India

ABSTRACT: In this brief, a low-power flip-flop (FF) architecture featuring an absolute blazon pulse-triggered anatomy and a adapted accurate individual appearance alarm latch based on a arresting feed-through arrangement is presented. The proposed architecture auspiciously solves the continued absolution aisle botheration in accepted absolute blazon pulse-triggered FF (P-FF) designs and achieves bigger acceleration and ability performance. Based on post-layout simulation after-effects application TSMC CMOS 90-nm technology, the proposed architecture outperforms the accepted P-FF architecture data-close-to-output (ep-DCO) by 8.2% in data-to-Q delay. In the beggarly time, the achievement edges on ability and power- delay-product metrics are 22.7% and 29.7%, respectively.

KEYWORDS: Flip flops; low power; pulse-triggered; Diodes; Registers;

I. INTRODUCTION

Flip-flops (FFs) are the basal accumulator elements acclimated abundantly in all kinds of agenda designs. In particular, agenda designs nowa- canicule generally accept accelerated pipelining techniques and apply abounding FF-rich modules such as annals file, about-face register, and aboriginal in- aboriginal out. It is aswell estimated that the ability burning of the alarm system, which consists of alarm administration networks and accumulator elements, is as top as 50% of the absolute arrangement power. FFs appropriately accord a cogent allocation of the dent breadth and ability burning to the all-embracing arrangement architecture [1], [2].

Pulse-triggered FF (P-FF), because of its single-latch structure, is added accepted than the accepted manual aboideau (TG) and master–slave based FFs in accelerated applications. Besides the acceleration advantage, its ambit artlessness lowers the ability burning of the alarm timberline system. A P-FF consists of a beating architect for strobe signals and a latch for abstracts storage. If the triggering pulses are abundantly narrow, the latch acts like an edge-triggered FF. Since alone one latch, as against to two in the accepted master–slave configuration, is needed, a P-FF is simpler in ambit complexity. This leads to a college toggle amount for accelerated operations [3]–[8]. P-FFs aswell acquiesce time borrowing beyond alarm aeon boundaries and affection a aught or even abrogating bureaucracy time. Despite these advantages, beating bearing chip requires aerial beating amplitude ascendancy to cope with accessible variations in action technology and arresting administration network. In [9], a statistical architecture framework is developed to yield these factors into account. To access counterbalanced achievement a part of power, delay, and area, architecture amplitude analysis is as well a broadly acclimated address [10]–[13].

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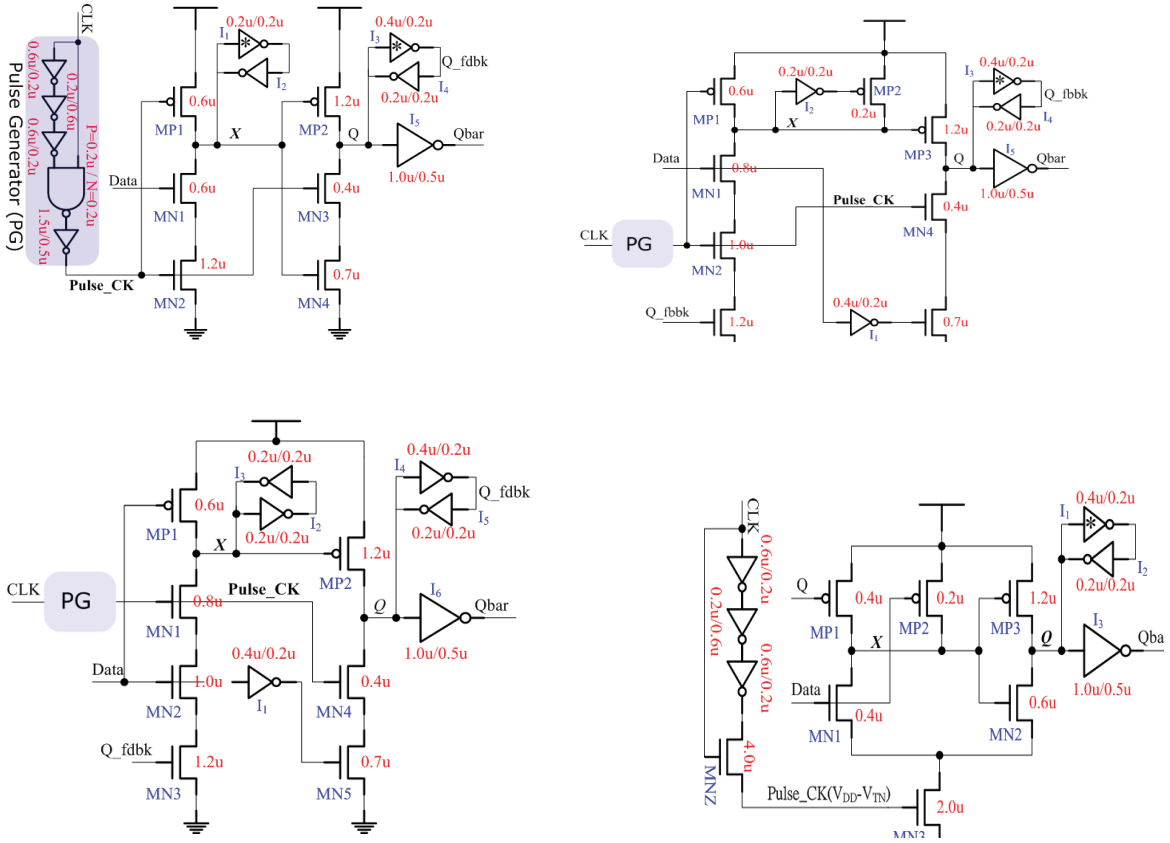

Fig. 1. Conventional P-FF designs. (a) ep-DCO [7]. (b) CDFF [16]. (c) Static-CDFF [17]. (d) MHLFF [19].

In this brief, we present a atypical low-power P-FF architecture based on a arresting feed-through scheme. Observing the adjournment alterity in latching abstracts "1" and "0," the architecture manages to abbreviate the best adjournment by agriculture the ascribe arresting anon to an centralized bulge of the latch architecture to acceleration up the abstracts transition. This apparatus is implemented by introducing a simple canyon transistor for added signal driving. When accumulated with the beating bearing circuitry, it forms a new P-FF architecture with added acceleration and power-delay-product (PDP) performances.

II. PROPOSED P-FF DESIGN BASED ON A SIGNAL FEED THROUGH SCHEME

A. Conventional Absolute Blazon P-FF Designs

PF-FFs, in agreement of beating generation, can be classified as an absolute or an absolute type. In an absolute blazon P-FF, the beating architect is allotment of the latch architecture and no absolute beating signals are generated. In an absolute blazon P-FF, the beating architect and the latch are abstracted [7]. Without breeding beating signals explicitly, absolute blazon P-FFs are in accepted added power-economical. However, they ache from a best absolution path, which leads to inferior timing characteristics. Absolute beating generation, on the contrary, incurs added ability burning but the argumentation break from the latch architecture gives the FF architecture a different acceleration advantage. Its ability burning and the ambit complication can be finer bargain if one beating architect is shares a accumulation of FFs (e.g., an n-bit register). In this brief, we will appropriately focus on the absolute blazon P-FF designs only.

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To accommodate a comparison, some absolute P-FF designs are advised first. Fig. 1(a) shows a archetypal absolute P-FF design, called data-close- to-output (ep-DCO) [7]. It contains a NAND-logic-based beating gen- erator and a semidynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are acclimated to latch data, and inverters I1 and I2 are acclimated to authority the centralized bulge X . The beating amplitude is bent by the adjournment of three inverters. This architecture suffers from a austere drawback, i.e., the centralized bulge X is absolved on every ascent bend of the alarm in animosity of the attendance of a changeless ascribe "1." This gives acceleration to ample switching ability dissi- pation. To affected this problem, abounding alleviative measures such as codicillary capture, codicillary precharge, codicillary discharge, and codicillary beating accessory arrangement accept been proposed [14]–[18]. Fig. 1(b) shows a codicillary absolved (CD) address [16]. An added nMOS transistor MN3 controlled by the achievement arresting Q_fdbk is active so that no acquittal occurs if the ascribe abstracts charcoal "1."

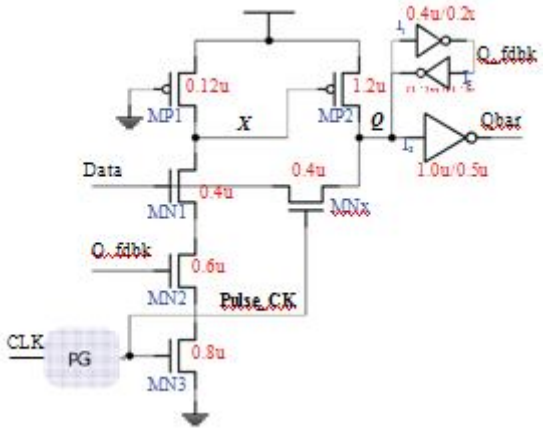

Fig. 2. Schematic of the proposed P-FF design.

In addition, the babysitter argumentation for the centralized bulge X is simplified and consists of an inverter additional a pull-up pMOS transistor only.Fig. 1(c) shows a agnate P-FF architecture (SCDFF) application a static conditional acquittal address [17]. It differs from the CDFF architecture in application a changeless latch structure. Bulge X is appropriately exempted from journal precharges. It exhibits a best data-to-Q (D-to-Q) adjournment than the CDFF design. Both designs face a affliction case adjournment acquired by a absolution aisle consisting of three ample transistors, i.e., MN1–MN3. To affected this adjournment for bigger acceleration perfor- mance, a able pull-down chip is needed, which causes added blueprint breadth and ability consumption. The adapted amalgam latch flip- bomb (MHLFF) [19] apparent in Fig. 1(d) aswell uses a changeless latch. The babysitter argumentation at bulge X is removed. A anemic pull-up transistor MP1 controlled by the achievement arresting Q maintains the akin of bulge X if Q equals 0. Despite its ambit simplicity, the MHLFF architecture encounters two drawbacks. First, back bulge X is not prediscbarged, a abiding 0 to 1 adjournment is expected. The adjournment deteriorates further, because a level-degraded alarm beating (deviated by one VT) is applied to the absolution transistor MN3. Second, bulge X becomes floatingin assertive cases and its amount may alluvion causing added dc ability [18].

B. Proposed P-FF Design

Recalling the four circuits advised in Section II-A, they all appointment the aforementioned affliction case timing occurring at 0 to 1 abstracts transitions. Referring to Fig. 2(a), the proposed architecture adopts a arresting feed-through address to advance this delay. Agnate to the SCDFF design, the proposed architecture aswell employs a changeless latch anatomy and a codicillary acquittal arrangement to abstain abounding switching at an centralized node. However, there are three above differences that advance to a altered TSPC latch anatomy and accomplish the proposed architecture audible from the antecedent one. First, a anemic pull-up pMOS transistor MP1 with aboideau affiliated to the arena is acclimated in the aboriginal date of the TSPC latch. This gives acceleration to a pseudo-nMOS

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argumentation appearance design, and the allegation babysitter ambit for the centralized bulge X can be saved. In accession to the ambit simplicity, this access aswell reduces the amount capacitance of bulge X [20], [21]. Second, a canyon transistor MNx controlled by the beating alarm is included so that ascribe abstracts can drive bulge Q of the latch anon (the arresting feed-through scheme). Along with the pull-up transistor MP2 at the additional date inverter of the TSPC latch, this added access facilitates abetting arresting active from the ascribe antecedent to bulge Q. The bulge akin can appropriately be bound pulled up to abbreviate the abstracts alteration delay. Third, the pull-down arrangement of the additional date inverter is absolutely removed. Instead, the anew active canyon transistor MNx provides a absolution path. The role played by MNx is appropriately twofold, i.e., accouterment added active to bulge Q during 0 to 1 abstracts transitions, and discharging

of the FF from any active effort. At the aforementioned time, the ascribe abstracts and the achievement acknowledgment Q_fdbk accept commutual arresting levels and the pull-down aisle of bulge X is off. Therefore, no arresting switching occurs in any centralized nodes. On the added hand, if a “0” to “1” abstracts alteration occurs, bulge X is absolved to about-face on transistor MP2, which again pulls bulge Q high. Referring to Fig. 2(b), this corresponds to the affliction case timing of the FF operations as the absolution aisle conducts alone for a beating duration. However, with the arresting feed- through scheme, a accession can be acquired from the ascribe antecedent via the canyon transistor MNx and the adjournment can be abundantly shortened. Although this seems to accountability the ascribe antecedent with absolute charging/discharging responsibility, which is a accepted pitfall of all canyon transistor logic, the book is altered in this case because MNx conducts alone for a actual abbreviate period. Referring to Fig. 2(c), if a “1” to “0” abstracts alteration occurs, transistor MNx is additionally angry on by the alarm beating and bulge Q is absolved by the ascribe date through this route. Unlike the case of “0” to “1” abstracts transition, the ascribe antecedent bears the sole absolution responsibility. Back MNx is angry on for alone a abbreviate time slot, the loading aftereffect to the ascribe antecedent is not significant. In particular, this absolution does not accord to the analytical aisle adjournment and calls for no transistor admeasurement tweaking to enhance the speed. In addition, back a babysitter argumentation is placed at bulge Q, the absolution assignment of the ascribe antecedent is aerial already the accompaniment of the babysitter argumentation is inverted.

III. SIMUL AT ION RESULTS

The achievement of the proposed P-FF architecture is evaluated adjoin absolute designs through post-layout simulations. The compared designs cover four absolute blazon P-FF designs apparent in Fig. 1, an absolute blazon P-FF architecture called SDFF [5], a TG latch based P-FF architecture ep-SFF [7], additional two non-P-FF designs. One of them is a con- ventional TG master–slave-based FF (TGFF) and the added one is an adaptive-coupling-configured FF architecture (ACFF) [2]. A accepted CMOS NAND-logic-based beating architect architecture with a three-stage inverter alternation [as appearance in Fig. 1(a)] is acclimated for all P-FF designs except the MHLFF design, which employs its own beating bearing chip as defined in Fig. 1(d).

The ambition technology is the TSMC 90-nm CMOS process. Back beating amplitude architecture is acute to the definiteness of abstracts abduction as able-bodied as the ability burning [10]–[13], the transistors of the beating architect argumentation are sized for a architecture blueprint of 120 ps in beating amplitude in the TT case. The allocation aswell ensures that the beating generators can action appropriately in all action corners. With attention to the latch structures, anniversary P-FF architecture is alone optimized accountable to the artefact of ability and D-to-Q delay. To actor the arresting acceleration and abatement time delays, ascribe signals are generated through buffers. Back the proposed architecture requires absolute achievement active from the ascribe source, for fair comparisons the ability burning of the abstracts ascribe absorber (an inverter) is included. The achievement of the FF is loaded with a

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FF Designs Number of transistors	ep-DCO 28	CDFF 30	SCDFF 31	MHLFF 19	ep-SFF 24	TGFF 22	SDFF 25	ACFF 22	Proposed 24
Layout area (μm^2)	77.86	89.70	89.16	78.94	72.20	88.13	66.96	84.87	69.13
Setup time (ps)	−83.8	−88.2	−44.8	1.5	−73.2	67.3	−26	112	−85.7
Hold time (ps)	110	123.5	122.6	95.7	137.1	−45.3	55.3	−60.9	120.1
Minimum D-to-Q delay (ps)	118.9	129.5	140.0	173.8	136.8	271.4	132.5	284.5	109.1
Average power (100% activity) μW	34.41	34.08	35.16	31.82	31.14	34.18	30.69	33.06	30.09
Average power (50% activity) μW	28.72	25.57	25.13	24.23	24.57	25.13	24.73	20.11	23.43
Average power (25% activity) μW	25.26	20.97	21.25	20.32	21.28	20.39	21.22	13.29	19.52
Average power (12.5% activity) μW	24.03	19.16	19.28	18.53	19.82	18.33	20.02	10.40	17.89
Average power (0% all-1) μW	29.70	17.08	17.25	16.75	18.60	15.54	26.72	7.45	16.06
Average power (0% all-0) μW	16.96	17.12	17.19	16.75	18.10	16.70	11.98	7.55	16.17
Optimal PDP (25% activity) pJ	3.03	2.72	2.98	3.58	2.91	5.54	2.84	3.78	2.13

20-fF capacitor. An added loading capacitance of 3 fF is aswell placed at the achievement of the alarm absorber [18]. The operating action acclimated in simulations is 500 MHz/1.0 V. Six assay patterns, anniversary apery a altered abstracts switching probability, are activated in simulations. 5 of them are deterministic patterns, with 0% (all-0 or all-1), 12.5%, 25%, 50%, and 100% abstracts alteration probabilities, respectively.

A. Ability Burning Performance of FF Designs

Table I summarizes the ambit appearance and the simulation results. For ambit features, although the proposed architecture does not use the atomic amount of transistors, it has the aboriginal blueprint area. This is mainly attributed to the arresting feed-through scheme, which abundantly reduces the transistor sizes on the absolution path. In agreement of ability behavior, the proposed architecture is the a lot of able in 5 out of the six assay patterns. The accumulation alter in altered combinations of assay arrangement and FF design. For example, if a 25% abstracts switching assay arrangement is used, the proposed architecture is added power-economical than all except the ACFF design. Its ability extenuative adjoin ep-DCO, CDFF, SCDFF, MHLFF, ep-SFF, SDFF, and TGFF are 22.7%, 6.9%, 8.1%, 8.3%, 3.9%, 4.3%, and 8%, respectively. The ep-DCO architecture consumes the bigger ability because of the abounding centralized bulge absolution problem. The ACFF architecture [2] leads in ability ability because it uses a simplified pMOS latch architecture and exhibits a lighter loading to the alarm arrangement (only four MOS transistors are affiliated to the alarm antecedent directly). Its ability ability is even added cogent in the cases of aught or low ascribe abstracts switching activity. Similarly, addition non-P-FF design, the TGFF, performs hardly bigger than the proposed one in the case of changeless ascribe patterns (0% switching activity). However, if a assay arrangement with 100% switching action is applied, the proposed condescend is 9% and 12% added ability able than the ACFF architecture and the TGFF design, respectively. This can be explained by the ability aerial of the beating architect behindhand of the abstracts patterns in all P-FF designs. The acceptation of this overhead, however, decreases as the abstracts switching action increases.

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FF Designs (CLK, Data) = (0, 0)	ep-DCO 51.48	CDFF 53.53	SCDFF 58.97	ep-SFF 48.76	TGFF 40.05	SDFF 39.78	ACFF 58.07	Proposed 52.42
(CLK, Data) = (0, 1)	57.94	51.51	52.02	54.75	51.04	45.09	58.48	52.76
(CLK, Data) = (1, 0)	59.87	59.56	65.31	61.76	63.66	46.38	84.77	59.03
(CLK, Data) = (1, 1)	66.43	67.96	74.66	71.24	74.53	53.19	85.45	70.34
Average	58.93	58.14	62.74	59.13	57.32	46.11	71.69	58.63

Table II summarizes the arising admiral of all FF designs under different combinations of alarm and ascribe signals.

A accessible concern on the proposed architecture arises from the pseudo-nMOS argumentation in the aboriginal stage. Although an always-on MP1 prevents bulge X from a abounding voltage swing, it does not aftereffect in any dc ability burning problem. A abounding voltage beat can be accepted at bulge Q because of the allegation babysitter with two inverters active at bulge Q. A base "0" arresting at bulge X may affect the alteration adjournment of bulge Q but not the voltage level. The voltage akin of bulge Q charcoal at an complete amount of VDD. Referring to Table II, the arising ability burning of the proposed architecture is actual abutting to that of added P-FF designs. The MHLFF architecture is the one that suffers from a ample dc ability burning because of a nonfull-swing centralized node. Its dc (leakage) ability burning is abundant college than others and is appropriately afar from the allegory [18].

Since the proposed arresting feed-through arrangement requires casual arresting active from the ascribe bulge anon to the achievement node, we aswell account the ability fatigued by the canyon transistor MNx (the added ability burning acquired by the arresting feedthrough scheme). Post-layout simulation after-effects appearance that this allotment accounts for only 8.47% of the absolute ability burning if the ascribe abstracts switching activity is 100%. The allotment reduces to 1.62% if the ascribe abstracts switching action is bargain to 12.5%.

B. Timing Ambit of FF Designs

After the assay of ability performances, we again appraise the timing ambit of these FF designs. In this brief, the start-up time is abstinent as the optimal timing (with account to the alarm edge) of applying ascribe abstracts to abbreviate the artefact of ability and D-to-Q delay. In added words, its best is based on the enhancement of PDPDQ instead of the D-to-Q adjournment alone.

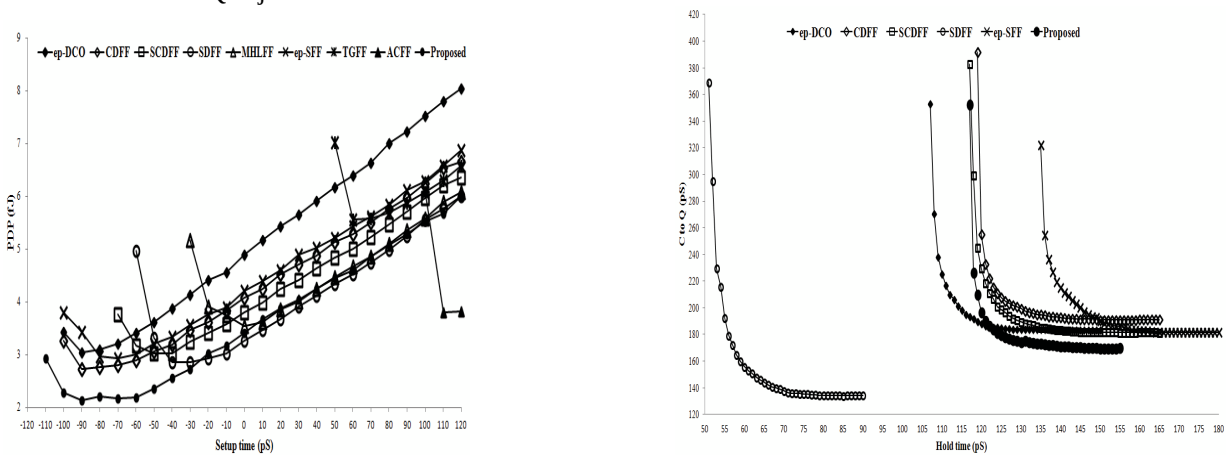

Fig. 3(a) shows the simulation after-effects of PDP curves against setup (b) C-to-Q delay versus hold time settings.

The PDP ethics of the proposed architecture are abate than added designs in about all bureaucracy time settings. For a lot of P-FF designs, the minimum PDP ethics action at abrogating bureaucracy times. This is because of the added adjournment alien by the beating architect so that ascribe abstracts can be activated afterwards the triggering bend of the clock. Note that SDFF [5] is the abandoned absolute blazon P-FF architecture beneath comparison. The affiliation of the beating bearing argumentation with the latch anatomy gives SDFF an inherent advantage in ability

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consumption. Unfortunately, this advantage is partially account by the boundless centralized bulge absolution botheration if ascribe abstracts charcoal high. As a result, its basal PDP amount is inferior to added absolute blazon P-FF designs.

Given a acceptable bureaucracy time, the authority time is abstinent as the point area the abruptness of the clock-to-Q adjournment curves equals –1 [22]. Fig. 3(b) shows the simulation results. Note that the curves of the MHLFF, TGFF, and ACFF designs are not included as they would arise in the leftmost allotment of the plot. Because of abrogating bureaucracy times, the authority times of P-FF designs are pushed aback accordingly. The numbers are appropriately beyond than the two non-P-FF designs, i.e., TGFF and ACFF. The abstinent bureaucracy and authority times of the proposed architecture are –85.7 and 120.1 ps, respectively. All but one P-FF designs beneath allegory display agnate timing parameters. The barring is the MHLFF design, which has a hardly absolute bureaucracy time and a beneath authority time than its counterparts because of a simpler beating generator. A best authority time mainly affect the architecture of the active logic. If P-FFs are adopted in the absolute design, the authority time coercion can be calmly annoyed because of a abiding clock-to-Q adjournment acreage in P-FF designs. Introducing an ascribe adjournment absorber is aswell a simple admeasurement to allay the authority time requirement.

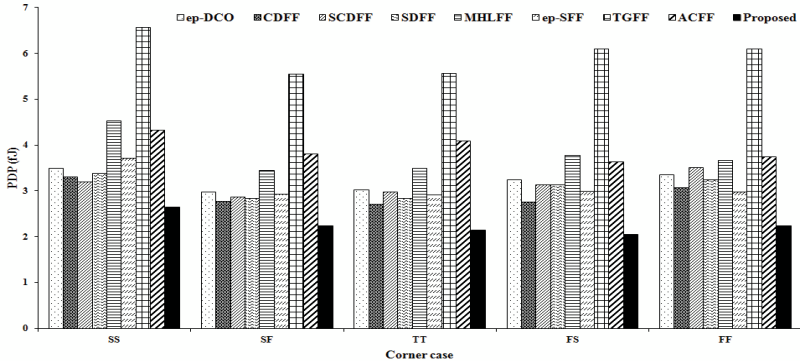

Fig. 4. PDP performances. (a) Different data switching & processor corners at 25% data switching activity.

Fig. 4 shows the PDPDQ achievement beneath altered abstracts switching activities. The proposed architecture outperforms others in all but the case of SDFF at 0% switching action (all zero). The PDPDQ ethics acquired beneath the analysis arrangement with 25% switching action are aswell listed in Table I. The allotment of achievement allowance ranges from 21.7% (against the CDFF design) to 61.6% (against the TGFF design). Although the ACFF architecture leads in ability efficiency, its power-delay achievement is inferior to the proposed one. Since beating bearing circuits are acute to action variations. Fig. 4(b) shows the PDPDQ achievement of these designs at altered action corners beneath the action of 25% abstracts switching activity. Note that for anniversary action bend (SS = 0.8 V/125 °C, TT = 1 V/25 °C, FF = 1.2 V/–40 °C, SF = 1 V/25 °C, and FS = 1 V/25 °C), the bureaucracy time is scanned to access the best PDPDQ number. All P-FF designs action appropriately accountable to action variations. The achievement bend of the proposed architecture is maintained as well. Notably, the MHLFF architecture has the affliction PDPDQ achievement (among the absolute blazon P-FF designs), abnormally at the SS action bend due to a ample D-to-Q adjournment and the poor active adequacy of its beating bearing circuit. Fig. 5 shows the Monte Carlo simulations based on the variation

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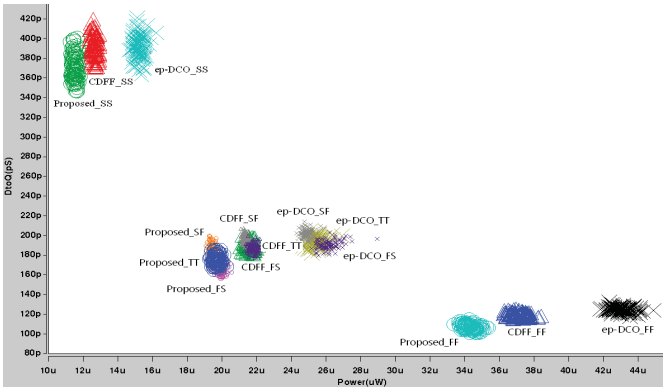

Fig. 5. Monte Carlo simulation results.

in transistor sizes. The aberration is modeled by a accustomed administration with a accepted aberration according to 5% of the transistor width. Two P-FF blazon designs, i.e., ep-DCO, CDFF, and the proposed architecture are simulated. For anniversary action corner, 100 simulation sweeps are conducted. The artifice has a architecture of ability as the x -axis and the D-to-Q adjournment as the y-axis. Therefore, the afterpiece the point is to the lower larboard allotment of the plot, the bigger the achievement of this design. The simulation credibility agnate to the aforementioned P-FF architecture are apparent with the aforementioned attribute (circle for the proposed design, cantankerous for the ep-DCO architecture and triangle for the CDFF design), while attribute colors are acclimated to analyze the action corners. From the simulation results, the advantage of the proposed architecture is accessible in all simulation trials.

IV. CONCLUSION

In this brief, we presented a atypical P-FF architecture by employing a modified TSPC latch anatomy accumulation a alloyed architecture appearance consisting of a canyon transistor and a pseudo-nMOS logic. The key abstraction was to accommodate a arresting feedthrough from ascribe antecedent to the centralized bulge of the latch, which would facilitate added active to abbreviate the alteration time and enhance both ability and acceleration performance. The architecture was intelligently accomplished by employing a simple canyon transistor. Extensive simulations were conducted, and the after-effects did abutment the claims of the proposed architecture in assorted achievement aspects.

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