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Survey of FPGA Implementation of Various Length Multiplier based on Compressor

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ABSTRACT: With the advent of new technology in the fields of VLSI and communication, there is also an ever growing demand for high speed processing and low area design. It is also a well-known fact that the multiplier unit forms an integral part of processor design. Due to this regard, high speed multiplier architectures become the need of the day. In this paper, we have developed three designs for Urdhwa Multiplier. In first design we have developed 4:2 compressors based on full adder and utilization in term of 42 delays and 21 areas. In second design we have developed 4:2 compressors based on XOR gate and utilization in term of 36 delays and 24 areas. In third design we have developed 4:2 compressors based on full adder and utilization in term of 28 delays and 18 areas.

KEYWORDS: 4:2 Compressor based on Full Adder, 4:2 Compressor based on XOR Gate, 4:2 Compressor based on XOR-XNOR Gate

I. INTRODUCTION

Digital signal processing (DSP) is the mathematical manipulation of an information signal to modify or improve it in some way. It is characterized by the representation of discrete time, discrete frequency, or other discrete domain signals by a sequence of numbers or symbols and the processing of these signals [1].

The goal of DSP is usually to measure, filter and/or compress continuous real-world analog signals. The first step is usually to convert the signal from an analog to a digital form, by sampling and then digitizing it using an analog-to-digital converter (ADC), which turns the analog signal into a stream of numbers. However, often, the required output signal is another analog output signal, which requires a digital-to-analog converter (DAC). Even if this process is more complex than analog processing and has a discrete value range, the application of computational power to digital signal processing allows for many advantages over analog processing in many applications, such as error detection and correction in transmission as well as data compression. DSP algorithms have long been run on standard computers, as well as on specialized processors called digital signal processor and on purpose-built hardware such as application-specific integrated circuit (ASICs). Today there are additional technologies used for digital signal processing including more powerful general purpose microprocessors, field-programmable gate arrays (FPGAs), digital signal controllers (mostly for industrial apps such as motor control), and stream processors, among others [2-3].

Multipliers are extensively used in Microprocessors, DSP and Communication applications. For higher order Multiplications, a huge number of adders are to be used to perform the partial product addition. The need of low power and high speed Multiplier is increasing as the need of high speed processors are increasing. The Vedic multiplication technique is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems [1]. The mathematical operations using, Vedic Method are very fast and requires less hardware, this can be used to improve the computational speed of processors. This paper describes the design and implementation of 4x4 bit Vedic multiplier based on Urdhva- Tiryakbhyam sutra (Vertically and Crosswise technique) of Vedic Mathematics using EDA (Electronic Design Automation) tool. The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple ones. This is so because

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the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Vedic Mathematics is a methodology of arithmetic rules that allow more efficient speed implementation. It also provides some effective algorithms which can be applied to various branches of engineering such as computing.

II. LITERATURE REVIEW

Jiafeng Xie et al. [1], redundant basis (RB) multipliers over Galois Field have gained huge popularity in elliptic curve cryptography (ECC) mainly because of their negligible hardware cost for squaring and modular reduction. In this paper, we have proposed a novel recursive decomposition algorithm for RB multiplication to obtain high-throughput digit-serial implementation. Through efficient projection of signal-flow graph (SFG) of the proposed algorithm, a highly regular processor-space flow-graph (PSFG) is derived. By identifying suitable cut-sets, we have modified the PSFG suitably and performed efficient feed-forward cut-set retiming to derive three novel multipliers which not only involve significantly less time-complexity than the existing ones but also require less area and less power consumption compared with the others. Both theoretical analysis and synthesis results confirm the efficiency of proposed multipliers over the existing ones. The synthesis results for field programmable gate array (FPGA) and application specific integrated circuit (ASIC) realization of the proposed designs and competing existing designs are compared. It is shown that the proposed high-throughput structures are the best among the corresponding designs, for FPGA and ASIC implementation.

Sushma R. Huddar [2], with the advent of new technology in the fields of VLSI and communication, there is also an ever growing demand for high speed processing and low area design. It is also a well-known fact that the multiplier unit forms an integral part of processor design. Due to this regard, high speed multiplier architectures become the need of the day. In this paper, we introduce a novel architecture to perform high speed multiplication using ancient Vedic maths techniques. A new high speed approach utilizing 4:2 compressors and novel 7:2 compressors for addition has also been incorporated in the same and has been explored. Upon comparison, the compressor based multiplier introduced in this paper, is almost two times faster than the popular methods of multiplication. With regards to area, a 1% reduction is seen. The design and experiments were carried out on a Xilinx Spartan 3e series of FPGA and the timing and area of the design, on the same have been calculated.

D. Radhakrishnan [3], novel CMOS 4-2 compressor using pass logic is presented in this paper. An XOR-XNOR combination gate is used to build the circuit while totally eliminating the use of inverters. The total power dissipation has been cut down to a minimum while providing the full output voltage swing at all nodes in the circuit. Furthermore, the complete circuit is implemented with a bare minimum of 28 transistors.

L. Sriraman et al. [4], in this paper, a novel multiplier architecture based on ROM approach using Vedic Mathematics is proposed. This multiplier's architecture is similar to that of a Constant Coefficient Multiplier (KCM). However, for KCM one input is to be fixed, while the proposed multiplier can multiply two variables. The proposed multiplier is implemented on a Cyclone III FPGA, compared with Array Multiplier and Urdhava Multiplier for both 8 bit and 16 bit cases and the results are presented. The proposed multiplier is 1.5 times faster than the other multipliers for 16x16 case and consumes only 76% area for 8x8 multiplier and 42% area for 16x16 multiplier.

Himanshu Thapliyal et al. [5], the major time consuming arithmetic operations in ECC are point additions and doubling. Exponentiation operations like square and cube are the major bottlenecks in the efficiency of point additions and doubling. This paper presents efficient hardware circuitry for point doubling using square algorithms of Ancient Indian Vedic Mathematics. In order to calculate the square of a number, "Duplex" D property of binary numbers is proposed.

Honey Durga Tiwari et al. [6], Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). It mainly deals with Vedic mathematical formulae and their application to various branches of mathematics. The algorithms based on conventional mathematics can be simplified and even optimized by the use of Vedic Sutras. These methods and ideas can be directly applied to trigonometry, plain and spherical geometry, conics, calculus (both differential and integral), and applied mathematics of various kinds. In this paper new multiplier and square architecture is proposed based on algorithm of

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ancient Indian Vedic Mathematics, for low power and high speed applications. It is based on generating all partial products and their sums in one step. The design implementation on ALTERA Cyclone –II FPGA shows that the proposed Vedic multiplier and square are faster than array multiplier and Booth multiplier.

III. URDHWA MULTIPLIER

Vedic mathematics is an ancient fast calculation mathematics technique which is taken from historical ancient book of wisdom. Vedic mathematics is an ancient Vedic mathematics which provides the unique technique of mental calculation with the help of simple rules and principles. Swami Bharati Krishna Tirtha (1884-1960), former Jagadguru Sankaracharya of Puri culled set of 16 Sutras (aphorisms) and 13 Sub - Sutras (corollaries) from the Atharva Veda. He developed methods and techniques for amplifying the principles contained in the formulas and their sub-formulas, and called it Vedic Mathematics. According to him, there has been considerable literature on Mathematics in the Veda-sakhas.

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.

- **4:2 Compressor based on Full Adder**

To add binary numbers with minimal carry propagation we use compressor adder instead of other adder. Compressor is a digital modern circuit which is used for high speed with minimum gates requires designing technique. This compressor becomes the essential tool for fast multiplication adding technique by keeping an eye on fast processor and lesser area.

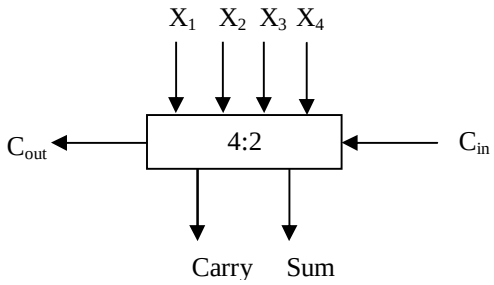

Figure 1: Block Diagram of 4:2 Compressors

4:2 compressors are capable of adding 4 bits and one carry, in turn producing a 3 bit output. The 4:2 compressors has 4 inputs G_1, G_2, G_3 and G_4 and 2 outputs Sum and Carry along with a Carry-in (Cin) and a Carry-out (Cout) as shown in Figure 1. The input Cin is the output from the previous lower significant compressor.

The Cout is the output to the compressor in the next significant stage. The critical path is smaller in comparison with an equivalent circuit to add 5 bits using full adders and half adders. The 4:2 compressors is governed by the basic equation

$$X_1 + X_2 + X_3 + X_4 + C_{in} = Sum + 2 * (Carry + C_{out}) \quad (1)$$

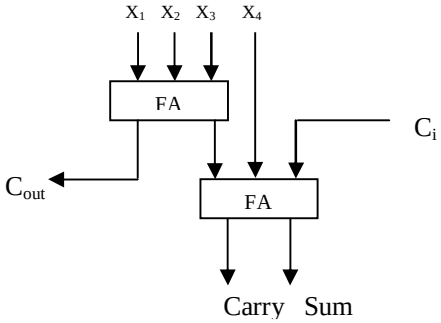

Figure 2: 4:2 Compressors based on Full Adder

The standard implementation of the 4:2 compressors is done using 2 Full Adder cells as shown in Figure 2.

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- **4:2 Compressor based on XOR Gate**

When the individual full Adders are broken into their constituent XOR blocks, it can be observed that the overall delay is equal to 4*XOR. The block diagram in figure 3 shows the existing architecture for the implementation of the 4:2 compressor with a delay of 3*XOR. The equations governing the outputs in the existing architecture are shown below

$$Sum = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus C_{in} \quad (2)$$

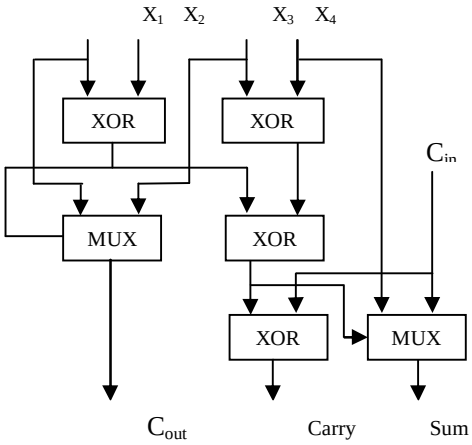

Figure 3: 4:2 Compressors based on XOR Gate

$$C_{out} = (X_1 \oplus X_2).X_3 + \overline{(X_1 + X_2)} \cdot X_3 \quad (3)$$

$$Carry = (X_1 \oplus X_2 \oplus X_3 \oplus X_4) \cdot C_{in} + \overline{(X_1 \oplus X_2 \oplus X_3 \oplus X_4)} \cdot X_4 \quad (4)$$

- **Compressor based on XOR Gate**

Thus replacing some XOR blocks with multiplexer's results in a significant improvement in delay. Also the MUX block at the SUM output gets the select bit before the inputs arrive and thus the transistors are already switched by the time they arrive. This minimizes the delay to a considerable extent. This is shown in figure 4.

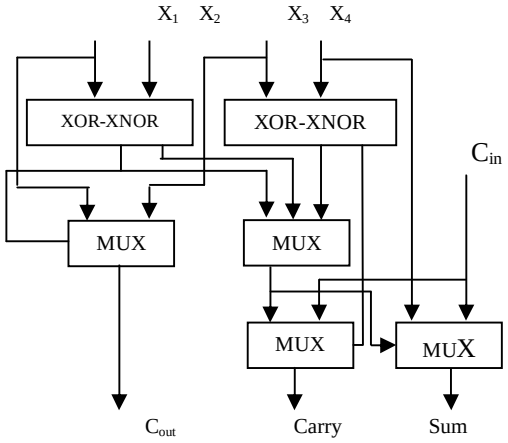

Figure 4: 4:2 Compressors based on XOR-XNOR Gate

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The equations governing the outputs in the proposed architecture are shown below

$$Sum = (X_1 \oplus X_2) \cdot (X_3 \oplus X_4) \uparrow (X_1 \oplus X_2) \cdot (X_3 \oplus X_4) \cdot C_{in} \quad (5)$$

$$C_{out} = (X_1 \oplus X_2) \cdot X_3 + \overline{(X_1 + X_2)} \cdot X_1 \quad (6)$$

$$Carry = (X_1 \oplus X_2 \oplus X_3 \oplus X_4) \cdot C_{in} + \overline{(X_1 \oplus X_2 \oplus X_3 \oplus X_4)} \cdot X_4 \quad (7)$$

- **7:2 Compressor**

Similar to its 4:2 compressor counterpart, the 7:2 compressors as shown in figure 5, is capable of adding 7 bits of input and 2 carry's from the previous stages, at a time. In our implementation, we have designed a novel 7:2 compressor utilizing two 4:2 compressors, two full adders and one half adders. The architecture for the same has been shown in Figure 5.

$$Sum1 = S_1 \oplus S_2 \quad (8)$$

$$Carry1 = S_3 \oplus C_1 \oplus C_{21} \quad (9)$$

$$C_{out1} = C_3 \oplus C_2 \oplus C_{22} \quad (10)$$

$$C_{out2} = C_3 C_2 + C_{22} C_2 + C_3 C_{22} \quad (11)$$

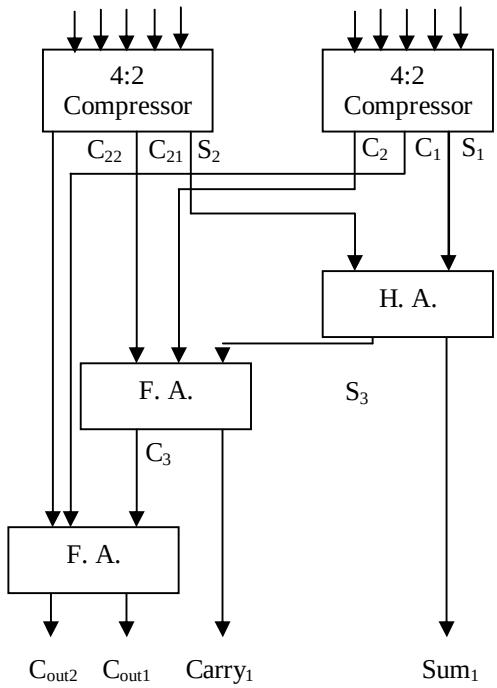

Figure 5: 7:2 Compressor using 4:2 Compressor

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IV. DELAY AND AREA EVALUATION METHODOLOGY

The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter (AOI), each having delay equal to 1 unit and area equal to 1 unit.

Table 1: Delay and Area Count of the Basic Blocks of Urdhwa Multiplier

Adder Blocks	Delay	Area
XOR	3	5
2:1 MUX	3	4
Half Adder	3	6
Full Adder	6	13

We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block.

V. SIMULATION RESULT

We functionally verified each unit presented in this paper including all three 4:2 Compressor, 7:2 Compressor, Compressor based Urdhwa multiplier. We have been found from the results shown in Table 3 respectively, that number of slices used is same in case of 4:2 compressor based on Full adder and 4:2 compressor based on XOR gate which is less than slices used in 4:2 compressor based on XOR-XNOR gate.

Table II: Delay and Area Count of the of Urdhwa Multiplier

Architecture	No. of Gate Count	Delay
4:2 Compressor based on Full Adder	42	21
7:2 Compressor	116	57
Compressor based Urdhwa Multiplier	1132	591
4:2 Compressor based on XOR Gate	36	24
Modified 7:2 Compressor	104	63
Modified Compressor based Multiplier	1012	654
4:2 Compressor based on XOR-XNOR Gate	28	18
Proposed 7:2 Compressor	88	51
Proposed Compressor based Multiplier	852	531

VI. CONCLUSION

Among all three designs, proposed Urdhwa multiplier based on XOR-XNOR gate provides the least amount of Maximum combinational path delay (MCDP). Also, it takes least number of slices i.e. occupy least area among all three design.

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