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Network on Chip Based on Adaptive Routing Algorithm

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ABSTRACT: Synchronous networks-on-chip (NoC) require tailored schedulers achieving low latency, high throughput, and fairness while avoiding packet collisions. Efficient schedulers exist for rearrangeable non-blocking NoC. However, NoCs fabricated in integrated photonics typically suffer a blocking behavior due to the limitations of the switching capabilities in the space and wavelength domains. This paper discusses a scheduler for an integrated optical NoC based on a ring topology and realized with multiple resonating microrings (multi-microring, MMR). Scheduling in MMR architecture consists of the conventional matching sub-problem and the wavelength assignment sub-problem. The paper's contribution is twofold. Advanced adaptive parallel wavelength matching (aaPWM) algorithm .In addition, bidirectionality with one or two transceivers per port is proposed as a way to overcome the throughput degradation caused by the blocking behavior. Simulation results indicate that bidirectionality is very effective in improving the throughput and reducing the latency even when using a single transceiver

I. INTRODUCTION

Network on chip is a communication subsystem on an integrated circuit (commonly called a "chip"), typically between IP cores in a system on a chip (SoC). NoCs can span synchronous and asynchronous clock domains or use unclocked asynchronous logic. NoC technology applies networking theory and methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnections. NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs Network on chip is an emerging paradigm for communications within large VLSI systems implemented on a single silicon chip. In a NoC system, modules such as processor cores, memories and specialized IP blocks exchange data using a network as a "public transportation" sub-system for the information traffic. A NoC is constructed from multiple point-to-point data links interconnected by switches , such that messages can be relayed from any source module to any destination module over several links, by making routing decisions at the switches. A NoC is similar to a modern telecommunications network, using digital bit-packet switching over multiplexed links. Although packet-switching is sometimes claimed as necessity for a NoC, there are several NoC proposals utilizing circuit-switching techniques.

II. DESIGN AND ANALYSIS OF DATA TRANSMISSION MODULE

The data transmission module is the basic module in the smart reliable network on chip. In transmission module first we encrypted the data or information before transmission and we transmit the encrypted data according to the enable signal.The proposed NoC is based on new error detection mechanisms suitable for dynamic NoCs, where the number and position of processor elements or faulty blocks vary during runtime. Recently the trend of embedded systems has been moving toward multiprocessor systems-on-chip in order to meet the requirements of real-time applications. The complexity of these SoCs is increasing and the communication medium is becoming a major issue of them MPSoC. Generally, integrating a network-on-chip into the SoC provides an effective means to interconnect several processor elements (PEs) or intellectual properties (IP) .The NoC medium features a high level of modularity, flexibility, and throughput. An NoC comprises routers and interconnections allowing communication between the PEs and/or IPs. The NoC relies on data packet exchange. The path for a data packet between a source and a destination through the routers is defined by the routing algorithm. Therefore, the path that a data packet is allowed to take in the network depends mainly on the adaptiveness permitted by the routing algorithm, which is applied locally in each router being crossed and to each data packet.

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ANALYSIS OF NODES AND NETWORKS

In this module, design and analyses the nodes in the reliable network. Thus the node in the network is designed for establishing the link between the source and destination. The nodes in the network having different node value, calculate the all possible route value before transmit the data to the destination with respect to the node value and choose the reliable path for networking.In network module, design the network and analyses the performance. The network is designed by make the link between the active nodes in the design.To make the reliable operation we use the advanced adaptive routing algorithm. In this method, detect the faulty nodes in the network is adaptive and make sure the reliability.

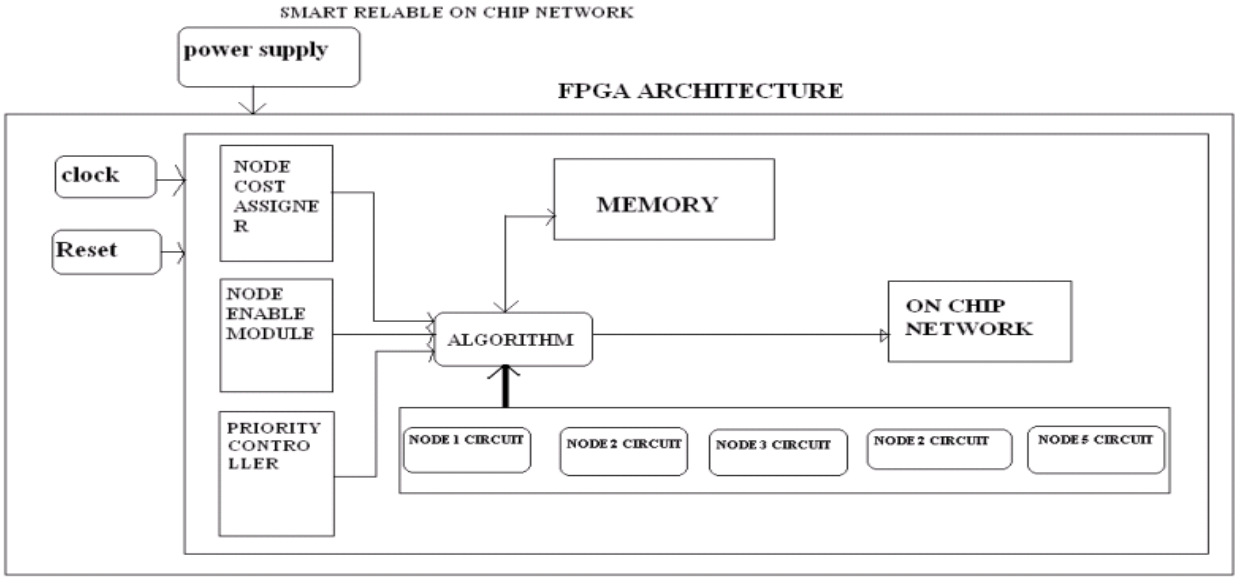
III. PROPOSED ALGORITHM

In the proposed design Advanced Routing Algorithm is implemented where the data packets are sent in high speed and priority based approach. The advantage of doing this reduces the frequent checking of unconnected nodes and making the return path delay. In the proposed system we implement various nodes and then design some logic module inside each node. The logic module inside the each node is considering as the process designed inside the integrated circuit. Moreover, we implement the self replacement concept in the proposed system so it handle error 0r fault by itself. The implementation of self replacement concept achieves advantage in terms of time.

PARALLELISM AND SCALABILITY

The wires in the links of the NoC are shared by many signals. A high level of parallelism is achieved, because all links in the NoC can operate simultaneously on different data packets. Therefore, as the complexity of integrated systems keeps growing, a NoC provides enhanced performance (such as throughput) and scalability in comparison with previous communication architectures (e.g., dedicated point-to-point signal wires, shared buses, or segmented buses with bridges). Of course, the algorithms must be designed in such a way that they offer large parallelism and can hence utilize the potential of NoC.

IV. BLOCK DIAGRAM



BENEFITS OF ADAPTING NOCs

Traditionally, ICs have been designed with dedicated point-to-point connections, with one wire dedicated to each signal. For large designs, in particular, this has several limitations from a physical design viewpoint.

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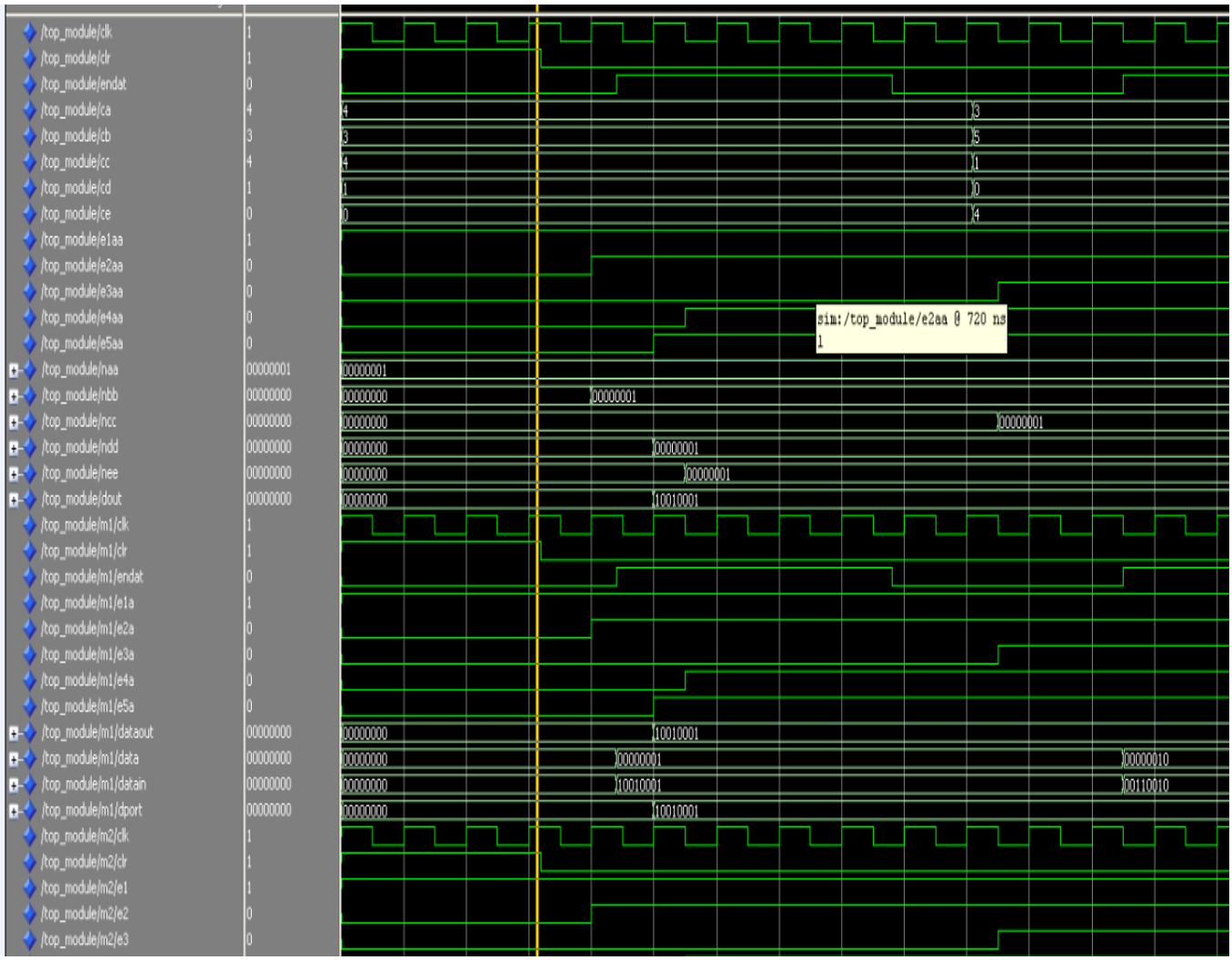
The wires occupy much of the area of the chip, and in nanometer CMOS technology, interconnects dominate both performance and dynamic power dissipation, as signal propagation in wires across the chip requires multiple clock cycles. NoC links can reduce the complexity of designing wires for predictable speed, power, noise, reliability, etc. From a system design viewpoint, with the advent of multi-core processor systems, a network is a natural architectural choice. A NoC can provide separation between computation and communication, support modularity and IP reuse via standard interfaces, handle synchronization issues, serve as a platform for system test, and, hence, increase engineering productivity.

V. RESULT



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VI. CONCLUSION

In smart reliable network on chip, first we designed the transmission module for transmit the data or information to the destination network. Before transmitting the data we are encrypt the transmitting data using encryption module. After encryption we transmit the data based on the enable signal. In second we designed the nodes for interconnecting the source and destination ,after design of nodes we are interconnected the nodes to create the network for proper transmission of data. In this project we designed the adaptive routing algorithm for selecting the data and detecting the faulty nodes in the network. Finally we interconnect the all sub_modules in the design and analyse the output.

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