Implementation of Robust Router Design for Area Critical Applications

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ABSTRACT: The router is a" **Network Router**" has a one input port from which the packet enters. It has five output ports where the packet is driven out. Packet contains 2 parts. They are data (payload) and address sequence. Packet width is 8 bits and the length of the packet transferring can be between 1 bytes to 63 bytes. The switch drives the packet to respective ports based on this destination address of the packets. Each output port has 3-bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 5 bits. In this paper the Xilinx ISE EDA Tool is used for synthesis and Modelsim is used for simulation. In the proposed design the FSM is designed with reduced number of states. Due to reduction of states the amount of time to produce the response became less obviously the frequency is improved. At the same time the memory required to design of this Router chip is also reduced. In the existed design no of LUTS are 724. In the existed design the Total memory usage is 297148 kilobytes and the maximum Frequency is 76.374MHz.Where as in the proposed design the no of LUTS are 240.In the proposed design the Total memory usage is 249164 kilobytes and the maximum Frequency is 81.162MHz.

KEYWORDS: Router; Verilog; Finite State Machine; Look Up Tables.

I. INTRODUCTION

A router is a device that forwards data packets between computer networks. This creates an overlay internetwork, as a router is connected to two or more data lines from different networks. When a data packet comes in one of the lines, the router reads the address information in the packet to determine its ultimate destination. Then, using information in its routing table or routing policy, it directs the packet to the next network on its journey. Routers perform the "traffic directing" functions on the Internet. A data packet is typically forwarded from one router to another through the networks that constitute the internetwork until it reaches its destination node.

The most familiar type of routers are home and small office routers that simply pass data, such as web pages, email, IM, and videos between the home computers and the Internet. An example of a router would be the owner's cable or DSL router, which connects to the Internet through an ISP. More sophisticated routers, such as enterprise routers, connect large business or ISP networks up to the powerful core routers that forward data at high speed along the optical fiber lines of the Internet backbone. Though routers are typically dedicated hardware devices, use of software-based routers has grown increasingly common.

What defines a router is not its shape, color, size or manufacturer, but its job function of routing data packets between computers. A cable modem which routes data between your PC and your ISP can be considered a router. In its most basic form, a router could simply be one of two computers running the Windows 98 (or higher) operating system connected together using ICS (Internet Connection Sharing). In this scenario, the computer that is connected to the Internet is acting as the router for the second computer to obtain its Internet connection. Going a step up from ICS, we have a category of hardware routers that are used to perform the same basic task as ICS, albeit with more features and functions. Often called broadband or Internet connection sharing routers, these routers allow you to share one Internet connection computers.

Routing is the process of selecting best paths in a network. In the past, the term routing was also used to mean forwarding network traffic among networks. However this latter function is much better described as simply

forwarding. Routing is performed for many kinds of networks, including the telephone network (circuit switching), electronic data networks (such as the Internet), and transportation networks. This article is concerned primarily with routing in electronic data networks using packet switching technology. In packet switching networks, routing directs packet forwarding (the transit of logically addressed network packets from their source toward their ultimate destination) through intermediate nodes. Intermediate nodes are typically network hardware devices such as routers, bridges, gateways, firewalls, or switches. In many instances, an ISP will allow you to use a router and connect multiple computers to a single Internet connection and pay a nominal fee for each additional computer sharing the connection. This is when home users will want to look at smaller routers, often called broadband routers that enable two or more computers to share an Internet connection. Within a business or organization, you may need to connect multiple computers to the Internet, but also want to connect multiple private networks not all routers are created equal since their job will differ slightly from network to network. General-purpose computers can also forward packets and perform routing, though they are not specialized hardware and may suffer from limited performance. The routing process usually directs forwarding on the basis of routing tables which maintain a record of the routes to various network destinations. Thus, constructing routing tables, which are held in the router's memory, is very important for efficient routing. Most routing algorithms use only one network path at a time. Multipath routing techniques enable the use of multiple alternative paths. In case of overlapping/equal routes, the following elements are considered in order to decide which routes get installed into the routing table (sorted by priority).

II. PRINCIPLE

In Specified the compact contest limit and the short implementation window we adopted a set of design principles to spend the on hand time as proficiently as possible. This document provides specifications for the Router is a packet base protocol. Router drives the incoming packet which comes from the enter port to output ports based on the address contained in the packet. The router is a "Network Router" has a one input port from which the packet enters. It has three amount produced ports where the packet is driven out. Packet contains 2 parts. They are data and address sequence. Packet width is 8 bits and the length of the packet can be between 1 byte to 63bytes. Packet header contains three fields DA and length. Goal address (DA) of the packet is of 8 bits. The switch drives the packet to personal ports based on this destination address of the packets. Each output port has 8-bit unique port address. If the objective address of the packet matches the port address, then switch drives the envelope to the output port, Length of the data is of 8 bits and from 0 to 33.Length is exact in terms of bytes. Data should be in terms of bytes and can take anything. Outline check sequence contains the security check of the packet. It is calculated over the subtitle and data. The communication on network on chip is carried away from home by means of router, so meant for implement better NOC , the router should be efficiently design. This router chains three similar connections at the same time. It uses store and forward type of flow control in count to FSM Controller deterministic steering which improves the act of router. The router is an "association Router" has a one input port from which the packet enters. It has five crop ports where the packet is motivated out. Carton contains 2 parts. They are data and address sequence. Packet width is 8 bit and the length of the pot can be sandwiched between 1 byte to 63 bytes. Packet header contains three fields DA and length. Goal address (DA) of the envelope is of 8 bits. The switch drives the packet to respective ports based on this destination tackle of the packets. Each output port has speck unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits and from 0 to 62.

The register has a positive edge clock, an active high clock enable and an active high asynchronous reset. The output of the register is the input of the de-multiplexer. The data input to the register is transferred to the output port at the positive edge of the clock if and only if the enable is 1 and the reset is 0. If the reset is 1, then the output port of the register is set to zeros. If the enable is 0, then the output port keeps its current value. Since ROUTER is synchronous, it has a clock pulse along with the data. RS-232 and other asynchronous protocols do not use a clock pulse, but the data must be timed very accurately. Since ROUTER has a clock signal, the clock can vary without disrupting the data. The data rate will simply change along with the changes in the clock rate. The five Router Design is done by using of the five blocks .The blocks are 8-Bit Register, Router controller and output block. The router controller is design by using FSM design and the output block consists of five ways to transmit the payload. These functions are discussed clearly.
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III. OPERATION

The Five Port Router Design is done by using of the three blocks. The blocks are 8-Bit Register, Router Controller and output block. The router controller is design by using FSM design and the output block consists of four FIFO's combined together. The FIFO's store data packets and when you want to send data that time the data will read from the FIFO's. In this router design has five output ports. It is used to drive the data into router. The paper using the global clock, reset signals and suspended data signals are the outputs of the router. The FSM controller gives the SUSPENDED_DATA information also.
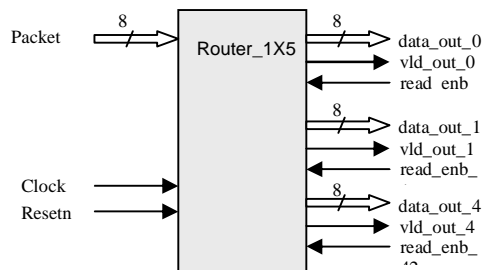
Fig 1. Block Diagram of Router Protocol

These functions are discussed clearly in below FSM description. The ROUTER can operate with a single master device and with one or more slave devices. If a single slave device is used, the RE (read enable) pin may be fixed to logic low if the slave permits it. Some slaves require the falling edge (HIGH→LOW transition) of the slave select to initiate an action such as the mobile operators, which starts conversion on said transition. With multiple slave devices, an independent RE signal is required from the master for each slave device.
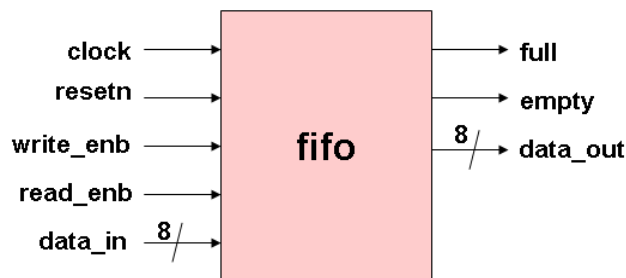

Fig 2. FIFO Block

There are 5 fifos used in the router design. Each FIFO is of 8 bit width and 16 bit depth. The FIFO works on system clock. It has synchronous input signal reset. If resetn is low then full is 0, empty is 1 and data_out 0. In the Write operation, the data from input data_in is sampled at rising edge of the clock when input write_enb is high and FIFO is not full. In the Read Operation, the data is read from output data_out at rising edge of the clock, when read_enb is high and FIFO is not empty. Read and Write operation can be done simultaneously. Full indicates that all the locations inside FIFO have been written. Empty indicates that all the locations of FIFO are empty.
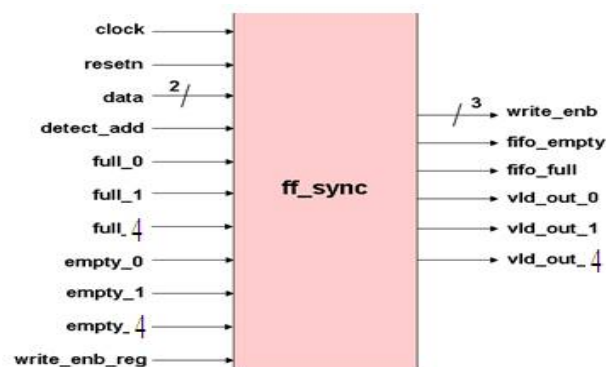
Fig 3. Synchronous Block

This module provides synchronization between fsm and FIFO modules.4 it provides faithful communication between single input port and three output ports. It will detect the address of channel and will latch it till packet_valid is asserted; address and write_enb_reg will be used for latching the incoming data into the FIFO of that particular channel. A fifo_full output signal is generated, when the present FIFO is full, and fifo_empty output signal is generated by the present FIFO when it is empty. The output vld_out signal is generated when empty of present FIFO goes low, that means present FIFO is ready to read. The write_enb_reg signal which comes from the fsm is used to generate write_enb signal for the present FIFO which is selected by present address.
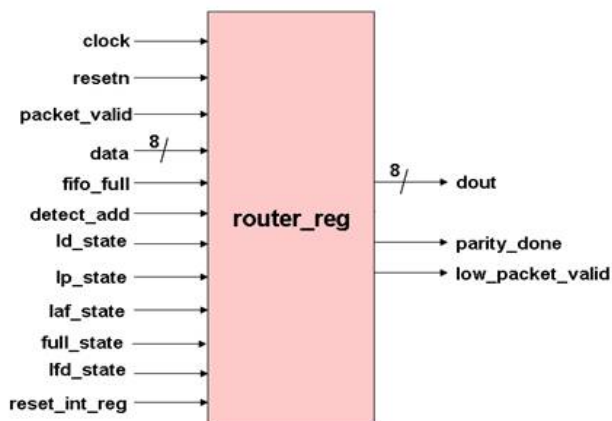

Fig 4: Router Register Block

This module contains status, data and parity registers required by router. All the registers in this module are latched on rising edge of the clock. Data registers latches the data from data input based on state and status control signals, and this latched data is sent to the fifo for storage. Apart from it, data is also latched into the parity registers for parity calculation and it is compared with the parity byte of the packet. An error signal is generated if packet parity is not equal to the calculated parity. Internal parity register stores the parity calculated for packet data, when packet is transmitted fully, the internal calculated parity is compared with parity byte of the packet. An error signal is generated if packet parity is not equal to the calculated parity. The 'fsm_router' module is the controller circuit for the router. This module generates all the control signals when new packet is sent to router. These control signals are used by other modules to send data at output, writing data into the fifo.

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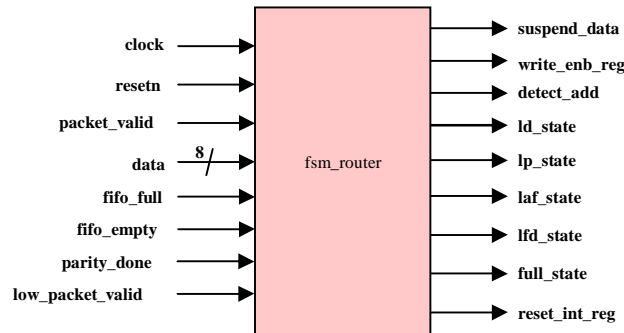
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Fig 5.FSM Router
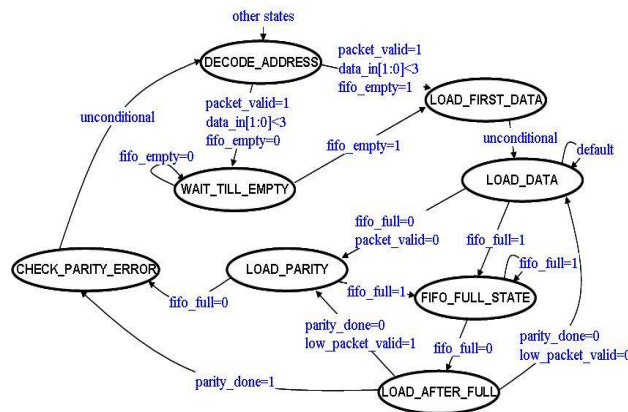

Fig 6. FSM State Diagram

IV. RESULTS

In this paper the Xilinx ISE EDA Tool is used for synthesis and for simulation.
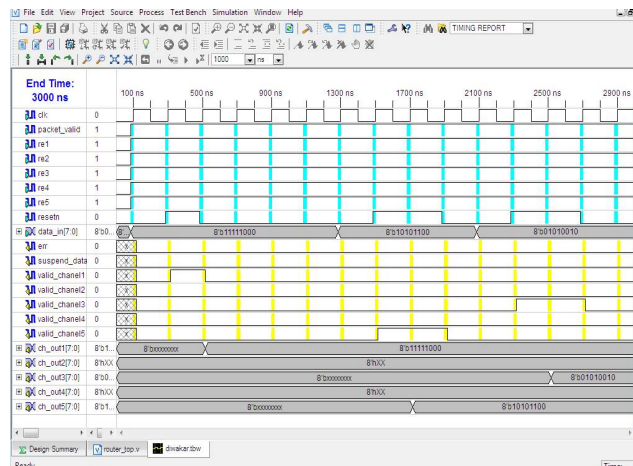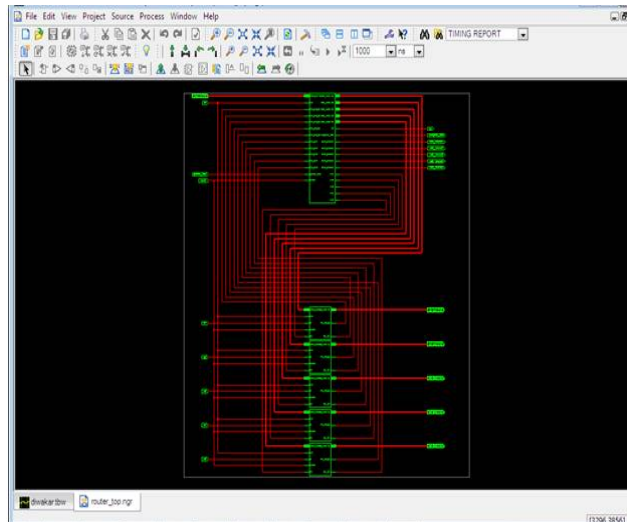

Fig 7. Test bench results

Fig 8. RTL SCHEMATIC Diagram

Table 1. Device Utilization Summary

Logic Utilization	Used	Available	Utilization
Total Number Slice Registers	112	1,536	7%
Number used as Flip Flops	72		
Number used as Latches	40		
Number of 4 input LUTs	229	1,536	14%
Logic Distribution			
Number of occupied Slices	178	768	23%
Number of Slices containing only related logic	178	178	100%
Number of Slices containing unrelated logic	0	178	0%
Total Number 4 input LUTs	309	1,536	20%
Number used as logic	229		
Number used for Dual Port RAMs	80		
Number of bonded IOBs	63	124	50%
IOB Flip Flops	40		
Number of GCLKs	2	8	25%
Total equivalent gate count for design	7,602		
Additional JTAG gate count for IOBs	3,024		

V. CONCLUSION

The data which can be send through the router is reached the destination with 9.375ns latency which obviously operates with high frequency. In future there is a chance to estimate the power consumption also.

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