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Review Paper on Composite Arithmetic Logic Unit using Reversible Gate

Archana Kumari[1], Prof. Suresh. S. Gawande[2]

M. Tech. Scholar, Department of Electronics and Communication, RKDF College of Engineering, Bhabha University, Bhopal, India[1]

Guide, Department of Electronics and Communication, RKDF College of Engineering, Bhabha University, Bhopal, India[2]

ABSTRACT: In today's world reversible arithmeticlogic unit is one of the very important parts of any system having many applications in computers, mobile, calculators etc. Reversible logic is useful in mechanical applications of nanotechnology, given that the friction generated by contacting corpuscles within a confined volume can be significantly reduced by eliminating sliding contact using mechanical reversible logic. We have reviewof reversible arithmetic logic unit based on reversible programmable gate. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. Reversible arithmetic logic unit are consisting of different gate.

KEYWORDS: Reversible Gates, Reversible Arithmetic Logic Unit, VHDL Implementation

I. INTRODUCTION

An Arithmetic and Logic Unit (ALU) is a combinational circuit that performs logic and arithmetic micro-operations on a pair of n-bit operands (ex. A[3:0] and B[3:0]). The operations performed by an ALU are controlled by a set of function-select inputs. In this lab you will design a 4-bit ALU with 3 function-select inputs: Mode M, Select S1 and S0 inputs. The mode input M selects between a Logic (M=0) and Arithmetic (M=1) operation. The functions performed by the ALU are specified in Table 1.1.

When doing arithmetic, we need to decide how to represent negative numbers. As is commonly done in digital systems, negative numbers are represented in twos complement [6]. This has a number of advantages over the sign and magnitude representation such as easy addition or subtraction of mixed positive and negative numbers. Also, the number zero has a unique representation in twos complement.

Table 1.1: Functions of ALU

M =0 Logic				
S1	S0	C0	Function	Operation
0	0	X	A_i. B_i	AND
0	1	X	A_i + B_i	OR
1	0	X	A_i \$ B_i	XOR
1	1	X	A_i !\$ B_i	XNOR
M =1 Logic				
S1	S0	C0	Function	Operation
0	0	0	A	Transfer A
0	0	1	A+1	Increment A by 1
0	1	0	A+B	Add A and B
0	1	1	A+B+1	Increment the sum of A and B by 1
1	0	0	A+B'	A plus one's complement of B
1	0	1	A-B	Sub-tractor B from A (i.e. B'+A+1)
1	1	0	A'+B	B plus one's complement of A
1	1	1	B-A	B minus A (or A' + B +1)

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There are different ways to design a bit-slice of the ALU. One method consists of writing the truth table for the one bit ALU. This table has 6 inputs (M, S1, S0, C_0, A_i and B_i) and two outputs F_i and C_{i+1}. This can be done but may be tedious when it has to be done by hand.

An alternative way is to split the ALU into two modules, one Logic and one Arithmetic module. Designing each module separately will be easier than designing a bit-slice as one unit. A possible block diagram of the ALU is shown in Figure 1. It consists of three modules: 2:1 MUX, a Logic unit and an Arithmetic unit.

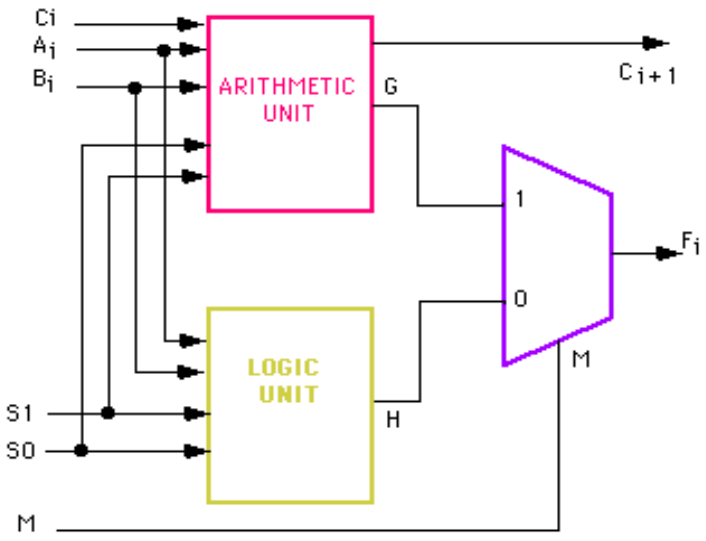

Figure 1: Block diagram of a bit-slice ALU

II. REVERSIBLE GATE

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gates available. It is most commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize the various Boolean functions in various logical architectures.

○ BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

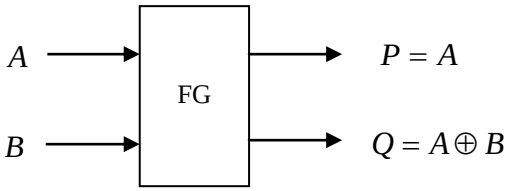

Figure 2: Feynman gate

In figure 3, the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

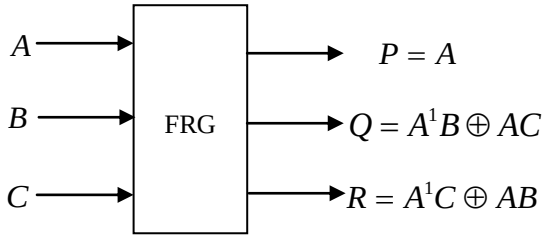

Figure 3: Fredkingate

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Figure 4 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

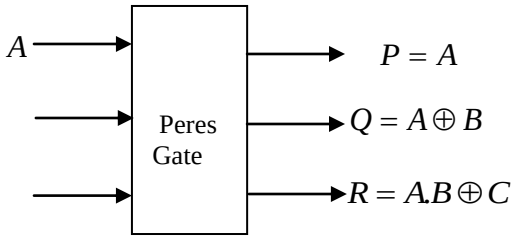

Figure 4: Peres gate

The HNG gate, presented in fig, produces the followinglogical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 5.

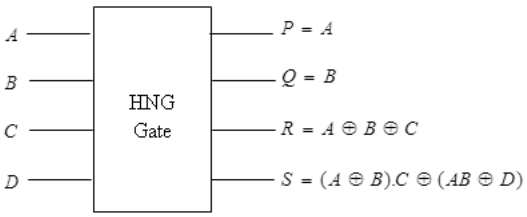

Figure 5: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or(PAOG) gate – is presented which produces outputs

$$P = A \quad (5)$$

$$Q = A \oplus B \quad (6)$$

$$R = AB \oplus C \quad (7)$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \quad (8)$$

Fig. 6 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

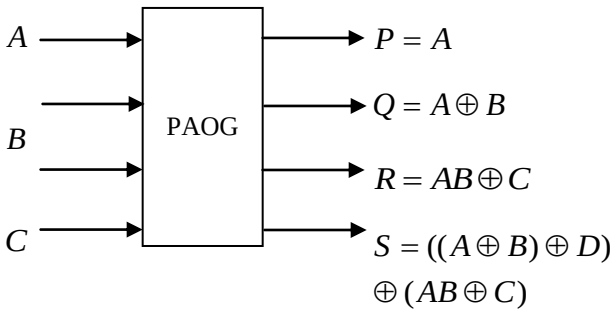

Figure 6: Block Diagram of the PAOG

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Several 4x4 gates have been described in the literature targeting low costand delay which may be implemented in a programmable manner to produce a high number of logical calculations. The DKG gate produces the followinglogical output calculations:

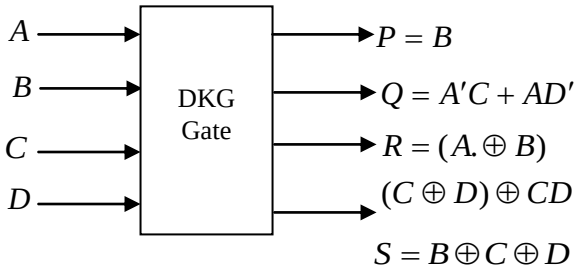

Figure 7: DKG Gate

$$P = B \quad (9)$$

$$Q = A'C + AD' \quad (10)$$

$$R = (A. \oplus B)(C \oplus D) \oplus CD \quad (11)$$

$$S = B \oplus C \oplus D \quad (12)$$

III. LITERATURE REVIEW

You-TunTeng et al. [1], the advanced encryption standard (AES)'s hardware implementation of the SubBytes and inverse SubBytes operations is the focus of this work. All building blocks in the S-box (and inverse S-box) of the SubBytes (and inverse SubBytes) transformation are optimized using composite field arithmetic (CFA) in response to this. To further improve area efficiency, a joint S-box and inverse S-box design is also proposed. In particular, there is a decrease in the area of the multiplier in the Galois composite field. In GF, the squaring and multiplication with constant are combined and optimized. In addition, GF multiplicative inversion is manually optimized. Additionally, the pre_processing and post_processing modules are used to combine and optimize the S-box and inverse S-box. A balanced and pipelined architecture is developed to boost throughput. Utilizing the proposed engineering, a throughput of 5.79 Gbps for the S-box can be accomplished on Virtex-6 XC6VLX240T and 10% better than the ordinary work. The proposed design still has the highest area efficiency and is approximately 30% better than conventional works made with the TSMC 90nm process, as shown by the ASIC implementation result.

S. Nagaraj et al. [2], due to extensive device scaling, semiconductor devices have seen significant improvements in performance and speed, while power dissipation has emerged as a major concern. Reversible computing, an emerging technology in the VLSI industry, could be the breakthrough because device scaling has reached its limit. Reversible logic circuits benefit greatly from this technology's lack of power dissipation. The ALU is a crucial part of the system and is used in applications like calculators, smartphones, and computers. The 32 Bit number-crunching rationale unit is planned utilizing Verilog Equipment Portrayal Language with tasks, for example, AND rationale, OR rationale, FullAdder utilizing The slightest bit ALU. In comparison to irreversible ALU, the reversible ALU is able to function quickly. The area, delay, and power dissipation of reversible logic gates are reduced. Consequently, reversible gates are utilized in VLSI design methods. The AND and OR gates for each one-bit ALU are replaced by an ALU made of reversible logic gates designed in this paper using the Toffoli, Fredkin, and Peres Gate. Modelsim Altera 6.3g is used for all logic, and Xilinx ISE 14.7 is used for the synthesis. The reversible logic-based ALU reduces area by 34% and delay by 48.91 percent.

Behrouz Safaiezadehet al. [3],due to its small size, fast, low latency, and low power consumption, quantum dot cellular automata (QCA) technology is regarded as one of the most suitable alternatives for addressing nanoscale digital circuit design issues caused by CMOS technology. The arithmetic logic unit (ALU), also known as the microprocessor's heart, is one of the most important components. Utilizing both standard reversible blocks and a brand-new reversible block, the BS1 Block, this paper presents a QCA-based reversible ALU unit. In the proposed scheme, logic and arithmetic operations are carried out by the proposed block. QCA Designer performs the simulations of the proposed design. The simulated results indicate that the proposed structure outperforms previous studies by 35%, 27%, and 30%, respectively, in terms of quantum cost, cell count, and occupied area.

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A. Reyhani-Masoleh et al. [4],One of the areas of cryptography that has received the most research is the way AES S-boxes are implemented. In this paper, we propose three new equipment plans for the AES S-confine that can serve the forward, opposite and consolidated information ways. The smallest AES S-box ever proposed in each of these categories is represented by each of these designs. We accomplish this by optimizing each block in each of the three proposed architectures and employing a novel tower field representation over conventional bases. In the CMOS STM 65 nm and NanGate 15 nm technologies, our complexity analysis and ASIC synthesis results demonstrate that our designs outperform their competitors in terms of area and power.

C. A. Murugan et al. [5],the successful cryptographic algorithm known as Advanced Encryption Standard (AES) can be used to ensure the safety of electronic data. It must continue to resist the majority of attacks. AES-128 encryption iterative architecture is designed in this work to use less hardware and use less space. By incorporating a reworked S-box structure into the AES algorithm, reduced area is achieved. The Vedic multiplier's inclusion in the Mix column transformation of the AES Encryption procedure also reduces hardware consumption. The Spartan 3, Virtex-4, and Virtex-5 Xilinx Spartan FPGA series were used to implement the proposed 128-bit encryption architecture. The optimization result shows that the proposed S-box method has a smaller area than other conventional works that have been done in the past.

S. Sawataishi et al. [6],for the most recent authenticated encryptions with associated data (AEADs), this brief presents a reliable and unified piece of hardware. Although some major AEADs, like the advanced encryption standard (AES), block chaining, and the XOR-Encryption-XOR (XEX) scheme, share a few fundamental components, each AEAD has its own mode of operation and/or sub-functions, making it difficult to efficiently integrate multiple AEADs into hardware. To perform a set of AEADs with minimal power and space requirements, the hardware that is proposed in this brief effectively combines the fundamental components. The given AEAD algorithm directs the adaptation of the proposed configurable datapath to a set of peripheral operations, such as block chaining and XEX. An experimental design that has been adapted to four AES-based AEADs is also used to demonstrate the veracity of the proposed hardware in this brief. As a result, we confirm that the proposed hardware can perform the four AEADs with comparable throughput and power consumption to the dedicated AEAD hardware while taking up significantly less space. In addition, we verified that the throughput and power consumption of the proposed hardware are superior to those of software implemented on a general-purpose processor.

Hari M. et al. [7], one of the foundations for new technologies like quantum, DNA, and optical computing is reversibility. It can be used to create ultra-low-power circuits that will aid in lowering global energy consumption. Additionally, testing these circuits to verify their functionality has been a major concern. A novel Arithmetic Logic Unit (ALU) design that can scale up to N bits is presented in this paper. To achieve circuit parity preserving, the design process makes use of the properties of Toffoli and Fredkin gates, demonstrating its inherent testability. The proposed architecture covers every single bit of a circuit's fault. For the purpose of determining operating costs in terms of the number of inputs, gate count, quantum cost, garbage outputs, and ancillary inputs, the design and implementation are carried out using a reversible circuit analyzer. A method for building the Arithmetic Logic Unit (ALU) using reversible logic gates as logic components is proposed in this paper. A reversible ALU with the same function as a traditional ALU is constructed by employing reversible logic gates rather than traditional logic gates like AND gates and OR gates. By logically reusing the logic information bits, the presented reversible ALU achieves the objective of lowering power consumption while simultaneously reducing the use and loss of information bits.

Parth Khatter et al. [8],Reversible rationale have gotten extraordinary consideration in the late years because of its capacity to decrease the power scattering which is the principal necessity in low power computerized plan. Advanced computing, low-power CMOS design, optical information processing, DNA computing, bioinformation, quantum computation, and nanotechnology are just a few of its many potential uses. Because bits of information are deleted during logic operations, conventional digital circuits lose a lot of energy. Therefore, power consumption can be greatly reduced if logic gates are constructed so that the information bits are not destroyed. In the event of a reversible computation, the information bits are not corrupted. Reversible gates have been developed as a result of this. ALU is a fundamental component of any computer system's central processing unit (CPU); The reversible arithmetic unit offers a significant power optimization. Numerous arithmetic operations can be carried out by applying the right control logic to one of the parallel adder's input variables.

IV. SIMULATION TOOL

Environment setup is the work environment or tools on which result analysis has been done for Xilinx 6.2i. Xilinx is the very strong software tool to analysis and simulate the complex circuits. There are so many versions for Xilinx software such as 6.1i, 9.1i, 10.2i, 13.1i and 14.2i. Generally two programming language are using VHDL and Verilog.

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VHDL is an acronym for VHSIC hardware description language (VHSIC is an acronym for very high speed integrated circuits). It is a hardware description language that can be used to model a digital system at many levels of absorption ranging from the algorithm level to the gate level [14]. VHDL allows users or programmers to use certain blocks which comprise of certain set of sequential statements. One such block is called a process. The (<=) operator, it is called the assignment operator and is used only for assigning values to signals. For variables the operator used is (:=).
Some chief terms that are used at the basic level are: - Libraries, Data types, Signals, Variables, Entity, and Architecture. Other important terms for the VHDL program such as process, component, function, procedures and state diagrams are used in programming.

Reversible Gate Parameter:-
Gate Count (GC): The number of gates used to realize reversible circuit
Garbage Outputs (GO): The number of unused outputs in a reversible logic. The inputs regenerated at the outputs are not garbage outputs.
Ancilla Inputs (AI): The number of input kept constant at either 0 or 1.
Delay : It corresponds to number of primitive quantum gates in the critical path of the circuit.
Quantum Cost:- Quantum cost is defined, as the number of basic quantum gates like controlled-NOT, Controlled V+, Controlled V and NOT gate.

V. CONCLUSION

This thesis mainly focuses on a novel design of reversible processor components. Internal architecture components i;e, ALU, CU, register files and PC having better performance with proposed circuitry as compared to previous counterparts. Also, registers and the memory for program and data fall into the category of improved performance with reduced delay. Memory access pattern, execution, and complexity of instruction are kept in mind improve the execution time by using Harvard architecture instead of von Neumann. Power dissipation is also less about negligible since an overall system is designed using reversible nature of logics. With all above demonstration, using proposed designs improve the performance of CPU and execution time will be faster.

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