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A Study of Interconnect Wires and their Parameters

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ABSTRACT: The paper aims to study the importance of interconnect wires in deep-submicron semiconductor technology , its impact on various parameters of VLSI circuits. The paper also discusses the introduction of interconnect wires , different types of interconnects used in various integrated circuits , interconnect material. How the resistance and inductance start including in the capacitance model of interconnect wires is also being explained. The paper also focuses on different wire model such as ideal wire , lumped model ,distributed RC model , transmission line model.

KEYWORDS*:* Interconnect , Lumped model ,Distributed model , Transmission line model.

I. INTRODUCTION

Throughout most of the past history of integrated circuits, on-chip interconnect wires were considered to be second class citizens that had only to be considered in special cases or when performing high-precision analysis. With the introduction of deep-submicron semiconductor technologies, this picture is undergoing rapid changes. The parasitics effects introduced by the wires display a scaling behaviour that differs from the active devices such as transistors, and tend to gain in importance as device dimensions are reduced and circuit speed is increased. In fact, they start to dominate some of the relevant metrics of digital integrated circuits such as speed, energy-consumption, and reliability. This situation is aggravated by the fact that improvements in technology make the production of ever larger die sizes economically feasible, which results in an increase in the average length of an interconnect wire and in the associated parasitic effects. A careful and in-depth analysis of the role and the behaviour of the interconnect wire in a semiconductor technology is therefore not only desirable, but even essential.

II. LITERATURE SURVEY ON INTERCONNECT

Interconnects in integrated circuits distribute clock and other signals and provide power or ground to the various integrated circuits. There are three types of interconnects: local, intermediate, and global. Local interconnects consist of very thin lines, connecting gates, and transistors within a functional block. They usually span only a few gates and occupy first and, sometimes, second metal layers. Intermediate interconnects are wider and taller than local interconnects in order to provide lower resistance; intermediate wiring provides clock and signal distribution within a functional block with typical lengths up to 3 to 4 mm. Global interconnects provide clock and signal distribution between the functional blocks and deliver power/ground to all functions. Global interconnects occupy the top one or two layers, and they are longer than 4 mm—as long as half the chip perimeter. It is critical that low-resistivity global interconnects be used as the bias voltage decreases and the total current consumption of the chip increases.

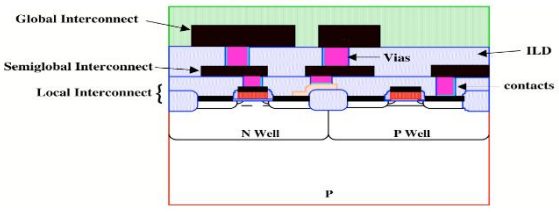

Fig. 1 Showing interconnects, contacts and vias, separated by dielectric layers.

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In the past, interconnect to be modeled as a single lumped capacitance that is added to the gate capacitance. But with increasing device densities per unit area, the cross-sectional area of interconnects has been reduced to provide more interconnect per unit area. Both the decreased cross-sectional area and the increased wire length have caused the global wire resistances to dramatically increase. The interconnect model now includes the resistance of the interconnect. Including resistance in the interconnect model dramatically changed the design and analysis of integrated circuits. Completely new problems and design techniques have emerged due to the transition from a capacitive to an *RC* model. At present, issues involved in a transition from an *RC* interconnect model to an *RLC* model which includes the inductance of the interconnect. This transition has the potential to change all aspects of the design and analysis of integrated circuits in analogy to the transition from a capacitive to an *RC* interconnect model.

III. IMPACT OF INTERCONNECTS ON VLSI DESIGN METHODOLOGY

In deep submicron technologies, degraded interconnect performance and high-speed operation reduce system noise immunity and timing budget which in turn result in faults in system operation. Due to the complexity of the system, chip design poses a difficult challenge to ensure that the resulting system is reliable. The increased difficulty in designing, verifying, and testing the chips has become a larger barrier to provide reliable chips within ever shorter time-to-market than that of providing the technology for manufacturing them. State-of-the-art VLSI design tools have included signal integrity and timing verifications at the post-layout stage. Parasitics of three-dimensional interconnects are extracted based on pre-characterized interconnect library and/or scalable interconnect parasitic models. However, the large number of circuit nodes makes it computationally expensive or infeasible.

A. Signal Integrity

The signal integrity problem is sketched in following *figure*. Very basically, a signal takes a certain finite amount of time (t_{tof}) to travel from the driver to the receiver. This time is referred to as the "time-of-flight". In an ideal case, the received signal has the same quality as its original one. However, in a real case, the received signal quality is degraded because of many reasons such as crosstalk, signal
dispersion, and glitches in power supply. As a result, the signal is not considered to be received, or latched in, until it has been stable for a finite amount of time, which is called the "setting time", t_{set}. The setting time varies with various signal qualities, which consequently contributes to timing skew and jitter. If the signal quality is too poor to be judged by the receiver, malfunction may occur.

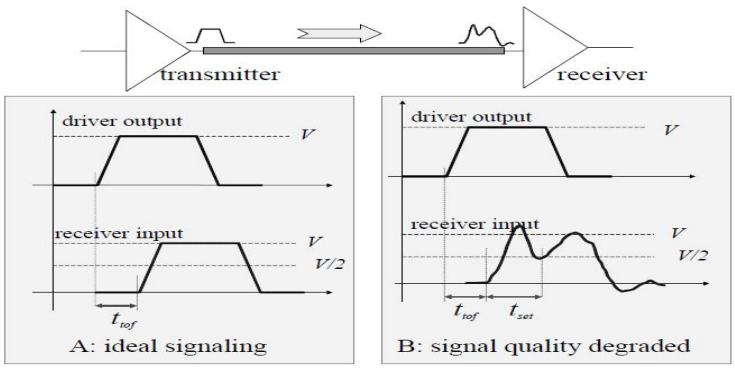

Fig.2 Signal integrity problem in VLSI circuits and systems

IV. INTERCONNECT MATERIAL

From a long time , aluminium has been used as an interconnect material . Copper can also be used as an interconnect material since it has various advantages over aluminium. The various advantages of copper are : (1) Copper has twice

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the thermal conductivity of aluminium and copper has ten to 100 times more resistance to electro migration failures than aluminium . Electro migration causes transport of the conductor material as a result of high current densities, which can ultimately lead to a void in the conductor .(2)The use of copper results in a power consumption reduction of 30% at a specific frequency. (3)By using copper rather than aluminium as interconnect material, the interconnect routing can be simplified, reducing the number of interconnect levels and resulting in fewer process steps. This translates to cost savings and higher device yield. Replacement of aluminium by copper was an enormous obstacle for semiconductor process engineers, since aluminium is deposited over the entire wafer surface and then patterned by reactive ion etching (RIE), and all efforts to apply RIE to copper failed. Copper cannot be patterned, and a new process had to be developed that could successfully fill a patterned dielectric.

V. INTERCONNECT PARAMETERS - RESISTANCE, INDUCTANCE AND CAPACITANCE

A. Capacitance

The capacitance of a wire is a function of its shape, its environment, its distance to the substrate, and the distance to surrounding wires. Rather than getting lost in complex equations and models, a designer typically will use an advanced extraction tool to get precise values of the interconnect capacitances of a completed layout. Most semiconductor manufacturers also provide empirical data for the various capacitance contributions, as measured from a number of test dies. Consider first a simple rectangular wire placed above the semiconductor substrate, as shown in Fig.3 If the width of the wire is substantially larger than the thickness of the insulating material, it may be assumed that the electrical-field lines are orthogonal to the capacitor plates, and that its capacitance can be modeled by the parallel-plate capacitor model. Under those circumstances, the total capacitance of the wire can be approximated as

$$C = (\varepsilon / t) * (WL)$$

Where *W* and *L* are respectively the width and length of the wire, and *t* and ε represent the thickness of the dielectric layer and its permittivity.

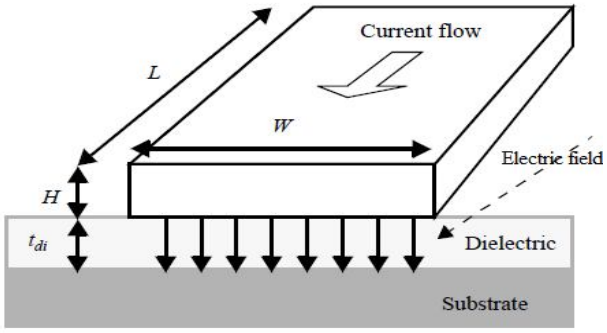

Fig.3 Parallel-plate capacitance model of interconnect wire.

In any chip, there are different capacitances present. They are as :a. Grounded capacitance : between a line and the substrate .b. Lateral capacitance : between metal lines on the same layer.c. Fringing capacitance : between various edges.d. Area capacitance : between two metal wires on different layers.

B. Resistance

The resistance of a wire is proportional to its length *L* and inversely proportional to itscross-section *A*. The resistance of a rectangular conductor in the style of Fig..3 can be expressed as

$$R = \rho L / A$$

where the constant ρ is the resistivity of the material (in Ω-m). Aluminum is the interconnect material most often used in integrated circuits because of its low cost and its compatibility with the standard integrated-circuit fabrication process. Unfortunately, it has a large resistivity compared to materials such as Copper. With ever-increasing performance targets, this is rapidly becoming a liability and top-of-the-line processes are now increasingly using

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Copper as the conductor of choice..Any interconnect wire is made up of a conducting material having some finite resistance . As in IC design technology , the interconnects are generally made in well defined pattern , so their resistance is defined in terms of sheet resistance which is technology dependent parameter .

C. Inductance

Integrated-circuit designers tend to dismiss inductance as something they heard about in their physics classes, but that has no impact on their field. This was definitely the case in the first decades of integrated digital circuit design. Yet with the adoption of low-resistive interconnect materials and the increase of switching frequencies to the super GHz range, inductance starts to play a role even on a chip. Consequences of on-chip inductance include ringing and overshoot effects, reflections of signals due to impedance mismatch, inductive coupling between lines, and switching noise due to *Ldi*/*dt* voltage drops. The inductance of a section of a circuit can always be evaluated with the aid of its definition, which states that a changing current passing through an inductor generates a voltage drop

$\Delta v = L \, di / dt$

It is possible to compute the inductance a wire directly from its geometry and its environment. A simpler approach relies on the fact that the capacitance *c* and the inductance *l* (per unit length) of a wire are related by the following expression

$$CL = \varepsilon\mu$$

with ε and μ respectively the permittivity and permeability of the surrounding dielectric.

VI. ELECTRICAL WIRE MODELS

The parasitic elements have an impact on the electrical behaviour of the circuit and influence its delay, power dissipation, and reliability. To study these effects requires the introduction of electrical models that estimate and approximate the real behaviour of the wire as a function of its parameters.

A. Ideal wire

In schematics, wires occur as simple lines with no attached parameters or parasitics. These wires have no impact on the electrical behaviour of the circuit. A voltage change at one end of the wire propagates immediately to its other ends, even if those are some distance away. Hence, it may be assumed that the same voltage is present at every segment of the wire at the every point in time, and that the whole wire is an *equipotential region*. While this *ideal-wire model* is simplistic, it has its value, especially in the early phases of the design process when the designer wants to concentrate on the properties and the behaviour of the transistors that are being connected. Also, when studying small circuit components such as gates, the wires tend to be very short and their parasitics ignorable. Taking these into account would just make the analysis unnecessarily complex. More often though, wire parasitics play a role and more complex models should be considered.

B. The lumped model

The circuit parasitics of a wire are distributed along its length and are not lumped into a single position. Yet, when only a single parasitic component is dominant, when the interaction between the components is small, or when looking at only one aspect of the circuit behaviour, it is often useful to lump the different fractions into a single circuit element. The advantage of this approach is that the effects of the parasitic then can be described by an ordinary differential equation. As long as the resistive component of the wire is small and the switching frequencies are in the low to medium range, it is meaningful to consider only the capacitive component of the wire, and to lump the distributed capacitance into a single capacitor as shown in Figure.4 Observe that in this model the wire still represents an equipotential region, and that the wire itself does not introduce any delay. The only impact on performance is introduced by the loading effect of the capacitor on the driving gate. This capacitive lumped model is simple, yet effective, and is the model of choice for the analysis of most interconnect wires in digital integrated circuits.

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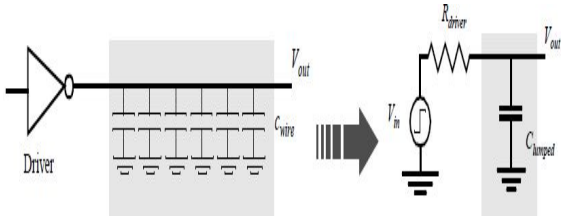

Fig. 4 The lumped model –effective for modelling shortinterconnects

C. The distributed RC line model

The lumped *RC* model is a pessimisticmodel for a resistive-capacitive wire, and that a distributed *rc* model is more appropriate. As before, *L* represents the total length of the wire, while *r* and *c* stand for the resistance and capacitance per unit length. A schematic representation of the distributed *rc* line is given in Fig.5

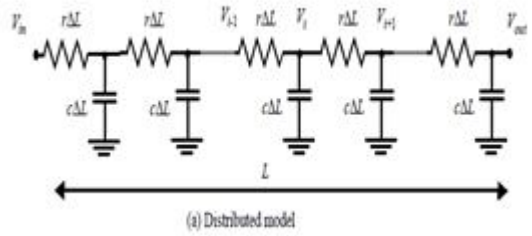

Fig. 5 Distributed RC model for the wires

The well known diffusion equations for this model

$$rc\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}$$

give us solution in time domain.

D. Transmission line model

Similar to the resistance and capacitance of an interconnect line, the inductance is distributed over the wire. A distributed *rlc* model of a wire, known as the transmission line model, becomes the most accurate approximation of the actual behaviour. The transmission line has the prime property that a signal propagates over the interconnection medium as a *wave*. This is in contrast to the distributed *rc* model, where the signal *diffuses* from the source to the destination governed by the diffusion equation, Eq. In the wave mode, a signal propagates by alternatively transferring energy from the electric to the magnetic fields, or equivalently from the capacitive to the inductive modes.

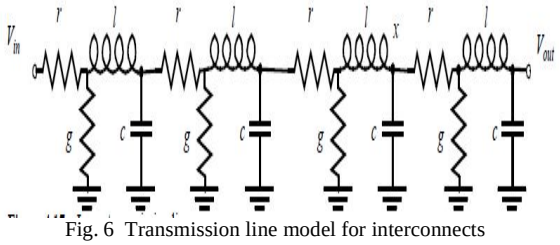

Fig. 6 Transmission line model for interconnects

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The wave propagation equation

$$\frac{\partial^2 v}{\partial x^2} = rc\frac{\partial v}{\partial t} + lc\frac{\partial^2 v}{\partial t^2}$$

along with boundary conditions provides us the final results depending upon whether the line is treated as lossless or lossy

VII. CONCLUSION

Concern about the performance of wires in scaled technologies and complexity in interconnect design have led to research exploring new interconnect-centric design methodologies. Despite the fact that local interconnects scale in performance, future design tools will still need more sophisticated capability in dealing with these wires for signal and power integrity as well as timing closure. Global interconnects and some intermediate interconnects that do not scale in length present serious problems to designers. The key focus of interconnect-centric design will be these global wires. A number of point tools and models for interconnect analysis are needed at different design stages, for global communication and interconnect design, for logic design and circuit design, as well as for physical design. Therefore, a better understand of the magnitude of the wire problem and interconnect constraints, better understanding of physical mechanisms of signal integrity and various design techniques at different design levels, are essential to the success of interconnect design in the DSM regime.

REFERENCES

[1] S. S. Sapatnekar, "RC interconnect optimization under the Elmore delay model," *Proc. IEEE/ACM Design Automation Conf.*, pp. 387–391, June 1994.
[2] D. A. Priore, "Inductance on Silicon for Sub-Micron CMOS VLSI," *Proceedings of the IEEE Symposium onVLSI Circuits*, pp. 17-18, May 1993.
[3] D. B. Jarvis, "The Effects of Interconnections on High-Speed Logic Circuits," *IEEE Transactions on ElectronicComputers*, Vol. EC-10, No. 4, pp. 476 - 487, October 1963.
[4] M. P. May, A. Taflove, and J. Baron, "FD-TD Modeling of Digital Signal Propagation in 3-D Circuits with Passive and Active Loads," *IEEE Transactions on*Microwave Theory and Techniques, Vol. MTT-42, No. 8 , pp. 1514 - 1523, August 1994
[5] T. Sakurai, "Approximation of Wiring Delay in MOSFET LSI," *IEEE Journal of Solid-State Circuits*, Vol. SC-18, No. 4, pp. 418 - 426, August 1983.
[6] G. Y. Yacoub, H. Pham, M. Ma, and E. G. Friedman, "T System for Critical Path Analysis Based on Back Annotation and Distributed Interconnect Impedance Models," *Microelectronic Journal*, Vol. 18, No. 3, pp. 21 - 30, June 1988.
[7] J. Torres, "Advanced Copper Interconnections for Silicon CMOS Technologies," *Applied Surface Science*, Vol. 91, No. 1, pp. 112 - 123, October 1995.
[8] K. K. Likharev and V. K. Semenov, "RSFQ Logic/Memory Family: A New Josephson-Junction Technology for Sub-Terahertz-Clock Frequency Digital System," *IEEE Transactions on Applied Superconductivity*, Vol. AS-1, No. 1, pp. 3 - 28, March1991.
[9] T. Sakurai and A. R. Newton "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas," *IEEE Journal of Solid-State Circuits*, Vol. SC-25, No. 2, pp. 584 - 593, April 1990.
[10] L. N. Dworsky, *Modern Transmission Line Theory and Applications*, John Wiley & Sons, Inc., New York, 1979.
[11] Y. Eo and W. R. Eisenstadt, "High-Speed VLSI Interconnect Modeling Based on S-Parameter Measurement," *IEEE Transactions on Components,Hybrids, and Manufacturing Technology*, Vol. CHMT-16, No. 5, pp. 555 - 562, August 1993.
[12] A. Deutsch, *et al.*, "High-Speed Signal Propagation on lossy transmission lines," *IBM Journal of Research andDevelopment*, Vol. 34, No. 4, pp. 601 - 615, July 1990.