ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 1, Issue 7, September 2013

Compact Model for Tunnel Field Effect Transistors

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ABSTRACT: Though silicon tunnel field effect transistor (TFET) has attracted attention for 60mV/decsubthreshold swing and very small OFF current (IOFF), its practical applications is questionable due to low ON current (I_{ON}) and complicated fabrication process steps. In this paper, using Landauerapproachacompact model for tunnel field-effect transistors (TFETs) has developed. The important transistor parameters, such as threshold voltage V_{th}, charge in the channel Q ,gate capacitance C_G, drain current I_D , subthreshold swing S, transconductanceg_m, have modelled. The low subthreshold swing values ie.,less than 60mV/dec observed in the modelshows a good match with the TCAD results. Modelling is carried out using TCAD simulation for different TFET structures ie.30-nm InPnTFET and 40-nm GenTFET.

KEYWORDS: Band-to-Band (BTB) Tunneling, compact model, metal-oxide-semicon0ductors, TCAD, tunnel field-effect transistor (TFET).

I. INTRODUCTION

As the transistor has been scaling, the power consumption in modern microelectronics circuits have been divided into the dynamic power consumption and static power consumption. With scaling, the static power consumption is becoming non-negligible.to reduce the power dissipation, supply voltage (V_{DD}) needs to be aggressively scaled which decreases both the static and dynamic components of power. The static power reduces as the OFF-state leakage current (I_{OFF}) decreases for lower V_{DD} and the dynamic power reduces as the rail-to-rail swing decreases. However, the ON current (I_{ON}) decreases with reduction in V_{DD} due to the non –scalability of the device threshold voltage and the transistor finite subthreshold slope of 60mV/dec(SS). This decreases the speed of the device and circuits. Therefore, in order to satisfy the speed criteria, I_{ON} has to be maintained at the required value which is achieved by lowering the threshold voltage of the device. This increases the static power consumption.For a low V_{DD}, the static power dissipation become dominantwhen compared to the dynamic power.

So the optimization between the speed and power dissipation of the device becomes a serious problem.

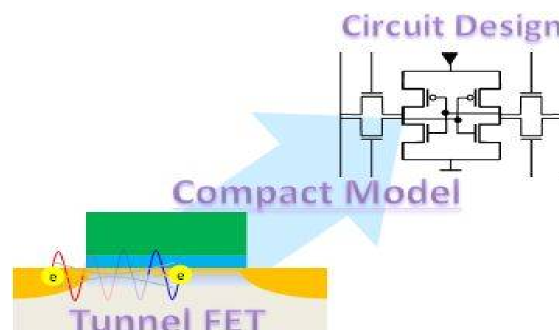

Fig.1 :Flow to the design of a large-scale integrated circuit using low-voltage tunnel FETs.A circuit can be designed by using the device-operation model to represent the characteristics of developed devices.

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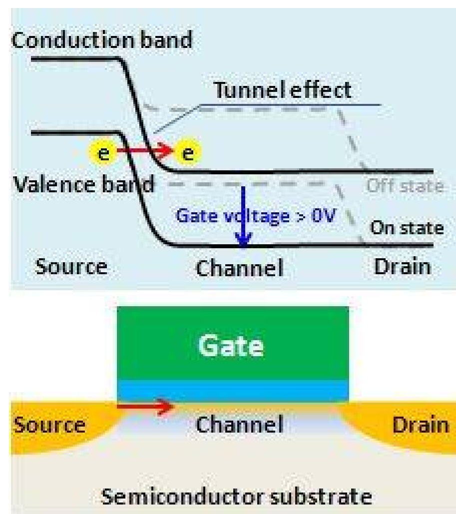

Fig.2. Structure and device principle of the tunnel FET The dotted gray lines indicate the off state.

As a result, several alternative device structures such as tunnel field-effect transistors (TFETs), impact ionization MOSFETs, MOSFETs with a ferroelectric insulator as a gate oxide, green transistors, and sandwich tunnel barrier FETs have been proposed in the literature. The TFET is a promising device to replace the traditional MOSFET for low standby power (LSTP) applications. While lowON-state current is a significant problem facing these devices, the lack of a good compact model is hampering the circuit simulation activity involving the TFETs, which is the focus of this paper. The modelling has been carried out for a standard silicon-on-insulator (SOI) TFET device structure, which resembles that of a gated p-i-n diode. The Landauer approach has been incorporated to evaluate the transistor current.

II.DEVICE STRUCTURE AND WORKING PRINCIPLE

In the off state, no empty states are available in the channel for tunnelling from the source, so the off current is very low. Decreasing V_G moves the valence band energy (E_V) of the channel above the conduction band energy (E_C) of the source so that interband tunnelling can occur. This switches the device to the on state, in which electrons in the energy window, $\Delta\Phi$ (green shading), can tunnel from the source conduction band into the channel valence band. Electrons in the tail of the Fermi distribution cannot tunnel because no empty states are available in the channel at their energy (dotted black line), so a slope of less than 60 mV decade^{-1} can be achieved. This is indicated in the schematic transfer characteristics shown in Fig.3.**c**. In contrast to a conventional MOSFET, a TFET has a slope that is not linear on a logarithmic scale, which can be explained by the complex dependency of the tunnel current on the transmission probability through the barrier, as well as on the number of available states determined by the source and channel Fermi functions. The BTBT can be approximated by the triangular potential barrier indicated in grey. Because the tunnel current depends on the transmission probability through the barrier, as well as on the number of available states determined by the source and channel Fermi functions, the resultant slope is not linear on a logarithmic scale, which it is for a conventional MOSFET. λ, screening tunnelling length. a.u., arbitrary units; E_F, Fermi energy.

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III.COMPACT MODELLING

Compact models of circuit elements are models that are sufficiently simple to be incorporated in circuit simulators and are sufficiently accurate to make the outcome of the simulators useful to circuit designers. The conflicting objectives of model simplicity and accuracy make thecompact modelling field and exciting and challenging research area for device physicists, modelling engineers and circuit.
Continued down scaling of semiconductor devices has made it necessary to incorporate new physical phenomena, while extended application have lead to the inclusion of the secondary and ternary effects

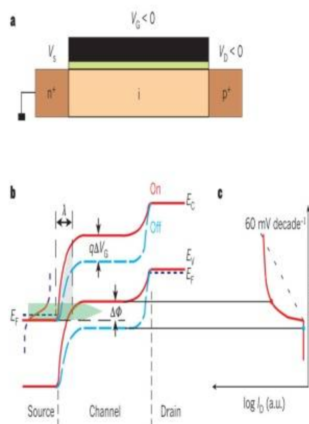

Fig.3.a, Schematic cross-section of p-type TFET with applied source (V_S), gate (V_G) and drain (V_D) voltages. **b**, Schematic energy band profile for the off state (dashed blue lines) and the on state (red lines) in a p-type TFET.

in order to achieve the required.model accuracy. In addition several rigid requirements in terms of model continuity and qualitative behaviour ("benchmarks") have been imposed over the years. At the same time, the increased size of the integrated circuits, which can now be subjected to the full SPICE analysis, disallowed proportional increase in the model execution dramaticallyincreased accuracy and model sophistication are accomplished without prohibitive decrease in the computational efficiency.

The developed compact model for tunnel FETs can calculate the tunnel current generated in the FET from the terminal voltages of the source, drain, and gate. First, the model predicts the electric field distribution at the location in the tunnel FET where the tunnel current is generated .The tunnel distance can be obtained from the electric field distribution, allowing estimation of the amount of the generated tunnel current. Because the model can be used to predict the electrical characteristics of individual devices, a circuit simulator with the model is described in Verilog –A language and therefore can be incorporated into various circuit simulators. Because a circuit simulation deals with multiple devices simultaneously, the model is expressed by analytical equations that can be calculated instantly. The validity of this model was evaluated by comparison with numerical simulations, including a numerical analysis method that divides a device structure into a group of small regions and solves equations (the finite element method).

An expression for the band - to- band tunnelling current in Tunnel FETs can be found by using the WKB approximation rule and taking the tunnel barrier as a triangularly shaped potential barrier.

T (E) using Wentzel, Kramer's, and Brillouin (WKB) approximation can be expressed as

$$T(E) = e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}$$

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$$\lambda = \sqrt{\frac{2\Phi_S}{qN_S}\left(\Phi_{bi} - \Delta\Phi\right) - \frac{2kT}{q}}$$

It has been shown that TFET exhibit subthreshold swing smaller than 60mV/dec. Moreover, it has been shown that TFETs has been scaled down to 20nm in channel length without much degradation of the subthreshold slope, I_{ON} and I_{OFF} .However TFETs have lower ON currents and higher threshold voltages compared with MOSFETs .The lack of a good compact model is hampering the circuit simulation activity involving the TFETs.

The important parameters to be considered are the following: average tunneling thickness λ; parameter f takes care of the errorintroduced with this formulation. The value of fvalue can be adjusted for different gate and drain biases and can be expressed as

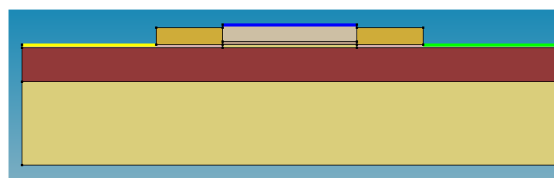
$$f=a_0+b_0+a_1V_{gs}+b_1V_{ds}$$

Where a_0,a_1, and b_1 are constants. There are two types of tunneling processing, viz..,

1) Trap -assisted Tunnelling
2) Band-to- band Tunnelling

A .THRESHOLD VOLTAGE

The threshold voltage, commonly abbreviated as $\mathbf{V_{th}}$, of a field-effect transistor (FET) is the value of the gate–source voltage when the conducting channel just begins to connect the source and drain contacts of the transistor, allowing significant current. In wide planar transistors the threshold voltage is essentially independent of the drain–source voltage .When the applied gate voltage is equal to the threshold voltage of MOS (V_{th}^{MOS}), there is an inversion in the channel.



.Fig.4. Structure of 30nm InPNTFET generated using TCAD SENTAURUS

The threshold voltage of MOS can be written as

$$V_{th} = \Phi_{ms} - \frac{Q_{ox}}{C_{ox}} + \sqrt{\frac{4qN_i\varepsilon_S\Phi_B}{C_{ox}}} + 2\Phi_B$$

WhenV_{GS}=V_{th}^{MOS},the device is in OFF-state . If we further increase the gate voltage beyond the threshold voltage of MOS, there is a downward shift in the bands of channel

The threshold voltage of nTFET of can be written as

$$V_{th} = \Phi_{ms} - \frac{Q_{ox}}{C_{ox}} + \sqrt{\frac{4qN_i\varepsilon_S\Phi_B}{C_{ox}}} + 2\Phi_B+\frac{E_g}{2q}$$

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B. CHARGE IN THE CHANNEL

The charge in the channel for superthreshold ($V_{GS} > V_{th}$) and subthreshold ($V_{GS} < V_{th}$) regions using tunneling current equations .The charge in the channel for a superthreshold region can be written as

$$Q = -\frac{I_{tun}\lambda}{v}$$

$$Q = q^2\lambda\frac{m^*}{\pi h^2}wfv_t\, e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}\ln\frac{1+e^{\frac{(V_{GS}-V_{th})}{V_t}}}{2}$$

.

Charge in the channel for the subthreshold region can be written as

$$Q = -\frac{I_{tun}\lambda}{v} \qquad Q = q^2 p\lambda\frac{m^*}{\pi h^2}wfv_t\, e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}\ln\frac{2}{1+e^{\frac{(V_{GS}-V_{th})}{V_t}}}$$

C. GATE CAPACITANCE:

The gate capacitance is a series combination of oxide capacitance Cox and channel capacitance C_C, where C_C is due to a variation of charges in the channel with gate voltage. The gate capacitance for both superthreshold and subthresholdregions can be written as

$$C_G = \left|\frac{dQ_m}{dV_{GS}}\right| = \left|\frac{dQ_{ox}}{dV_{GS}} + \frac{dQ}{dV_{GS}}\right| = \left|\frac{dQ}{dV_{GS}}\right|$$

Differentiating with respect to V_{GS}gives the gate capacitance for superthreshold region and is written as

$$C_G = -q^2\lambda\frac{m^*}{\pi h^2}wfv_t\, e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}\frac{e^{\frac{(V_{GS}-V_{th})}{V_t}}}{V_t\left(1+e^{\frac{(V_{GS}-V_{th})}{V_t}}\right)} + \beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)^2}\times \quad e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}\ln\frac{1+e^{\frac{(V_{GS}-V_{th})}{V_t}}}{2}$$

Differentiating with respect to V_{GS} gives the gate capacitance for subthreshold region and it is written as

$$C_G = q^2P\lambda\frac{m^*}{\pi h^2}wfv_t\, e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}\frac{e^{\frac{(V_{GS}-V_{th})}{V_t}}}{V_t\left(1+e^{\frac{(V_{GS}-V_{th})}{V_t}}\right)} + \beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)^2}\times$$

$$e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}\ln\frac{1+e^{\frac{(V_{GS}-V_{th})}{V_t}}}{2} + q^2P\lambda\frac{m^*}{\pi h^2}wf\frac{V_t}{V_{teq}}\times \quad e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}\ln\frac{1+e^{\frac{(V_{GS}-V_{th})}{V_t}}}{2}$$

D. DRAIN THRESHOLD VOLTAGE

The TFET has a new region calleddrain threshold region which is observed before the linear region.

Drain threshold voltage is the value of drain voltage below which the drain current is dominated by reverse-bias p-n junction current at the drain–channel junction.. The drain current for the sub drain threshold region($0 \le V_{DS} \le V_{Dth}$) can be written as

$$I_{DS} = Et_{epi}\frac{qn_i{}^2}{N_i}\sqrt{\frac{D_n}{\tau_e}}\left(1 - e^{\frac{V_{DS}}{V_t}}\right) + q\frac{n_i}{\tau_e}\sqrt{\frac{2\varepsilon_{si}}{q}\left(\frac{1}{N_i}+\frac{1}{N_D}\right)(V_{bi}+V_{DS})}$$

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E. DRAIN CURRENT

The drain current has been derived for linear, saturation and subthreshold regions.

For linear region I_{DS} is given by

$$I_{DS}=2\frac{\mu_{eff}}{\left(1+\frac{V_{DS}}{L\xi_c}\right)}q^2\lambda\frac{m^*}{L^2\pi h^2}fW\,e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}\times\left((V_{GS}-V_{th}-V_t\ln 2)(V_{DS}-V_{Dth})-\frac{(V_{DS}-V_{Dth})^2}{2}\right)$$

For saturation region ($V_{Dsat}\leq V_{DS}\leq V_{DD}$ and ($V_{GS}\geq V_{th}$), the I_{DS} is given by

$$I_{Dsat}=\mu q^2\lambda\frac{m^*}{L^2\pi h^2}fW\,e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}\times(V_{GS}-V_{th}-V_t\ln 2)^2$$

For subthreshold conduction ($V_{GS}\leq V_{th}$), the I_{DS} is given by

$$I_{DS}=q^2\lambda\frac{m^*}{L^2\pi h^2}D_nWfV_t\ln 2\,e^{\frac{V_{GS}-V_{th}}{V_{teq}}}\times\quad e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}$$

F. SUBTHRESHOLD SWING

In the subthreshold region the drain current behaviour – though being controlled by the gate terminal – is similar to the exponentially increasing current of a forward biased diode. Therefore a plot of logarithmic drain current versus gate voltage with drain, source, and bulk voltages fixed will exhibit approximately linear behaviour in this MOSFET operating regime. Its slope is the subthreshold slopeand it is given by

$$S=\left(\frac{d(\log I_{DS}}{dV_{GS}}\right)^{-1}=\frac{\ln 10}{\frac{1}{V_{teq}}+\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)^2}}$$

S_{avg} is a strong function of the parameter "n" (a positive real number) therefore at room temperature

$$S_{avg}<\frac{n}{(n+1)}V_t\ln 10\leq V_t\ln 10=60\frac{mV}{dec}$$

G. TRANSCONDUCTANCE

The transconductance$gm$and output conductance $g_{DS}$are obtained by differentiating drain current with respect to gate voltage and drain current.

$$g_m{}^{sat}=\mu q^2\lambda\frac{m^*}{L^2\pi h^2}fW\,e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}\times(V_{GS}-V_{th}-V_t\ln 2)^2\times\left(2+(V_{GS}-V_{th}-V_t\ln 2)\frac{\beta\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)^2}\right)$$

Similarly, in the subthreshold region, it can be written as

$$g_m{}^{sub}=I_s e^{\left(\frac{V_{GS}-V_{offset}-V_{th}}{V_{teq}}-\beta\frac{\lambda}{V_{GS}-V_{th}{}^{MOS}-\Phi_S}\right)}\times\left(\frac{1}{V_{teq}}+\frac{\beta\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)^2}\right)$$

$$g_{DS}=\frac{dI_D}{dV_{DS}}$$

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$$g_{DS}=2\mu q^2\lambda\frac{m^*}{L^2\pi h^2}fW\, e^{\left(-\beta\frac{\lambda}{(V_{GS}-V_{th}{}^{MOS}+\Phi_S)}\right)}\times((V_{GS}-V_{th}-V_t\ln2)-V_{DS})$$

IV.RESULTS AND DISCUSSION

Instead of using Germanium(Ge),Indium Phosphide(InP) can be used for boosting the I_{ON} current. Indium Phosphide (InP) is a member of the III-V family of semiconductors. III-V materials are binary crystals with one element from the metallic group 3 of the periodic table, and one from the non-metallic group 5. We have taken a standard TFET structure with abrupt source–channel and drain–channel junctions, as shown in Fig. 4.

The fig.5.shows the modeled drain current as a function of gate voltage at V_{DS}=1.0V for 30nm InP NTFET and 40 nm Ge NTFET. In proposed 30 nm InPNTFET,drain current is improved ie.I_{DS}=0.58mA when compared to 40 nm Ge NTFET(I_{DS}=0.284mA).The result shows that instead of using III group semiconductor material III-IV semiconductor materials provides the better output current. III-IV group material having more valence electrons when compared to using III group materials alone which

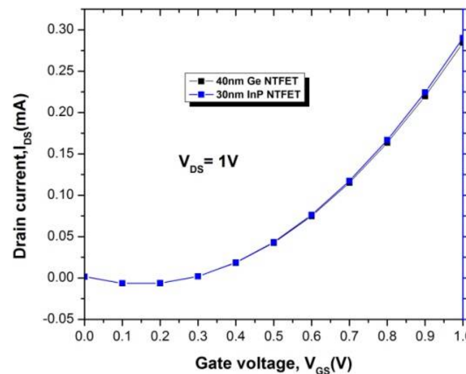

Fig.5 Modeled drain current as a function of gate voltage at V_{DS}=1.0V for 30nm InP NTFET and 40 nm Ge NTFET.

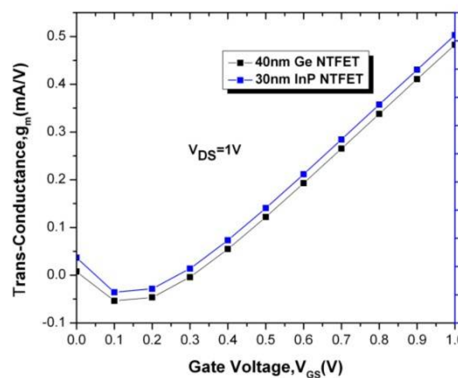

Fig.6. Modeled Trans-conductance as a function of gate voltage at V_{DS}=1.0 V for 30 nm InP NTFET and 40 nm GeNTFET **.**

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exhibits better conduction. So InP NTFET provides more current than Ge NTFET. Reduction of gate length provides the low leakage current and it will increase the frequency response and transconductance.

The figure 6 shows the Modeled Trans-conductance as a function of gate voltage at V_{DS}=1.0 V for 30 nm InP NTFET and 40 nm Ge NTFET **.**In proposed 30 nm InP, trans –conductance, $g_m$is improved i.e., g_m=0.48mA when compared with 40 nm Ge NTFET (g_m=0.21mA).The trans-conductance ,g_m is obtained by differentiating drain current with respect to gate voltage. So when drain current increases, g_m also increases.

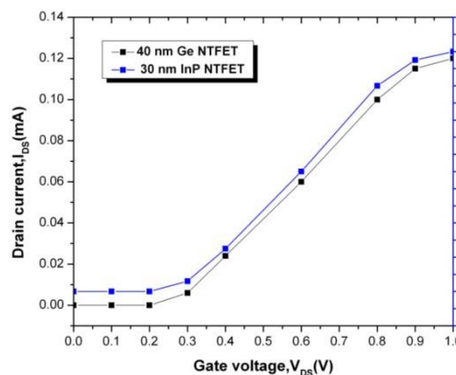

Fig.7. Modeled drain current as a function of drain voltage at V_{GS}=1.0 V for 30 nm InP NTFET.

The figure 7 shows the Modeled drain current as a function of drain voltage at V_{GS}=1.0 V for 30 nm InP NTFET. The drain current is varied according to the drain voltage , V_{DS} making the V_{GS} constant. As drain current increases, propagation delay decreases, mobility and oxide capacitance increases. Reduction of fall time is important because the tunnelling phenomena at the source channel interface are heavily depending on the drain. For 30 nm InP NTFET the drain current obtained is0.12mA and for 40 nm Ge NTFET is 0.11 mA.

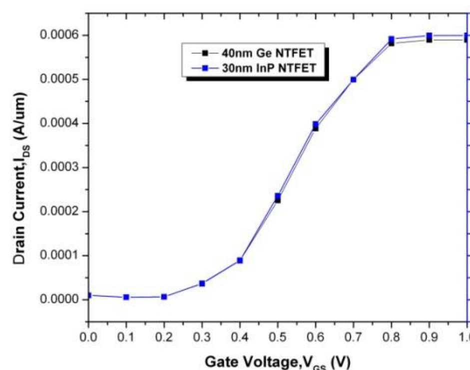

Fig.8. TCAD simulated drain current as a function of gate voltage at V_{DS}=1.0V for 30 nm InP NTFET and 40 nm Ge NTFET.

The figure 8 shows the TCAD simulated drain current as a function of gate voltage at V_{DS}=1.0V for 30 nm InP NTFET and 40 nm Ge NTFET. The simulation result also shows that when using 30 nm InP NTFET the drain current is improved as a function of gate voltage with 0.6 mA when compared to 40 nm Ge NTFET of 0.58 mA. The drain

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current in TFET is due to the tunneling of valence-band electrons from the source to the conduction band of the i-region. InP have more valence electrons compared to Ge.

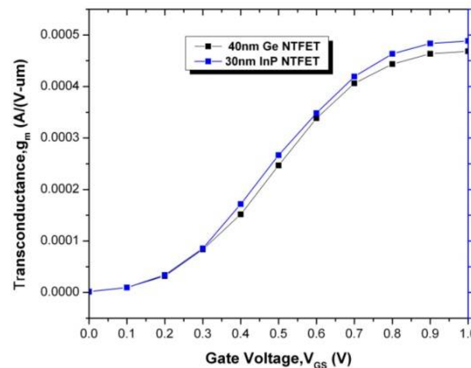

Fig.9.TCAD simulated trans-conductance as a function of gate voltage at V_{DS}=1.0 V for30 nm InP NTFET and 30 nm Ge NTFET

The figure 9 shows the TCAD simulated trans-conductance as a function of gate voltage at V_{DS}=1.0 V for 30 nm InP NTFET and 30 nm Ge NTFET. In proposed system g_m is improved for InPNTFET(g_m=4.88mA) when compared to Ge NTFET($g_{m=}$4.68mA).As drain current increases, g_m also increases.Reduction of gate length provides the low leakage current and it will increase the frequency response and transconductance.

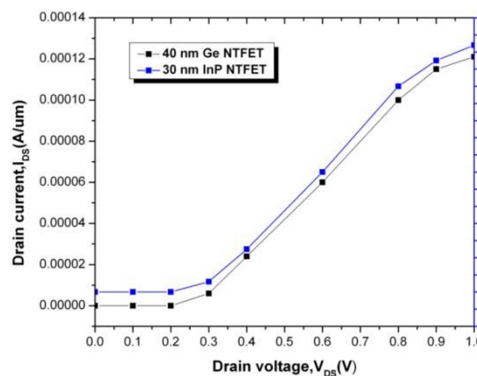

Fig.10. TCAD simulated drain current as a function of drain voltage at V_{GS} =1.0V for 30 nm InP NTFET and 40nm Ge NTFET.

The figure 10 shows the TCAD simulated drain current as a function of drain voltage at V_{GS} =1.0V for 30 nm InP NTFET and 40nm Ge NTFET. Increase in V_{DS}, from 0 to 1V bands are flat in the channel and in the n^+ doped drain region. A large band bending at the source channel interface. The slope of the band bending increases with drain biases. At V_{GS} =1V ,there is a sharp band bending at the source channel interface which enables the valence band electrons to tunnel into the conduction band. Drain current obtained for 30nm InP NTFET is 0.124mA and 40 nm Ge NTFET is 0.115 mA.

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V.CONCLUSION

While low ON-state current is a significant problem facing these devices, the lack of a good compact model is hampering the circuit simulation activity involving the TFET. We have developed a physics-based analytical model for TFET circuit applications using the Landauer approach. The compact model predictions shows that when using 30 nm InP NTFET I_{ON} current is improved compared with 40 nm Ge NTFET.

When using III-IV group semiconductor materials, the current can be improved because of its valence band electrons which facilitate strongconduction. InP facilitates the operation of very high speed electronics. InP has a very strong potential for creating integrated devices. Reduction of gate length provides the low leakage current and it will increase the frequency response and trans-conductance, g_m.The important electrical parameters Drain current, I_{DS}, Trans -conductance, $g_m$and output conductance, g_{ds} has improved when using Indium Phosphide.

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