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Implementation of PRPG with Low-Power BIST

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ABSTRACT: This project describes a low-power (LP) programmable generator capable of producing pseudorandom test patterns with desired toggling levels and enhanced fault coverage gradient compared with the best-to-date built-in self-test (BIST)- based pseudorandom test pattern generators. It is comprised of a linear finite state machine (a linear feedback shift register or a ring generator) driving an appropriate phase shifter, and it comes with a number of features allowing this device to produce binary sequences with preselected toggling (PRESTO) activity. We introduce a method to automatically select several controls of the generator offering easy and precise tuning. The same technique is subsequently employed to deterministically guide the generator toward test sequences with improved fault-coverage-to-pattern-count ratios. Furthermore, this proposes an LP test compression method that allows shaping the test power envelope in a fully predictable, accurate, and flexible fashion by adapting the PRESTO-based logic BIST (LBIST) infrastructure. The proposed architecture is extended in such that the patterns generated from PRPG is gone through CUT and then to TRA to perform ATE.

I. INTRODUCTION

The test pattern generator produces test vectors that are applied to the tested circuit during pseudo-random testing of combinational circuits. The nature of the generator thus directly influences the fault coverage achieved. The influence of the type of pseudo-random pattern generator on stuck-at fault coverage. Linear feedback shift registers (LFSRs) are mostly used as test pattern generators, and the generating polynomial is primitive to ensure the maximum period.

We have shown that it is not necessary to use primitive polynomials, and moreover that their using is even undesirable in most cases. This fact is documented by statistical graphs. The necessity of the proper choice of a generating polynomial and an LFSR seed is shown here, by designing a mixed-mode BIST for the ISCAS benchmarks. As the complexity of VLSI circuits constantly increases, there is a need of a built-in self-test (BIST) to be used. Built-in self-test enables the chip to test itself and to evaluate the circuit's response. Thus, the very complex and expensive external ATE (Automatic Test Equipment) may be. The main challenging areas in VLSI are performance, cost, and power dissipation.

Due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation VLSI circuits.

The power dissipation during test mode is 200% P more than in normal mode. Hence it is important aspect to optimize power during testing. Power optimization is one of the main challenges.

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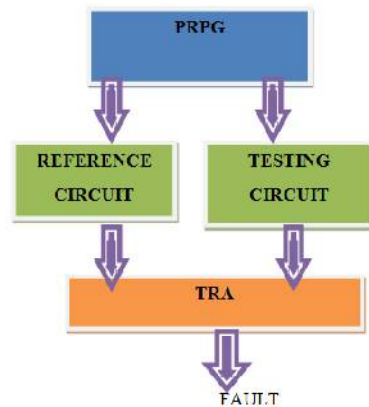


Fig 1. Test Pattern Generator

II. BASIC ARCHITECTURE

An n-bit PRPG connected with a phase shifter feeding scan chains forms a kernel of the generator producing the actual pseudorandom test patterns. A linear feedback shift register or a ring generator can implement a PRPG. More importantly, however, n hold latches are placed between the PRPG and the phase shifter. Each hold latch is individually controlled via a corresponding stage of an n-bit toggle control register.

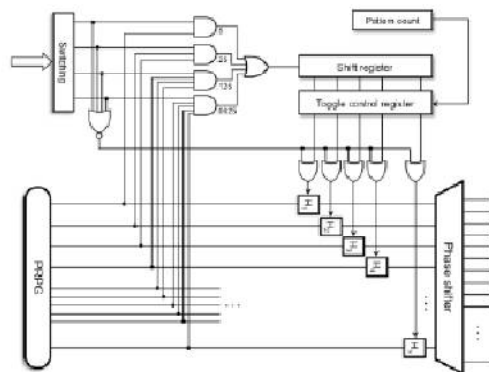


Fig 2. Basic architecture of a PRESTO generator

As long as its enable input is asserted, the given latch is transparent for data going from the PRPG to the phase shifter, and it is said to be in the toggle mode. When the latch is disabled, it captures and saves, for a number of clock cycles, the corresponding bit of PRPG, thus feeding the phase shifter (and possibly some scan chains) with a constant value. It is now in the hold mode. It is worth noting that each phase shifter output is obtained by XOR-ing outputs of three different hold latches.

Therefore, every scan chain remains in a low-power mode provided only disabled hold latches drive the corresponding phase shifter output the toggle control register supervises the hold latches. Its content comprises 0s and 1s, where 1s indicate latches in the toggle mode, thus transparent for data arriving from the PRPG. Their fraction determines a scan switching activity.

III. PROPOSED ARCHITECTURE

The ring generator can generate a single-input change (SIC) [3] sequence which can effectively reduce test power. The third approach aims to reduce the dynamic power dissipation during scan shift through gating of the outputs of a portion of the scan cells. Several low-power approaches have also been proposed for scan-based BIST. It will modifies scan-path structures, and lets the CUT inputs remain unchanged during a shift operation. Using multiple scan chains



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with many scan enable (SE) inputs [4] to activate one scan chain at a time, the TPG proposed in can reduce average power consumption during scan-based tests and the peak power in the CUT[4]. In a pseudorandom BIST scheme was proposed to reduce switching activities in scan chains. However, modules containing hard-to-detect faults still require extra test hardware either by inserting test points into the mission logic or by storing additional deterministic test patterns. In order to overcome this problem, an accumulator-based weighted pattern generation scheme was proposed. The scheme generates test patterns having one of three weights, namely 0, 1, and 0.5 therefore it can be utilized to drastically reduce the test application time in accumulator- based test pattern generation. However, the scheme proposed in possesses three major drawbacks More precisely it does not impose any requirements about the design of the adder (i.e., it can be implemented using any adder design) it does not require any modification of the adder and hence does not affect the operating speed of the adder. Furthermore, the proposed scheme compares favorably to the scheme proposed and in terms of the required hardware overhead. In this paper, we propose a PRPG for LP BIST applications. The generator primarily aims at reducing the switching activity during scan loading due to its preselected toggling (PRESTO) levels.

1) Minimum transitions: In the proposed pattern, each generated vector applied to each PRPG output, which can minimize the input transition and reduce test power. 2) Uniqueness of patterns: The proposed sequence does not contain any repeated patterns, and the number of distinct patterns in a sequence can meet the requirement of the target fault coverage for the CUT. 3) Uniform distribution of patterns: The conventional algorithms of modifying the test vectors generated by the LFSR use extra hardware to get more correlated test vectors with a low number of transitions. However, they may reduce the randomness in the patterns, which may result in lower fault coverage and higher test time. 4) Low hardware overhead consumed by extra TPGs[3]: The linear relations are selected with consecutive vectors or within a pattern, which has the benefit of generating a sequence with a sequential de-compressor[5]. Hence, the proposed TPG can be easily implemented by hardware. An n-bit PRPG [5] connected with a phase shifter feeding scan chains forms a kernel of the generator producing the actual pseudorandom test patterns. A linear feedback shift register or a ring generator can implement a PRPG. More importantly, however, n hold latches are placed between the PRPG and the phase shifter. Each hold latch is individually controlled via a corresponding stage of an n-bit toggle control register. As long as its enable input is asserted, the given latch is transparent for data going from the PRPG to the phase shifter, and it is said to be in the toggle mode.

When the latch is disabled, it captures and saves, for a number of clock cycles, the corresponding bit of PRPG, thus feeding the phase shifter (and possibly some scan chains) with a constant value. It is now in the hold mode. It is worth noting that each phase shifter output is obtained by XOR-ing outputs of three different hold latches. Therefore, every scan chain remains in a low-power mode provided only disabled hold latches drive the corresponding phase shifter output.

The performance of the PRESTO generator depends primarily on the following three factors (note that in the BIST mode they are delivered only once, at the very beginning of the entire test session): 1) The switching code (kept in the switching register); 2) The hold duty cycle (HC); 3) The toggle duty cycle (TC). The same signal allows the counter to have the input data kept in the Toggle or Hold register entered as the next state. Both the down counter and the T flip-flop [3] need to be initialized every test pattern. The initial value of the T flip flop decides whether the de-compressor will begin to operate either in the toggle or in the hold mode, while the initial value of the counter, further referred to as an offset, determines that mode's duration. As can be seen, functionality of the T flip-flops remains the same as that of the LP PRPG but two cases. First of all, the encoding procedure may completely disable the hold phase (when all hold latches are blocked) by loading the Hold register with an appropriate code, for example, 0000. If detected (No Hold signal in the figure), it overrides the output of the T flip-flop by using an additional OR gate, as shown in Fig. 3. As a result, the entire test pattern is going to be encoded within the toggle mode exclusively. In addition, all hold latches have to be properly initialized. Hence, a control signal First cycle .

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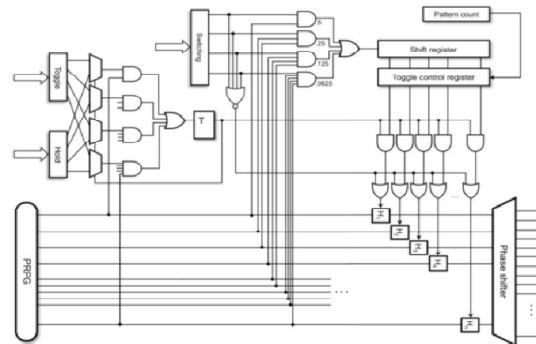
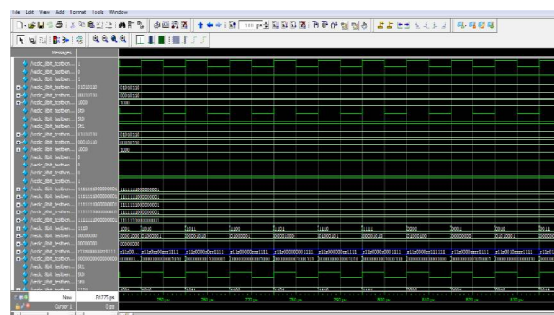


Fig.3. Fully operational version of PRESTO

IV. SOFTWARE IMPLEMENTATION RESULTS

Simulation is the process of verifying the functional characteristics of models at any level of abstraction. We use simulators to simulate the Hardware models. To test if the RTL code meets the functional requirements of the specification, we must see if all the RTL blocks are functionally correct. To achieve this we need to write a test bench, which generates clk, reset and the required test vectors. A sample test bench for a counter is shown below.

the toggle control register supervises the hold latches. Its content comprises 0s and 1s, where 1s indicate latches in the toggle mode, thus transparent for data arriving from the PRPG. Their fraction determines a scan switching activity. The control register is reloaded once per pattern with the content of an additional shift register. The enable signals injected into the shift register are produced in a probabilistic fashion by using the original PRPG with a programmable set of weights.



a) Functional verification in Modelsim

V. CONCLUSION

In the paper we carried out transition controlled PRNG and the LP decompressor design and its testing quality metrics through modelsim based simulation which can produce pseudorandom test patterns with scan shift-in switching activity precisely. The switching activity can be easily control the generator, so that the resultant test vectors can either yield a desired fault coverage faster than the conventional pseudorandom patterns while still reducing toggling rates down to desired levels, and offer visibly higher coverage numbers if run for comparable test times. And this design is extended into fully functional test data de-compressor with the ability to control scan shift-in switching activity through the process of encoding. The efficiency of proposed combine test compression with logic BIST is verified and proved to deliver high quality test.



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BIOGRAPHY



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