



# Design Of Efficient Shift Register with Double Edge Triggered Flip-Flop

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**ABSTRACT:** Energy efficiency is an important factor in digital designs. A large amount of power consumption is due to storage elements and clock distribution networks. For storage elements, instead of using single edge triggered flip-flop, Double Edge Triggered Flip-flop is used to save energy as they can maintain the same throughput with half of clock frequency. Clock gating is used to reduce the dynamic power consumption. Incorporating clock gating with double edge triggered flip-flop further reduces power consumption but introduces asynchronous data sampling. In proposed system, shift register is built with Double Edge Triggered flip-flop and the asynchronous data sampling is removed using in The circuit is simulated with Tanner Tool v14.1 and Modelsim 6.3f.

**KEYWORDS:** Asynchronous Data Sampling, Double Edge Triggered Flip-Flop, Clock Gating

## I. INTRODUCTION

Power consumption is becoming an crucial factor in digital designs. For a digital system, the power spent on the clock-tree and the storage element is a major source of power consumption. The Clock system accounts for 30% to 60% of the total power dissipation. As a result, deducing the power consumed by storage elements such as flip-flops and clock system will have a deep impact on the total power consumption. One effective and efficient approach is Double edge triggered flip flop (DETFF).Dual edge clocking requires Dual Edge-Triggered Storage Elements (DETSE), capable of capturing data on both rising and falling edge of the clock. Main advantage of DETSE is their operation at half the frequency of the conventional single-edge clocking, while obtaining the same data throughput. The second technique is Clock-gating for a large digital system, clock-gating technique is used to reduce the power consumed on idle circuitry in the design. The DETFF and clock gating combined together to further reduce dynamic power but it introduces the asynchronous data sampling problem between the clock edges at the output side it creates the data miss-communication error. This paper deals with the design of shift register with DETFF various clock gated DETFF proposed to analyze the sampling problem

## II. EXISTING SYSTEM

### A. Double Edge Triggered Half-Static Clock-Gated D Flip-Flop:

The Double Edge triggered half Static Clock Gated D-type Flip-Flop (DHSCGFF) design[1], which consists of two identical dynamic master latches and a half-static slave latch. Compared with the SET implementation[2], this DHSCGFF consists of an additional master latch in parallel to the original master latch. Unlike Yu's circuit[3], the proposed circuit does not swap the use of master and slave latches in alternative clock phases to avoid the problem of coupling the half-static latch directly to the input data path. Instead, these two master latches are triggered in alternative clock edges, which are controlled by two complementary signals C and  $C_{\text{bar}}$ .

# International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 11, November 2014

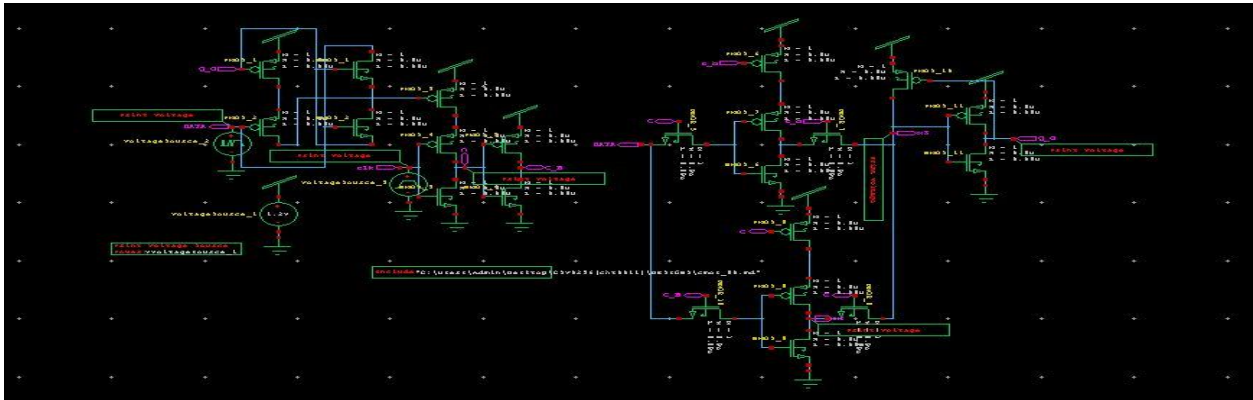


Fig.1 Double Edge Triggered Flip-Flop Half Static Clock Gated D-type Flip-Flop

A half-static slave latch stores the data from each master latch in alternative clock phases. The clock-gating circuit compares D with Q and outputs a logic "HIGH" at R to turn transistor M2 off when D = Q. This configuration suppresses the control signal C by deactivating the inverter chain. The core of the flip-flop is edge-triggered by C and  $C_{bar}$  so that it does not require the use of any pulse generator to generate a pulse-like transparent window within the flip-flop. The pass transistor logic simplifies the circuit and reduces the internal power dissipation. The circuit complexity and transistor count of the DHSCGFF is reduced by using pass transistor based clock-gating circuit, dynamic master latches and half-static slave latch, and thus reduces the total power dissipation. In contrast to other Latch-Mux double edge-triggered flip-flops that place a logic keeper at Node  $X_2$  to floating nodes (as well as the corresponding Node  $X_1$  in upper path), Tam's design added switches  $M_{B1}$  and  $M_{B2}$  into the latch that intentionally isolate Nodes  $X_1$  and  $X_2$ .

For transitions on D input that occur during global clock  $CLK=0$ , an asynchronous pulse is generated on internal clock. Then before switch  $M_{A2}$  turns OFF, there is only a very short amount of time for Node  $X_0$  to charge or discharge. If the value of  $X_0$  is strong enough to flip the nodes to the output, then an asynchronous transition will appear at the output. Otherwise, if the first trigger of the lower path has not successfully passed the input D to the output, then the upper path serves as a backup that will be triggered at the next falling edge of internal clock C.

### C. Methodologies To Remove Asynchronous Data Sampling:

By adjusting the transistor sizes around Node  $X_2$ , there are multiple sets of transistor sizing that can cause the asynchronous data sampling to fully appear (i.e., show both cases), partially appear (i.e., only one case is observed) or be hidden. The condition that makes the asynchronous transition appear depend upon whether the voltage of Node  $X_3$  reaches the critical value to flip the output.

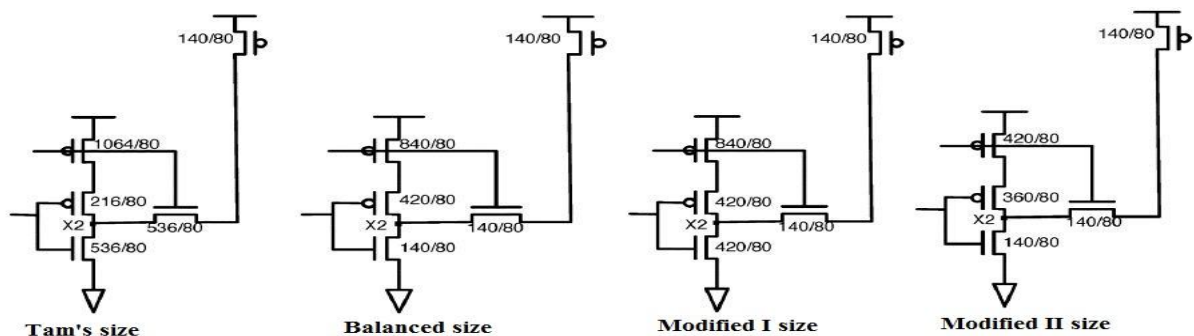


Fig.2 Modified Circuit of Node  $X_2$

The circuit's parameters such as transistor size are modified to eliminate Asynchronous Data Sampling.

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Vol. 2, Issue 11, November 2014

1. Balanced sized—the circuit produces similar rise and fall time, but one asynchronous transition appears in result.
2. Modified I—this circuit demonstrates that both possible asynchronous transitions can appear.
3. Modified II—the circuit demonstrates that both possible asynchronous transitions are removed.

### III. PROPOSED SYSTEM

In the proposed system, Double Edge Triggered Flip-Flops (DETFFs) are used to build shift register in order to reduce the power consumption, as that they can able to maintain the same throughput as single edge-triggered between flip-flops (SETFFs) while only using half of the clock frequency. Clock gating is also employed in this shift register to further reduce the power consumption. Incorporating Clock gating in shift register introduces Asynchronous Data Sampling problem that produces error in output.

#### A. Shift Registers

In digital circuits, Shift registers are a type of sequential logic circuit, used for the storage of digital data. Shift register is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the data input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the bit array stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input

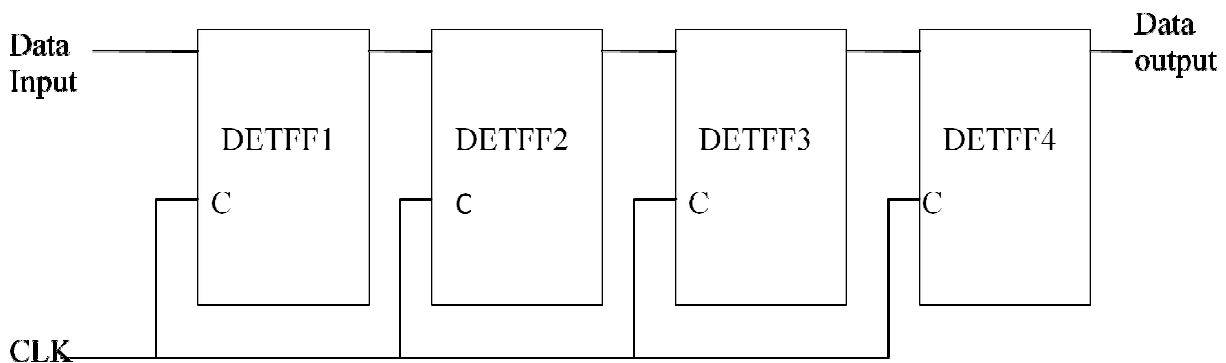


Fig.3 Implementation of Shift register with Double Edge Triggered Flip-Flop

The implementation of Shift register with Double Edge Triggered Flip Flop is shown in the Fig.3. The DETFF used in this design is Double Edge Triggered Half Static Clock Gated D-type Flip-Flop(DHSCGFF). The DHSCGFF is chosen for the implementation, as it consumes less power and delay and the Asynchronous Data Sampling is removed for this Flip-Flop. The data string is given a data input and is shifted right one stage each time 'Data Advance' is brought high. At each advance, the bit on the far left "Data Input" is shifted into the first flip-flop's output. The bit on the far right "Data output" is shifted out and lost. The data are stored after each flip-flop produces data output.

#### A. Scheme To Avoid Asynchronous Data Sampling:

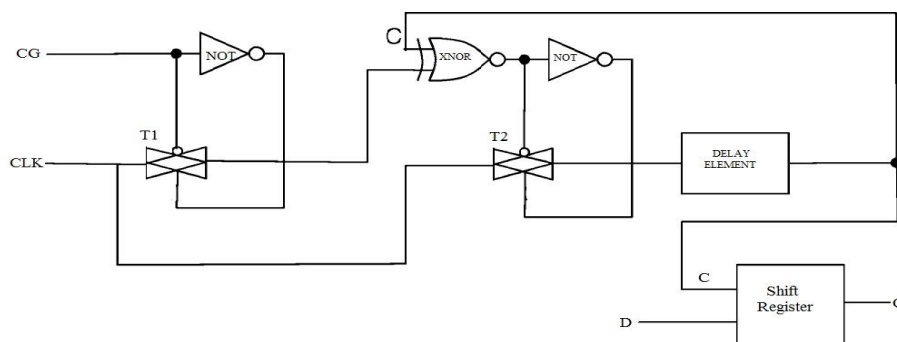


Fig..4 Scheme to avoid Asynchronous Data Sampling



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In the Scheme shown in the Fig.4 the CLK is controlled by the comparison of D and Q. If D has changed since the last clock transition and is different from Q, then CLK will pass to the second comparator to compare with the C. This CLK and C comparator controls the switch T2 between the CLK and C.

This second comparator prevents the asynchronous sampling occurred in this implementation. Asynchronous sampling occurs when D changes at the moment that CLK differs from C. However, with the second CLK & C comparator in Fig.4, the switch T2 will stay OFF when  $CLK \neq C$  and C will synchronize with CLK. In the next half cycle, the switch T2 turns ON, where  $CLK = C$ , but since they are equal, the flip-flop will not be triggered until C changes, which follows CLK when is ON.

## IV. POWER ANALYSIS

DESIGN	POWER CONSUMPTION ( $10^{-5}W$ )
DHSCGFF	13.24
Balanced Size	9.29
Modified I	9.93
Modified II	4.38

Table.1 Power of various DHSCGFF

Parameter	Shift Register with DHSCGFF	Shift Register with D Flip-Flop
Average Power	$7.74 \times 10^{-5}W$	$1.39 \times 10^{-4}W$
Minimum Power	$5.29 \times 10^{-8}W$	$1.25 \times 10^{-5}W$

Table.2 Comparison of Shift Register with DHSCGFF and D-FF

From the Table.1 it is shown that power consumption of Modified-II circuit is less when compared with DHSCGFF, Balanced size and Modified-I circuit. Modified-II circuit consumes less power because its critical parameters such as transistor's size is modified according to circuits specified limits.

Thus from the Table.2, it is proven that Shift Register built with Double Edge Triggered Flip-Flop consumes less amount of average power and minimum power when compared with Shift Register built with D Flip Flop.

The Shift Register built with Double Edge Triggered Flip-Flop consumes less power as that it can able to produce the same throughput with half of clock frequency of Single Edge Triggered Flip-Flop and it can produce double the throughput when compared with Single Edge Triggered Flip-Flop. As the power consumption in Flip-Flop circuits greatly depends on clock frequency, reducing the clock frequency in Double Edge Triggered Flip-Flop produces a good impact in power consumption of Shift Register built with Double Edge Triggered Flip-Flop.

## V. RESULTS AND DISCUSSION

From the output of DHSCGFF circuit shown in the Fig.5, it is analyzed that asynchronous data sampling occurs if D changes when  $CLK=0$  (before falling edge). In the DHSCGFF Balanced Size circuit in Fig.6 is large amount of delay occurs in output and a small error occurs due to asynchronous data sampling problem. If the DHSCGFF Modified-I circuit in Fig.7 is simulated delay occurs in output and error due to asynchronous data sampling problem are removed. In the DHSCGFF Modified-II Size both the delay problem and errors due to asynchronous data sampling problem are completely removed. From the result, it is proved that by modifying the size of transistor in various aspects of Tam's design reduces the delay and removes Asynchronous Data Sampling.

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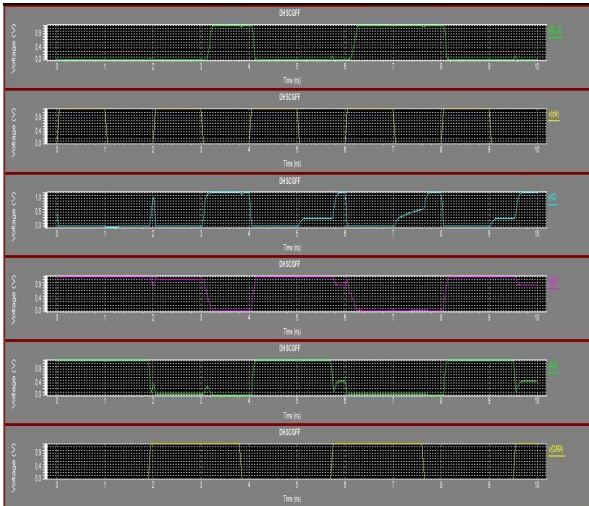


Fig.5 Output waveform of DHSCGFF circuit

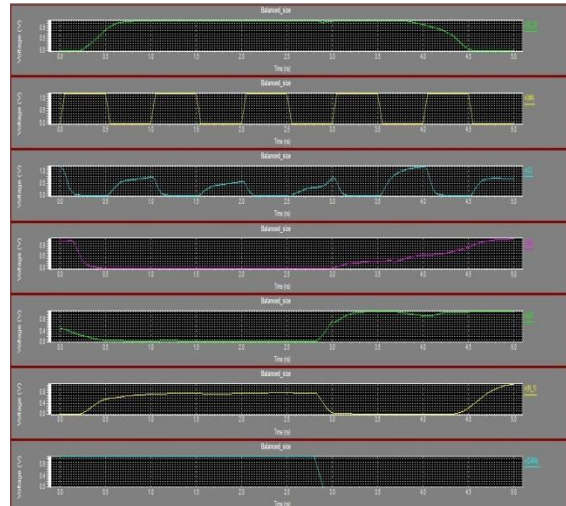


Fig.6 Output of DHSCGFF in Balanced size

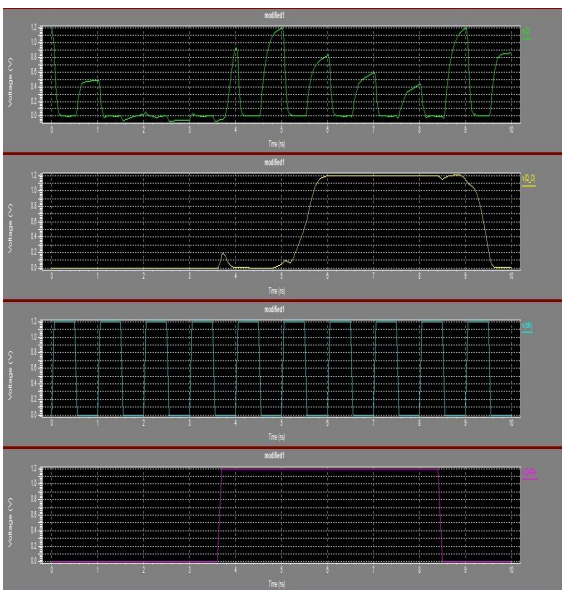


Fig.7 Output of DHSCGFF in Modified-I size

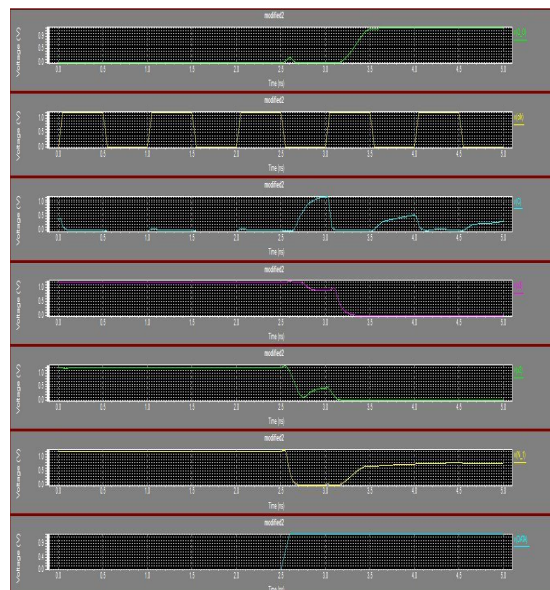


Fig.8 Output of DHSCGFF in Modified-II size

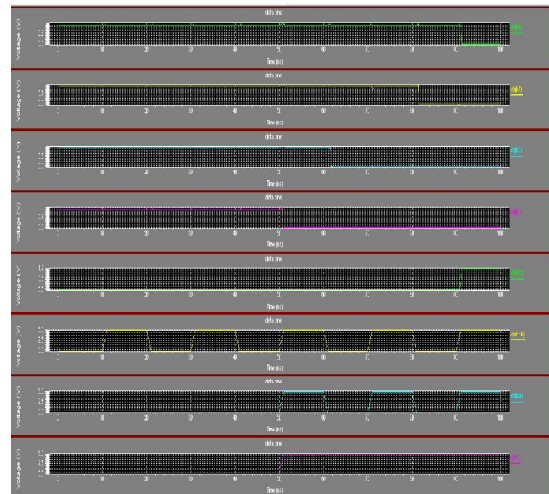
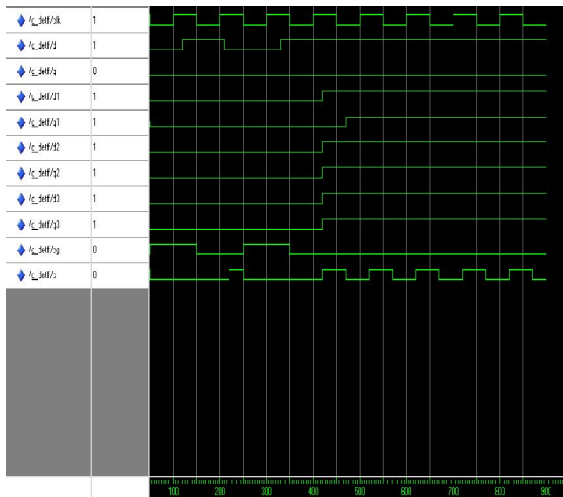


Fig.9 Output waveform without Asynchronous Data Sampling Error Fig.10 Simulation result of shift Register with DETFF

Simulation result of the asynchronous data sampling with respect to the behavior of the clock signal is shown in the Fig.9 The clk is the clock signal and the other inout signals will have the output as shown. For each simulation, four data switching cases have been tested respectively, from left to right: 1) D changes from 1 to 0 before a falling edge; 2) D changes from 0 to 1 before a rising edge; 3) D changes from 1 to 0 before a rising edge; and 4) D changes from 0 to 1 before a falling edge. The asynchronous transitions have been removed.

In the Shift Register built with Serial In Serial Out Configuration using Double Edge Triggered Flip-Flop Fig.10, the data are shifted in the order of one bit at a time on a single line. It produces the stored information on its output also in serial form. During each clock pulse, one bit is transmitted from left to right and from this output result it is shown the four bits (1010) being serially shifted out of the register and replaced by all zeros.

## VI.CONCLUSION

DETFF and clock gating are two methods to reduce dynamic power consumption, and both of them are successful when used separately. However, when applying clock gating into a DETFF, a data transition error may appear at the output between clock edges due to asynchronous data sampling, which has been defined and discussed. Solution has been provided to avoid the asynchronous sampling problem in clock-gated DETFF. The delay buffer using 4-bit serial-in serial-out shift register has implemented for the analysis of asynchronous data sampling. The power comparison between the Shift register implemented using double edge triggered flip-flop and D flip-flop shows that the average power and minimum power consumption of double edge triggered flip-flop is less compared to the implementation of shift register with D flip-flop. Thus the shift register was built using Double Edge Triggered Flip-Flop and the asynchronous data sampling is removed using proposed schemes.

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