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High Power Factor Bridgeless SEPIC Converter to Improve Total Harmonic Distortion

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ABSTRACT: The use of power electronic devices has increased, which have an effect on the gird. Thus to reduce the harmonics and reduce the effect on the grid active power filter technique is used. The single ended primary inductor converter (SEPIC) bridgeless power factor correction circuit is examined. The SEPIC converter is intended for 400V output. The performance analysis of the bridgeless SEPIC converter is demonstrated and verified using MATLAB/SIMULINK.

KEYWORDS: bridgeless SEPIC converter; total harmonic distortion THD; power factor correction PFC

I. INTRODUCTION

As many devices like computers make use of power electronics circuits, which uses switched mode power supplies (SMPS), if their design is inappropriate due to the existence of nonlinear loads the harmonics are introduced. Based on the IEC 61000-3-2 standard the harmonics present in these equipments are limited. [1].The power factor correction circuits can be Buck, Boost, Buck-Boost, SEPIC, Ćuk converters.

A buck converter is used in the devices where the load voltage is less than the source voltage. Since the buck converter has discontinuous input current, an extra filter is required to avoid such currents. To overcome this problem, buck-boost, SEPIC and Ćuk converters are used. The load voltage will be less than the source voltage and the source current is continuous in nature as these converters are used in both discontinuous conduction mode (DCM) and continuous conduction mode (CCM) [2]. The power factor correction process is used in common since it improves the power factor and efficiency of the circuit. Bridgeless boost converters are commonly used due to their decreased input current ripple. The power factor converter circuits have low output voltage;thus, they are used in many applications. A bridgeless buck converter is proposed in paper [3] and [4]. The conventional PFC buck converter has the load voltage less than the input voltage peak value [7].

Due to the step-up/down behaviour of the SEPIC converter, it can provide high factor no matter its output is less or more than the input voltage. SEPIC converter efficiency can be made better by eliminating the diode bridge which is present in the input side of the circuit; instead it requires large input inductor current and LC filter to reduce the input current ripple.

This paper put forth the bridgeless SEPIC converter to improve the THD by reducing harmonics and to improve the power factor in the circuit. The proposed circuit has a bridge and the DC/DC converter as the one stage of operation. Section 2 gives an impact on the SEPIC PFC circuit working modes. In section 3 the circuit design parameter for the SEPIC converter is explained briefly. The simulation results are shown in section 4. Lastly Section 5 concludes the work and discuss about the scope for future work.

The conventional SEPIC converter circuit is as shown in figure 1. There are two modes of operation based on the switch position. When switch Q_1 is ON, diode D will not conduct. The inductor L_1charges, output inductor L_2 and capacitor C_1 together make a resonant circuit. The Load current is drawn from the load capacitorC_0. In this mode the input inductor voltage will be equal to the input voltage. In second mode of operation, as soon as the switch Q_1 is

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turned off the diode will start conducting. Therefore, this creates the loop L_1, C_1, L_2. The inductor discharges as it is directly connected to load.

II. BRIDGELESS SEPICPFC CONVERTER

The bridgeless SEPIC converter has three dynamic switches Q_1, Q_3, Q_4 as shown in the figure 2. When all three switches are switched ON simultaneously the source current will increase linearly. The voltage across the inductor L_2 and the voltage across the capacitor C_1 will be equal and the output inductor current i_{L2} starts decreasing linearly. In next mode the switches Q_1, Q_3, Q_4 are off and diode D is made to conduct. Till the diode current quenches the inductor current on the source side decreases and inductor current i_{L2} increases. At the point when D is off, load gets disconnected from the source, and the inductor current float at input. The different working modes of SEPIC PFC converter is as shown in figure 3.

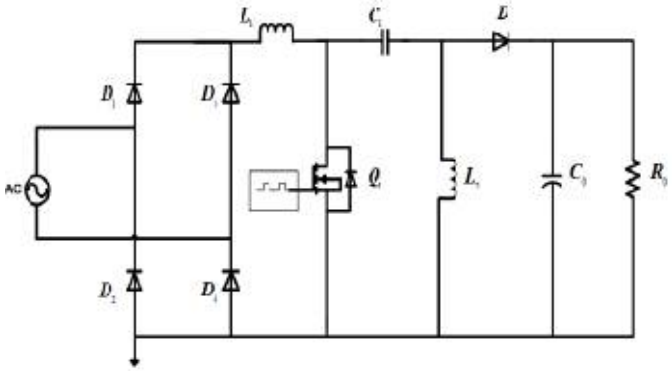

Figure 1: Conventional SEPIC PFC converter

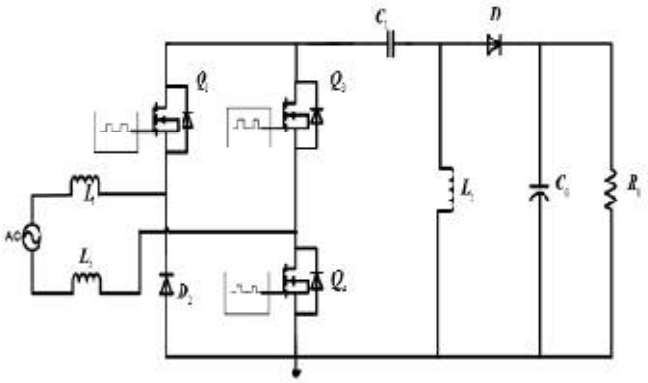

Figure 2: Bridgeless SEPIC PFC converter

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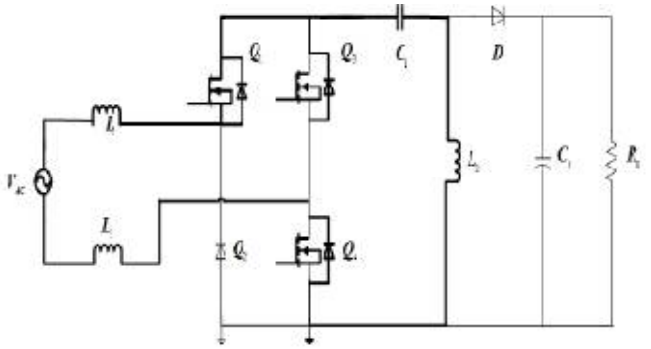
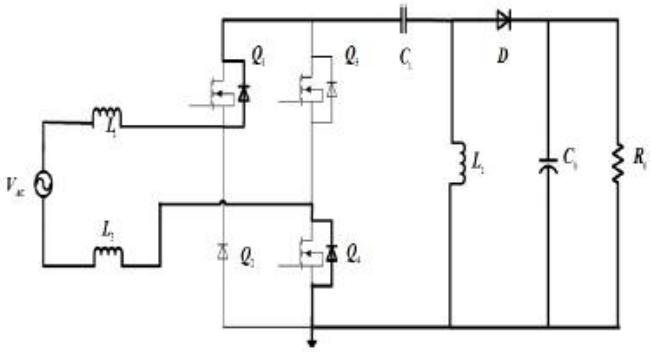
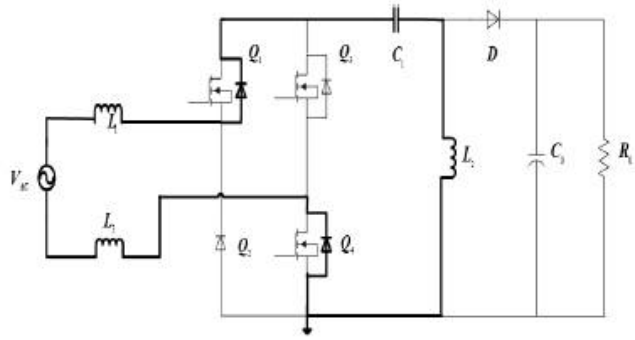


(a)



(b)



(c)

Figure 3: Operating modes for bridgeless SEPIC PFC converter

III. PRINCIPLE OF OPERATION

The SEPIC converter circuit formed by two proportioned designs is as shown in figure 3. The circuit operation in positive half cycle for switching time T_s is divided in to three different modes of operation as shown in figure 3(a-c).
Mode 1: When the switches Q_1, Q_3, Q_4 are turned on simultaneously, the source inductor current increases whereas the load inductor current decreases with the proportional rate of the source voltage V_{in}. Figure 3(a) shows working of the converter in this mode of operation. The rate of change of inductor currents can be written as

$$\frac{di_{ac}}{dt} = \frac{di_{L1}}{dt} = \frac{di_{L3}}{dt} = \frac{V_{in}}{L_{1,3}} \qquad (1)$$

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$$\frac{di_{L2}}{dt} = -\frac{V_{in}}{L_2} \quad (2)$$

Where $L_{1,3}$ value is given by

$$\frac{1}{L_{1,3}} = \frac{1}{L_1} + \frac{1}{L_3} \quad (3)$$

Therefore, the switch current is given by

$$i_{Q3} = i_{ac} - i_{L2} = \frac{V_{in}}{L_{1,3}} + \frac{V_{in}}{L_2} \quad (4)$$

This mode ends when Q_1, Q_3, Q_4switches are switched off.
Mode 2: When the switches Q_1, Q_3, Q_4 are switched off but the switches Q_1 and Q_4 are still conducting due to the free-wheeling action of the diodes which are connected across the respective switches. The diode *D* starts conducting providing the path for source and load currents. The source inductor current decreases linearly at a rate relative to the load voltage V_{out} and the load inductor is increased linearly. The inductor current can be obtained by the equations

$$\frac{di_{L1}}{dt} = \frac{di_{L3}}{dt} = -\frac{V_{in}}{L_{1,3}} \quad (5)$$

$$\frac{di_{L2}}{dt} = -\frac{V_{in}}{L_2} \quad (6)$$

Mode 3: The switches Q_1, Q_3, Q_4 are switched off, as shown in the figure 3(c). But the switches Q_1 and Q_4 are made to conduct through anti parallel diodes. The inductor currents are equal in this mode. The diode and switch voltage are equal to load and source voltage respectively. The time duration in this mode is given by

$$\Delta_1 = \frac{V_{in}}{V_{out}} \times d \quad (7)$$

Where *d* is the duty cycle.

IV. DESIGN OF THE BRIDGELESS SEPIC CONVERTER

The converter is designed for the SEPIC PFC converter. A 230V_{rms} 60Hz AC input to generate 400V dc output is designed for the proposed converter with a source current ripple is equal to 20% of the maximum value of AC current with switching frequency f_s 30 *kHz*.
The computation to find the values of inductors L_1 andL_2 is as follows. By assuming an efficiency of 95% the following equations are derived is as shown below

$$I_{in} = I_{in\_peak}\sin(\omega t) = \frac{2 \times P_o}{\eta \times V_{in\_peak}}\sin(\omega t) \quad (8)$$

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$$I_{in\_peak} = 2.58A$$

Input current ripple is

$$\Delta I_L = 20\% I_{in_{peak}} = 0.52A$$

$$\Delta I_L = \frac{V_s \times d}{L_1 \times f_s} \quad (9)$$

The load current in a switching time is equal to the fast diode average current. The load current switching time is given by

$$i_{o\_avg} = 0.5 i_{o\_peak} \Delta_1 \quad (10)$$

Where, i_{o_avg} is the maximum current of fast diode and Δ_1 is the duty cycle of D, $\Delta_1 < 1 - d$, and i_{o_avg} can be calculated as:

$$i_{o\_peak} = i_{L1} + i_{l2} = \left(\frac{1}{L_1} + \frac{1}{L_2}\right) V_{in} dT_s \quad (11)$$

$$i_{o\_avg} = 0.5 \left(\frac{{V_{in}}^2}{\left(\frac{1}{L_1} + \frac{1}{L_2}\right) V_o} d^2 T_s \right) \quad (12)$$

$$I_{dc\_avg} = (1/\pi) \int_0^{\pi} i_{o\_avg}\, d\omega t = \frac{{V_{in\_peak}}^2}{4 L_e V_o} d^2 T_s \quad (13)$$

Where, $L_e = \frac{L_{1,3} \times L_2}{L_{1,3} + L_2}$

From (7), the duty ratio d can be designed as:

$$d < \frac{V_0}{V_{in} + V_0} = 0.55 \quad (14)$$

Selecting $d = 0.5$.

$$L_e = \frac{{V_{in\_peak}}^2 \times d^2}{4 \times V_o \times f_s \times I_{0\_avg}} \quad (15)$$

L_1 *and* L_3 can be obtained as

$$L_{1,3} = \frac{V_{in\_peak} \times d}{f_s \times \Delta I_L} = 10.42mH \quad (16)$$

$$L_1 = L_3 = \frac{L_{1,3}}{2} = 5.21mH$$

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Therefore, L_2 can be obtained from the equation

$$\frac{1}{L_2} = \frac{1}{L_e} - \frac{1}{L_{1,3}} \Rightarrow L_2 = 581.7\mu H \quad (17)$$

The output capacitance can be calculated as

$$C_o = \frac{P_{load}}{V_o \times \Delta V_o(\%) \times 4 \times f_{ac}} = 20.8mF \quad (18)$$

The converter is controlled in multi loop fashion. The reference current is generated by voltage controller to maintain constant DC voltage and to generate the gate pulses PI controller is used. The SIMULINK model is as shown in the figure 4.

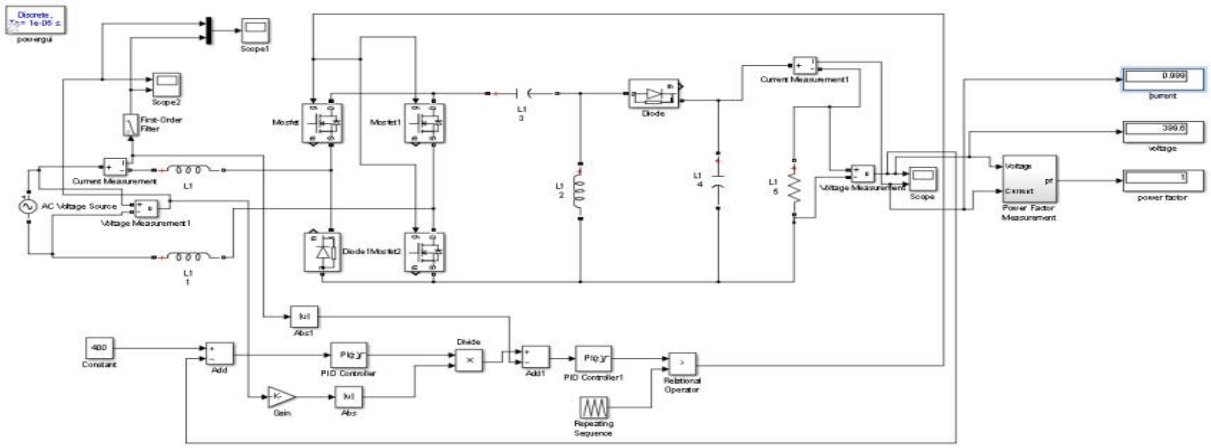

Figure 4: Simulation model of bridgeless SEPIC PFC converter circuit.

V. RESULTS AND DISCUSSIONS

The MATLAB/SIMULINK model of the bridgeless SEPIC PFC converter circuit is carried out. Figure 5 shows source voltage and current of the proposed converter. Figure 6 shows the output voltage and current of the proposed converter. The THD is shown in the Figure 7. The THD of the converter is 6.44% and power factor is improved to unity. The present topology gives better THD and Power Factor for high voltage application.

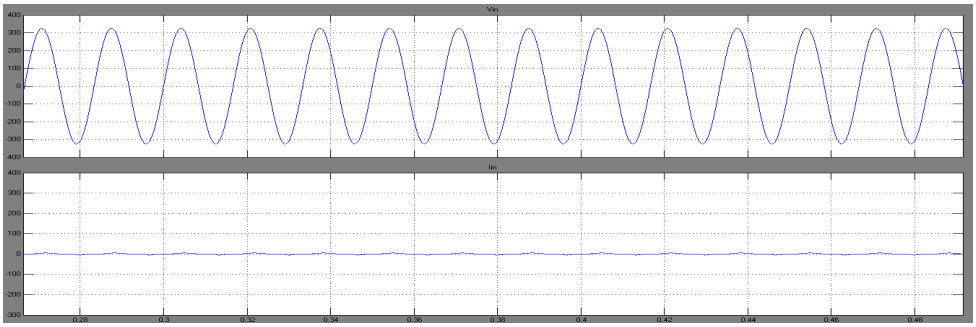

Figure 5: The source voltage and current of bridgeless SEPIC PFC converter.

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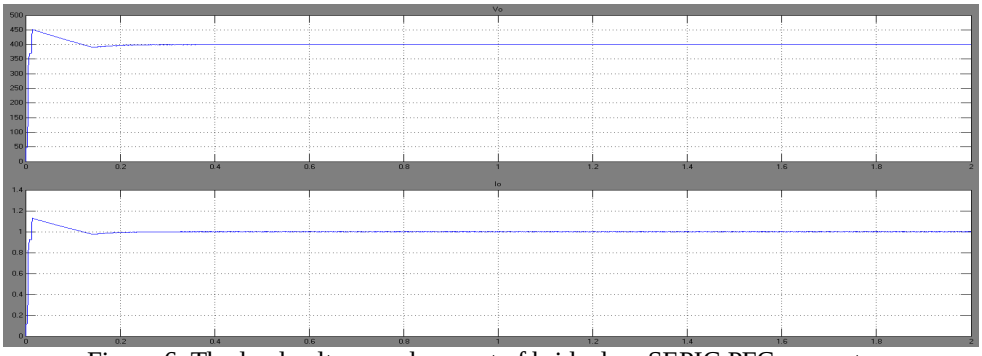

Figure 6: The load voltage and current of bridgeless SEPIC PFC converter.

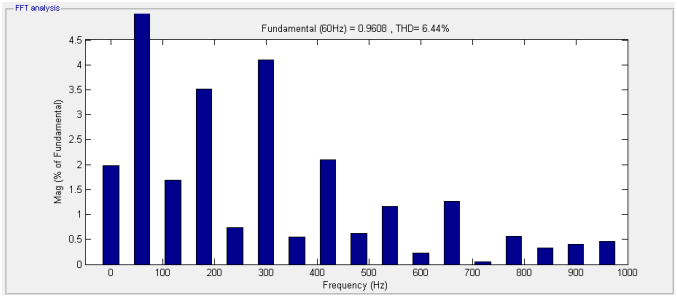

Figure 7: THD of the Bridgeless SEPIC PFC converter.

VI. CONCLUSION

The proposed bridgeless SEPIC converter is verified using MATLAB/SIMULINK tool. From simulation study, it is observed that the diode bridge in the input side is eliminated. Due to the elimination of this diode bridge the overall THD is improved to a better value and with the improvement in the power factor. The simulation is performed for high input voltage and the THD was reduced to 6.44%. The topology implemented is operating for 230V AC input to generate 400V DC output and unity power factor.

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