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Design of Pulse Width Modulation Controller on FPGA using HDL

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ABSTRACT: The paper develops high frequency PWM controller using FPGA. Pulse width modulation (PWM) has been widely used in communication and control system. PWM control is the most powerful technique that offers a simple method for controlling of analog systems with digital output. The simulated results having PWM frequencies up to 248.69 MHz can be produced with a duty cycle resolution of 0.39%. The VHDL modeling is used in the design process of PWM.

KEYWORDS: Pulse width modulation, Field programmable gate array, Hardware description language

I. INTRODUCTION

Pulse width modulation has been widely used in many applications especially in communication and control systems. The paper develops high frequency PWM generator architecture for using FPGA.Using pulse width modulation (PWM) in control system is not new, there are different approaches for developing pulse width modulation. Many digital circuits can generate PWM signals, but what is interesting is, to generate pulse width modulation using Hardware Description Language (VHDL) and implementing it on FPGA. FPGA implementation of PWM is selected because FPGA can process information faster, controller architecture can beoptimized for space or speed.In PWM, the time period of the square wave is kept constant and the time for which the signal remains high is varied.

PWM is a technique to provide a logic "1" and logic "0" for a controlled period of time. It is a signal source involves the modulation of its duty cycle to control the amount of power sent to a load. The following paper describe the design of PWM on a FPGA using very high speed integrated circuit hardware description language (VHDL). The PWM generates pulses on its output. The pulses are made in such a way that the average value of highs and lows is proportional to the PWM input. The duty cycle of the signal can be varied. A PWM input can be of any width. Most common values are 8-bits and 16-bits. A PWM signal is a constant period square wave with a varying duty cycle (on-time compared to off-time). In other words, the frequency of a PWM signal is constant but the time the signal remains high varies as shown in Figure 1. The duty cycle (percent on time) is given by τ/T.

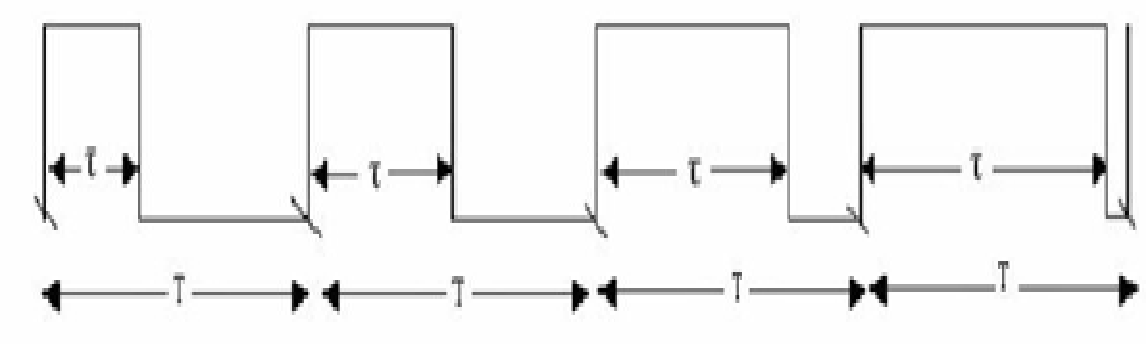

Fig.1 PWM signal with different duty cycles

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FPGAs are configurable ICs (user can design, program and make changes to his circuit whenever he wants)and used to implement logic functions. Today's FPGAs can hold several millions gates and have some significant advantage. They ensure ease of design, lower development costs and the opportunity to speed products to market. FPGA are programmable semiconductor devices that are based around a matrix of configurable logic block (CLBs) connected via programmable interconnects. FPGA can be programmed to the desired application or functionality requirement.

VHDL is a language that is used to describe the behaviour of digital circuit designs. It is VHSIC (Very High Speed Integrated Circuit) Hardware Description Language , and now used extensively by industry and academia for the purpose of simulating and synthesizing digital circuit design. Its designs can be simulated and translated into a form suitable for hardware implementation.VHDL modelling is used to generate the PWM.

To design the PWM in Field programmable gate array, first the functional description of the design modelled in very high speed integrated circuit HDL using the behavioral abstraction level and this VHDL code is synthesized and simulated using Xilinx Synthesis and simulation tool. After successfully synthesized and simulated the design it can be downloaded to the targeting device (FPGA).

II. RELATED WORK

The digital implementation of PWM is an important research area.The arrival of FPGA in power electronics brings out a dramatic change in the digital PWM control applications. With FPGA, the researchers got a better alternative solution for the digital implementation of PWM .The content of this thesis are based on various scholastic papers. Some of the papers are mentioning below and a brief idea of what they are about are mentioned. The digital implementation of PWM is an important research area.The arrival of FPGA in power electronics brings out a dramatic change in the digital PWM control applications. With FPGA, the researchers got a better alternative solution for the digital implementation of PWM .The content of this thesis are based on various scholastic papers. Some of the papers are mentioning below and a brief idea of what they are about are mentioned.

In [6], in this paper results show that PWM frequencies up to 3.985 MHz can be produced using the proposed design method with a duty cycle resolution of 1.56% using the Xilinx Foundation software v3.1. In [7], in this paper experimental results show that PWM frequency with an 8-bit data input was 46.875 kHzusing the XS40 v1.2 board, which contains the Xilinx 4010XLPC84-3 FPGA and PWM frequencies up to 3.985MHz can be produced with a duty cycle resolution of 1.56%.In [8], in this paper generation of PWM signals with varying duty cycle using VHDL code and tested on FPGA. A FPGA SPARTAN3 board is used as hardware and ISE10.1 XILINX is used as software. The generated PWM signals have a fixed frequency 10MHz.In [9], the generation of PWM signals is discussed using VHDL based on FPGA. A board SPARTAN3AN is used as a hardware and ISE14.4 XILINX is used as software. The generated PWM signals have a fixed frequency(11.8 KHz) depended on the frequency of sawtooth, and a variable duty cycle that changes from 0% to 100%.In [10],in this paper there are two classes of PWM techniques identified optimal PWM and carrier PWM.

The optimal PWM requires lot of computation and hence extra hardware and hence extra cost .Carrier PWM techniques require a carrier signal which is modulated with modulating signal to produce desired PWM signal. There are various methods depending upon architecture and requirement of the system. Their design implementation depends upon application type, power consumption, semiconductor devices, performance and cost criteria.In [11],in this paper PWM Generator architecture is used for low power switching supplies**.** The architecture is based on the principle that due to triggering of a counter by clock signal, clock is set equal to some multiple of switching frequency with help of a counter. The PWM output signal is set high before the clock signal and it remains high until it is reset after the counter value becomes equal to the duty cycle value.

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III. FUNCTIONAL DESCRIPTION OF THE PWM DESIGN

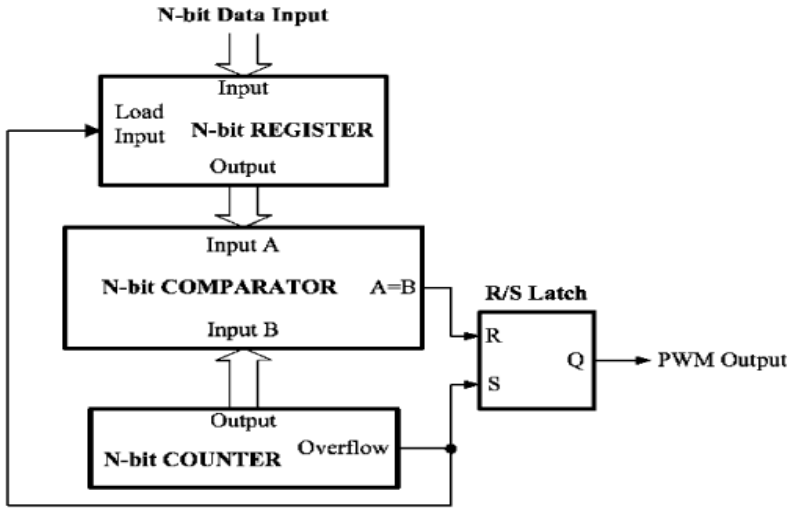

Fig.2 Block Diagram of PWM

The block diagram of the proposed architecture is shown in Fig.1. The system input is an N-bit dataword, corresponding to the desired PWM duty cycle value. The register stores the input to be processed .So when load signal is '1' the register provides input to output. The counter used is 8 bit up-counter. The N-bit register output, containing the N-bit data input, is compared with the output value of an N-bit counter, by means of a comparator. Whenthese two values become equal, the comparator output is used to reset the R/S latch output which produces the PWM wave. The R/S latch output is set when the counter reaches an overflow condition atthe end of a PWM period. Also, the counter overflow signal is used to load the N-bit data input to the input register. R S latch is used to set or reset the output. When 'r'signal is '1' output is reset to '0'.When 's' signal is '1' output is set to '1'.
The duty cycle is given from the following equation:
Duty Cycle = Data Value/2^n
where, Data Value is the N-bit input data value.

For an 8 bit input, resulting in 2^8 different duty cycle states. The duty cycle of the PWM signal is controlled by the data value. The higher the data value the higher the duty cycle.If an 8-bit input is used, then the duty cycle is in the range $0 \leq D \leq \frac{255}{256} = 99.6\%$. Since the PWMduty cycle has 2^8 different states, the generator resolution,α, is defined as,

$$\alpha = \frac{1}{2^N} \bullet 100\% = \frac{1}{2^8} \bullet 100\% = 0.39\%$$

Data value	Duty Cycles (%)
00000011	1.95
00010001	7.42
01111110	50
11110000	94.53

Table 1: Some of the Data Values for different Duty Cycles (N=8)

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Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1	1920	0%
Number of 4 input LUTs	2	3840	0%
Number of bonded IOBs	4	141	2%
Number of GCLKs	1	8	12%

IV. SIMULATION RESULTS

A software program using the VHDL language was developed, for synthesizing the block diagram presented in theprevious section, using the Xilinx ISE Design Suite 13.1 software. The RTL view of block diagram in fig.1 is shown in fig.3 and 4 and simulated waveforms are shown in fig.5,6.From the simulated waveform ,we observe that higher the data value , higher the duty cycle and lower the data value, lower the duty cycle.

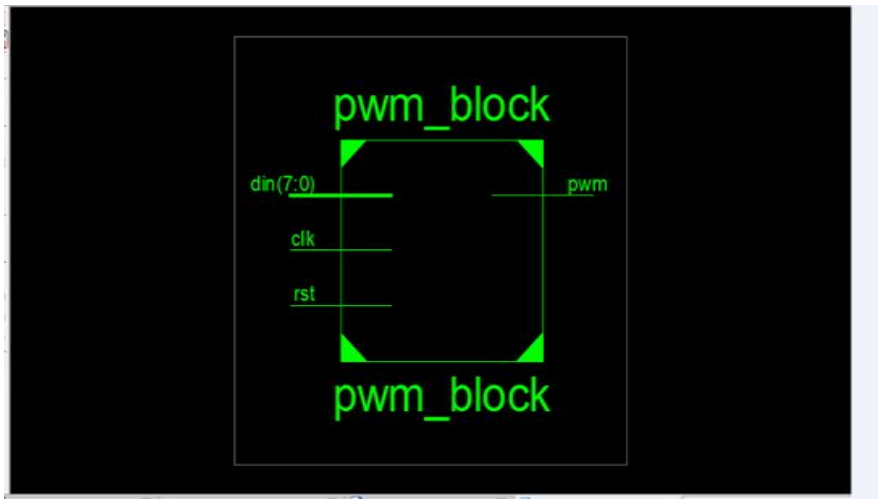

Fig.3 RTL view of PWM block

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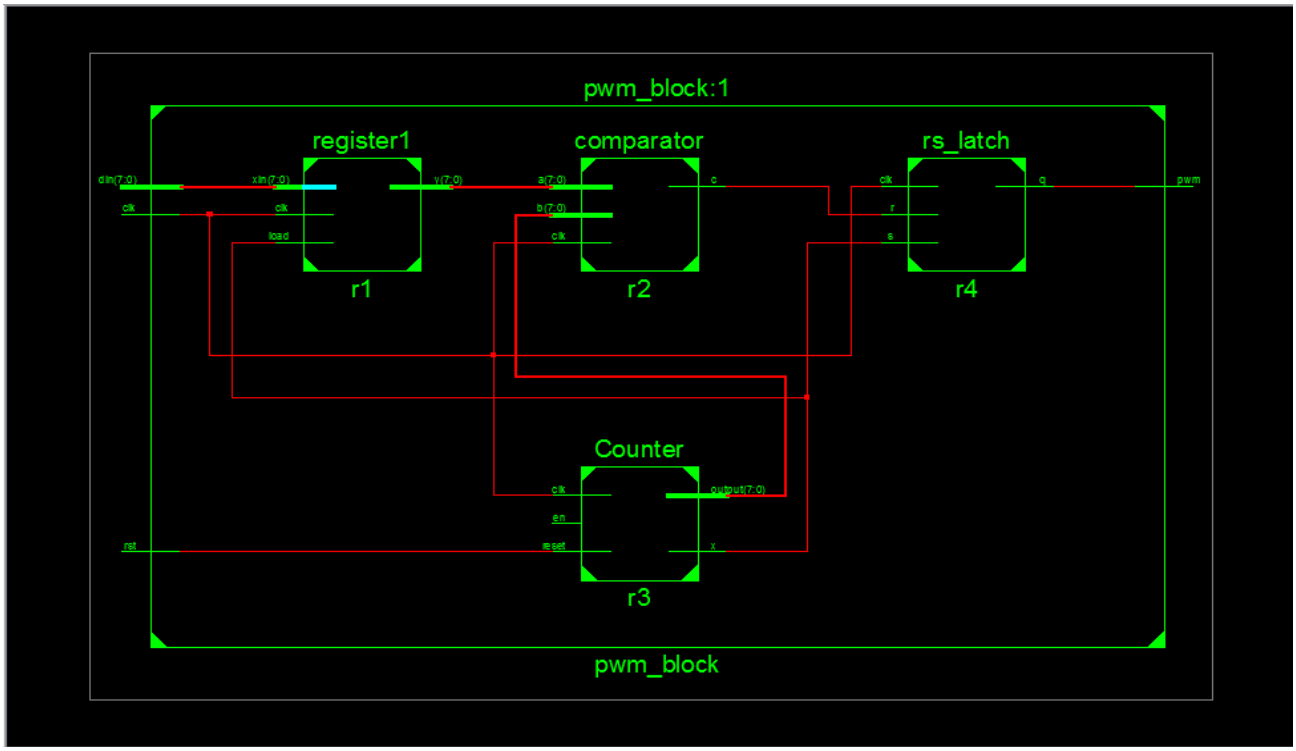

Fig.4 RTL view of PWM block

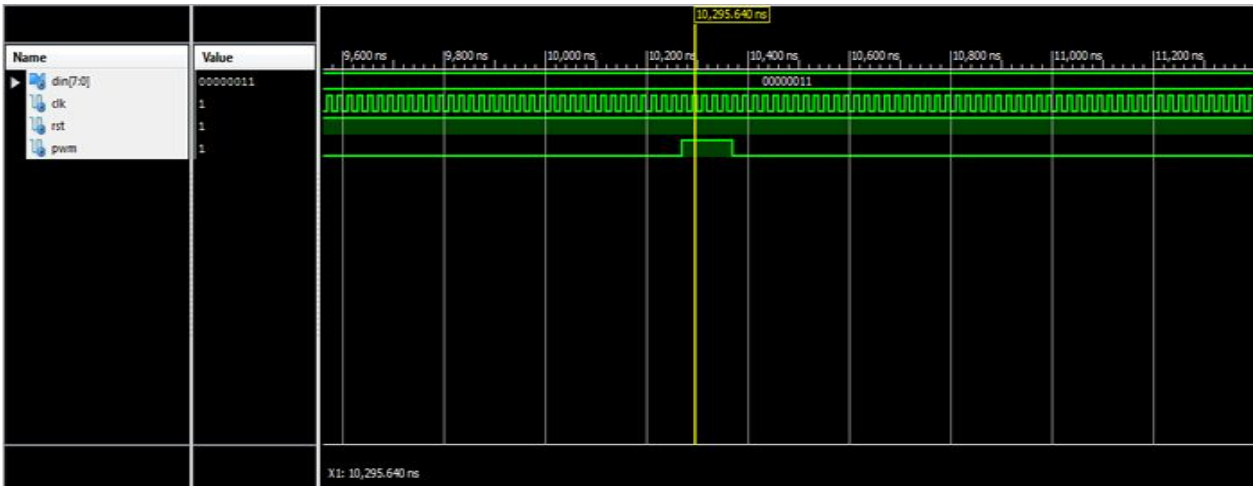

Fig.5 Simulated waveform when din=00000011

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Fig.6 Simulated waveform when din=00010001

V. CONCLUSION AND FUTURE WORK

Using Xilinx ISE Design Suite 13.1 software we can develop the proposed PWM in Xilinx FPGA. Due to the need of design flexibility in FPGA, an 8 bit resolution PWM was developed using VHDL modelingin Field Programmable Gate Array. The simulation results prove that using the proposed method, PWM frequencies up to 248.69 MHz can be produced with a duty cycle resolution of 0.39%. The VHDL modeling is used in the design process of PWM. Depending upon the application the requirement of the resolution is different. it is evident that higher values of N provide better resolution of the duty cycle, but performance should be taken into consideration when doing so. Future work should include high resolution of the duty cycle and high frequency application.

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BIOGRAPHY

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