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Implementation of FFT Processor using Urdhva Tiryakbhyam Sutra of Vedic Mathematics

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ABSTRACT:The FFT is a faster version of the Discrete Fourier Transform (DFT) and calculates Discrete Fourier Transform efficiently by reducing the computational complexity. It has low power consumption. It also reduces the area hence making the processor area-efficient.Fast Fourier Transform is an essential data processing technique in communication systems and DSP systems. In this brief, we propose high speed and area efficient 64 point FFT processor using Vedic algorithm. To reduce computational complexity and area, we develop FFT architecture by devising a radix-4 algorithm and optimizing the realization by Vedic algorithm. Furthermore, it can be used in decimation in frequency (DIF) and decimation in time (DIT) decompositions. Moreover, the design can achieve very high speed, which makes them suitable for the most demanding applications of FFT. Indeed, the proposed radix-4 Vedic algorithm based architecture requires fewer hardware resources. The synthesis results are same as that of theoretical analysis and it is observed that more than 15% reduction can be achieved in terms of slices count. In addition, the dynamic power consumption can be reduced and speed can be increased by as much as 25% using Vedic algorithm.

KEYWORDS:FFT, Vedic algorithm, DSP, radix-4,UrdhavaTiryakbhyam.

I. INTRODUCTION

Now a days, one of the important application of FFT is the orthogonal frequency division multiplexing (OFDM)[1]. It is mainly used in wireless local area network (WLAN), digital audio broadcasting (DAB), digital video broadcasting-terrestrial (DVB-T) and digital video broadcasting-handheld (DVB-H). Due to such diverse application of FFT, it is desirable to develop efficient FFT to meet the requirement of various OFDM communication standards [1]. The FFT is a faster version of the Discrete Fourier Transform (DFT) and calculates Discrete Fourier Transform efficiently in our work by reducing the computational complexity. Memory-based architecture is widely adopted to design an FFT processor. It consists of butterfly processing element and memory units. It has low power consumption but long latency and low throughput. To improve the efficiency of memory based FFT architecture, radix-4 butterfly processing units along with dual port memory is adopted.

With the advancement of VLSI, Fast Fourier Transform (FFT) is applied to wide field of digital signal processing (DSP) and communication system applications. The butterfly processing unit decides cost and characteristic of FFT processor. A butterfly unit is composed of complex adders and multipliers. The multiplier is usually the speed bottleneck in the design of the FFT processor [2]. If these complex multiplications are implemented using shift and add operation, it results in higher hardware cost and also, limits the performance of FFT[2]. To improve the performance of such complex computation Vedic algorithm is adopted. The benefits of Vedic algorithm for efficient implementation of complex multiplier have been largely unexplored. In recent years, several designs of FFT using Vedic algorithm have been proposed, but with the limited set of parameters.

VEDIC mathematics [3] is the ancient Indian system of mathematics which mainly deals with Vedic mathematical formulae and their application to various branches of mathematics. The word ‘Vedic’ is derived from the word ‘Veda’ which means the store-house of all knowledge. Vedic mathematics was reconstructed from the ancient Indian scrip-

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tures (Vedas) by Sri BharatiKrisnaTirtha (1884-1960) after his eight years of research on Vedas [3].This paper presents a simple digital multiplier architecture [3] based on the ancient Vedic mathematics Sutra (formula) called Urdhva-Tiryakbhyam(Vertically and Cross wise) Sutra which was traditionally used for decimal system in ancient India. In [3], this Sutra is shown to be a much more efficient multiplication algorithm as compared to the conventional counterparts.

Urdhva-Tiryakbhyam Sutra [4] is first applied to the binary number system and is used to develop digital multiplier architecture. This Sutra also shows the effectiveness of reducing the N×N multiplier [4] structure into an efficient 4×4 multiplier structures. This work presents a systematic design methodology for fast and area efficient digital multiplier based on Vedic mathematics [4].

In recent years, there has been some research in the design of multi-path pipelined FFT processors that provide a high throughput [5]. The area becomes even larger because the memory modules are duplicated for the 16 data path approach. In order to reduce the area and power consumption, several FFT algorithms and dynamic scaling schemes have been proposed [5]. The radix of the algorithm greatly influences the architecture of the FFT processor and the complexity of the implementation. A small radix is desirable because it results in a simple butterfly. Nevertheless, a high radix reduces the number of twiddle factor multiplications. The radix rk algorithms simultaneously achieve a simple butterfly and a reduced number of twiddle factor multiplications [5].

II. RELATED WORK

In order to reduce the area and power consumption, several FFT algorithms and dynamic scaling schemes have been proposed [5]. The radix of the algorithm greatly influences the architecture of the FFT processor and the complexity of the implementation. A small radix is desirable because it results in a simple butterfly.Nevertheless, a high radix reduces the number of twiddle factor multiplications. The radix rk algorithms simultaneously achieve a simple butterfly and a reduced number of twiddle factor multiplications [5]. The radix-2 algorithm is a well known simple algorithm for FFT processors, but it requires many complex multipliers. The radix-4 algorithm is primarily used for high data throughput FFT architectures, but requires a 4-point butterfly unit with high complexity.

One of the mentioned Sutras in the last subsection, UrdhvaTiryakbhyam (Vertically and Crosswise), deals with the multiplication of numbers. This Sutra has been traditionally used for the multiplication of two numbers in the decimal number system. In this paper, we apply the same idea to the binary number system to make it compatible with the digital hardware. The digits on the two ends of the line are multiplied and the result is added with the previous carry. When there are more lines in one step, all the results are added to the previous carry. The least significant digit of the number thus obtained acts as one of the result digits and the rest act as the carry for the next step. Initially the carry is taken to be zero.

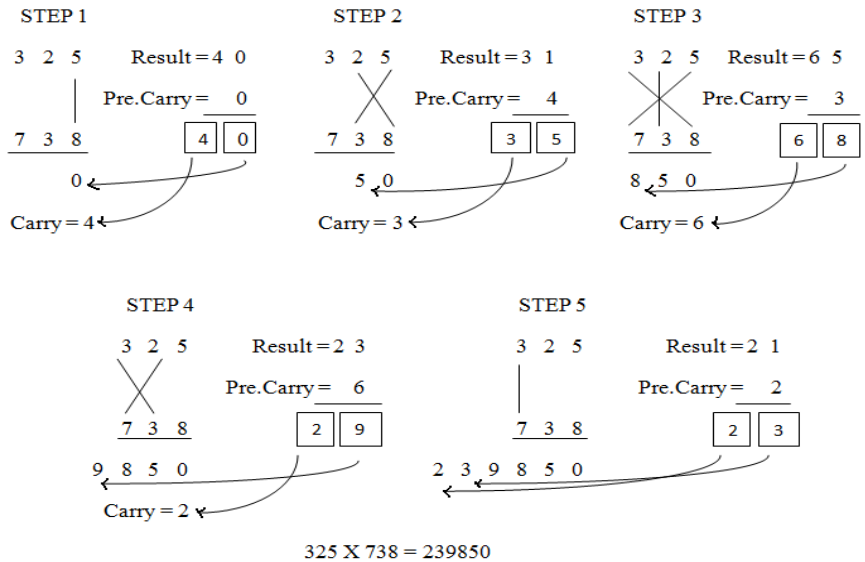

Fig. 1. 'Urdhva-tiryagbyham' method of multiplication.

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III.HARDWARE AND SOFTWARE DESIGN

A. Address Generation Unit (AGU):

The address generator performs memory addressing. The address generation unit controls the address bus going to memory. The FFT processor reads and writes from and to the 8 twin port memory banks concurrently. There are 8 read address buses, and 8 write address buses. They have two signals, "Start" and "Busy". The first one enables the processor to process the data and the second one indicates processing of data inputs [1]. The incoming data samples are partitioned into even and odd samples. After the assertion of the "Start" signal 64 input samples are clocked into the memory bank. A 6-bit counter controls the serial input of the data in the memory bank. Once all the data inputs are stored in memory bank, a signal "Busy" is asserted to process the data. AGU also controls the operation of selector unit by generating appropriate signals at a time. Initially, memory has the first 64 complex time samples. The butterfly unit selects four samples simultaneously and processes them and outputs the results in the same memory location. The butterfly unit is then given four more samples from memory banks. This process is repeated 16 times (for a 64-point FFT) until all the inputs in memory banks are depleted.

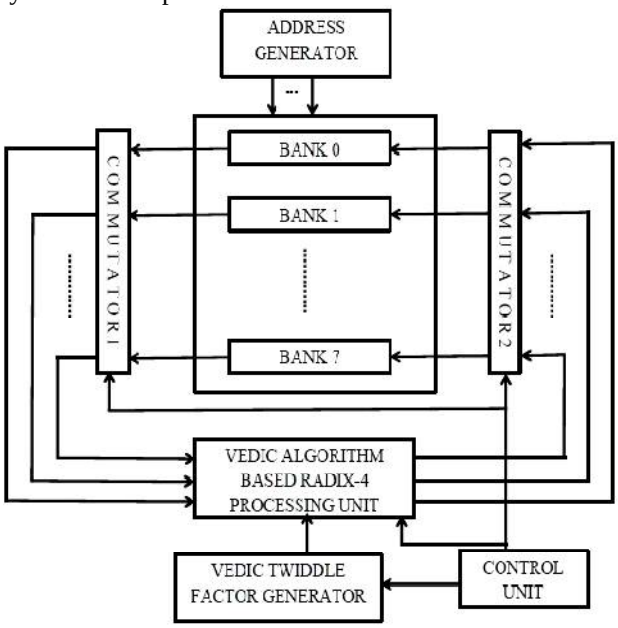

Fig. 2. Architecture of 64-point FFT using Vedic algorithm.

B.Radix-4 Butterfly Unit using Vedic Algorithm:

To perform 64-point FFT a single 4-point FFT unit is recursively used. This 4-point FFT is designed using high speed radix-4 algorithm. Moreover, the performance of FFT is limited by arithmetic operation such as complex multiplication. Complex multiplication of two numbers requires 4 multipliers, 2 adders and 1 subtractor or 3 multiplier and 5 adders. This large number of multipliers degrades the performance of FFT [2]. Vedic algorithm is an ancient and well known technique for arithmetic operation. The method which is used for multiplications is 'Urdhva-tiryagbhyam' which means vertical and crosswise. In this way, this algorithm performs multiplication of two given numbers in vertical and crosswise manner until left with only MSB bits. The proposed FFT utilizes Urdhva-tiryagbhyam method of Vedic algorithm to perform complex twiddle factor multiplications.

C.Twiddle Factor Generator:

The twiddle factors are generated using Vedic algorithm based Coordinate Rotation Digital Computer algorithm (CORDIC). CORDIC is a popular technique for computing trigonometric and exponential functions [2]. It performs rotation of a vector through some angle, specified by its coordinates. To eliminate the need of ROM to store twiddle factor, proposed FFT uses CORDIC to generate various values of twiddle factor. It uses two mode, rotation mode and vectoring mode. In rotation mode, the rotation by -45 degrees and the other by -135 degrees is obtained.

D. RAM:

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A memory unit is composed of 8 dual-port memory banks which facilitate 8-way parallel data access [2]. Each memory bank is 8-bit wide. From memory perceptive, in- place memory scheme is adopted so as to minimize the hardware resources and speed up the memory access time. For radix-r FFT, r banks of memory are needed to store data, and each memory bank could be dual-port memory. With "in-place" strategy, the r outputs of the butterfly can be written back to the same memory locations of the r inputs, and replace the old data.

E.Commutator:

The Commutator is one type of a switch that ensures efficient data routing mechanism. It consists of 8-to-1 MUXs [2]. It performs following functions. Commutator 1 routes the butterfly outputs to appropriate memory banks. These memory bank outputs are routed to proper 4-point butterfly inputs according to the control signals obtained from address generation unit. Commutator 2 is responsible for routing the input data to proper memory bank during FFT input period. It is also responsible for routing the memory output data to proper output.

IV. RESULT AND DISCUSSION

An efficient 64 point FFT module was designed using Vedic multipliers and modified adder and simulated using VHDL.FFT utilizing modified wallace multiplier and regular carry select adder was also simulated to compare the performances in terms of area and speed. Both the designs were implemented using the Sparten 3E and their synthesis reports were analyzed. Fig 3 shows the simulation of the testbench which was developed to test and verify the 64 point FFT. The values were verified with Matlab output. The 32 bit inputs are entered in both cases and the product and sum is verified respectively. The conclusion proves that our proposed system is better in terms of area and speed compared to the existing FFT processors.

For implementation of Braun Multiplier we are using Xilinx Integrated Software Environment (ISE). We are using Xilinx ISE 8.1i Project Navigator. The Xilinx Integrated Software Environment (ISE) consists of a set of programs to capture, simulate and implement digital hardware designs in a FPGA [5]. We use the Xilinx ISE 8.1i Project Navigator GUI for this work to help us visually manage and automate the entire design process with the aid of toolbars, menus or icons.

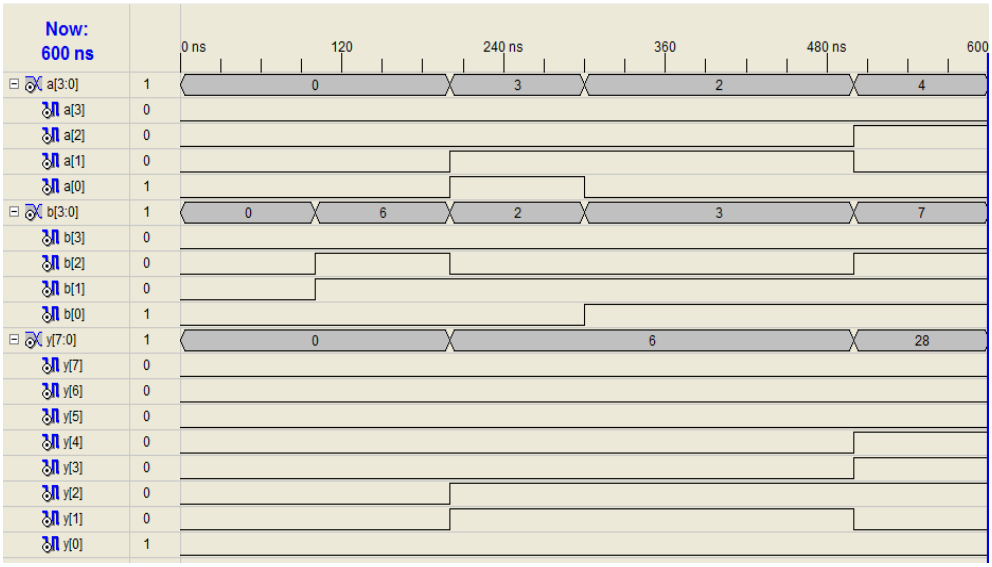

Fig.3 Test Bench waveforms for VedicMultiplier

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TABLE I
COMPARISON BETWEEN SYNTHESIS REPORTS OF PROPOSED AND CONVENTIONAL FFT

FFT Type	Number of Slices	Minimum period (ns)	Maximum combinational path delay (ns)
Proposed Vedic FFT	428	6.670ns	2.655ns
Conventional FFT	834	9.718 ns	3.745ns

V.CONCLUSION

Implementation results prove that the proposed FFT led to 26% area reduction and 25% speed improvement when compared with conventional FFT. This design had a maximum clock frequency of 95.2MHz. Such a 64-point FFT implemented using Vedic concepts and modified adder was found to have a good balance between performance and hardware requirements and is therefore most suitable for use in OFDM. Also, area minimization is obtained by devising an efficient Vedic algorithm based butterfly processing structure, while the novel twiddle factor multiplier has low power consumption and hardware complexity. Synthesis results show that the proposed FFT processor can provide up to 380.51 MHz speed and slices count is 373. The proposed FFT architecture can also be altered to support other longer FFT sizes. The main applications of this proposed FFT are in Digital Signal Processing, OFDM Systems, Digital Image Processing and Communication systems.

REFERENCES

1. Nisha John, Prof. Sadanandan G.K, "FPGA Implementation of a Novel Efficient Vedic FFT/IFFT Processor For OFDM", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 3, Issue 3, September 2014.
2. More T.V. ,Panat A.R. "FPGA implementation of FFT using vedic algorithm", Computational intelligene and Computing Research(ICCIC),pp-1-5,2013.
3. Harpreet Singh Dhillon, AbhijitMitra, "A Digital Multiplier Architecture using UrdhvaTiryakbhyam Sutra of Vedic Mathematics",IITG , pp-1-4,2010.
4. A.RonishaPrakash, S.Kirubaveni, "Performance Evaluation of FFT Processor Using Conventional and Vedic Algorithm", IEEE International Conference on Emerging Trends in Computing, Communication and Nanotechnology, pp-1-6,2013.
5. AsmitaHaveliya, "FPGA implementation of a Vedic convolution algorithm", International Journal of Engineering Research and Applications, Vol. 2, Issue 1, pp.678- 684,Jan-Feb 2012.