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DC–DC Buck Converter with Three-Level Zvsactive Clamping

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ABSTRACT: Buck regulator is the switching mode regulator to convert, unregulated dc voltage to a regulated dc voltage. This paper presents the study of a dc-dc buck converter with 3 level buck clamping, zero voltage switching active clamping, and constant-frequency pulse width modulation (PWM).

KEYWORDS: Buck, dc–dc converter, pulse width modulation (PWM), soft switching, three levels**.**

I. INTRODUCTION

BUCK-TYPE dc–dc converters are widely employed dc–dc converters in the world because no other topology is as simple. Their applications range from low-power regulators [1] to very high power step-down converters, [2] which are characterized by a low number of components, low control complexity, and no insulation. The conventional buck-type Topologies have low efficiencies because of high conduction losses [3][4] due to high-voltage-rated devices and high switching losses. The main parameters that impose limits on a buck converter with high-frequency pulse width modulation (PWM) operation are the junction capacitances of the semiconductors, parasitic inductances, and the reverse recovery of the diodes. To minimize these effects, many soft-switching techniques are employed. Soft-switching techniques typically increase the Current and/or voltage stresses in the semiconductor devices. Zero-voltage switching (ZVS) techniques [4-16] typically increase the voltage stress of the active

switches, and zero-current switching (ZCS) techniques increase current stresses. This condition is considered as the starting point of this paper, where the concept is to be ex-tended to a three-level version. In a buck converter topology employing a two-level ZVS buck-type active clamping circuit was introduced. However, this topology allows for ZVS in the turn-off switches, thus providing a higher efficiency at higher switching frequencies. An analysis of the two-level ZVS active clamping techniques pro-posed in shows that the two-level ZVS buck–buck converter is the only topology that limits the maximum voltage across the switches to the same level that is obtained in a conventional buck converter. This is the main reason for choosing three-level buck-type clamping for further study in this paper.

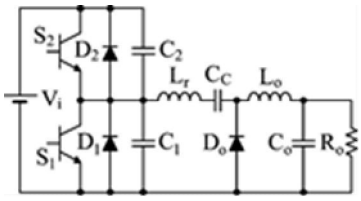

Fig. 1. Two-level ZVS PWM buck–buck converters

Three-level buck non isolated dc–dc PWM converters are used to reduce the voltage across the switches. Even though these converters operate at constant switching frequency, they do not feature soft switching. Compared to the conventional buck converter, the theoretical maximum voltage across theactive devices in is higher than half of the input

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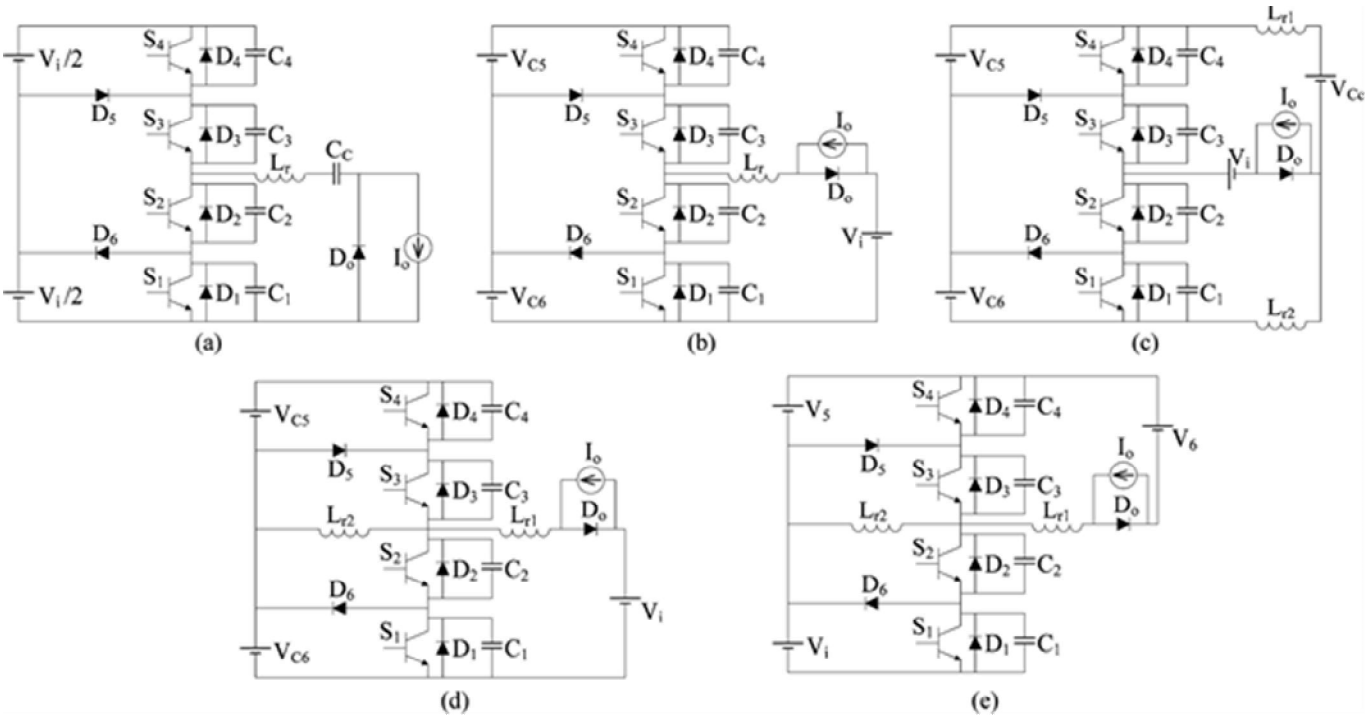

fig2: Buck converter using different three level converter for active clamping (a) Buck–buck.

(b) Buck–boost. (c)Buck–cuk. (d)Buck–sepic. (e)Buck–zeta

voltage. Thus, the proposal and analysis of a three-level buck-type converter with soft switching is presented in the following sections, where a family of distinct three-level ZVS active clamping Techniques applied to the dc–dc buck converter is presented. The different clamping strategies are compared, and the selection of three-level ZVS buck-type clamping for the buck converter is justified. The advantage of employing the three-level ZVS clamping proposed in this paper is the reduction of the maxi-mum voltage across the active switches by 50% compared to other two-level ZVS topologies Or to reduce the voltage stress of the switches, the three-level ZVS topology uses two active switches in addition to those included in other two-level ZVS topologies.

II. THREE-LEVEL ZVS PWM BUCK CONVERTERS

A family of buck-type converters is presented in Fig. 2, where different active clamping strategies are employed in order to achieve soft switching and blocking voltage reduction. In Fig. 2, index i relates the source to the input port and o relates the source to the output ports of the converters. The three-level soft-switching active clamping cells are classified according to the basic topology from which they are generated, and whichare introduced in[6].The input-to-output characteristics, referred to here as static gains, and the basic waveforms of the converters shown in Fig. 2 are the same as those for the two-level converters presented in[5][6].An example of these characteristics is shown in Fig. 3. Furthermore, the two-level buck–boost, buck–cuk, buck–sepic, and buck–buck–boost converters present the same input-to-output ratio as given in

$\frac{V_O}{V_i}$ = q = D − 2Ln(1) where D is the duty cycle, and Ln denotes the normalized output current that has no dimension and is given by

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$$L_n = L_r \frac{I_0 f_s}{V_i} \quad (2)$$

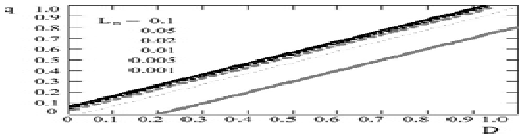

Fig. 3. Input-to-output voltage characteristic of the buck–boost converter.

Among the topologies that present the same static gain, the buck–boost converter presents a lower component count and the same or better functionality as the others. The transfer function of the buck–buck converter is given in the next section, while the static gain for the buck–zeta is

$$\frac{V_O}{V_i} = q = \frac{D}{1-D} - \frac{2L_n}{(1-D)[2L_n + (1-D)]} \quad (3)$$

⇒ buck–zeta.

Zeta-type clamping features ZVS operation throughout the complete load range. However, this type of clamping results in application of a high voltage across the active switches. There-fore, based on the comments made in Section I, the buck–zeta converter is not considered further. Boost-type clamping is advantageous because of the lower duty cycle loss. The main drawback of this technique is the dependence of the maximum voltage across the switches on duty cycle and power variations. Buck-type clamping features a maximum voltage across the active switches that are independent of any design parameter. The voltage across the switches is theoretically clamped to half ofthe input voltage.

III. THREE-LEVELBUCK– BUCKCONVERTER

For the reasons given in Section 2, the topology analysed in this section is the buck–buck converter. Fig. 4 presents the commutation cell for the three-level buck–buck converter and its basic circuit configuration. In order to ease the understanding of the converter's operation, the following assumptions are considered.

1) Switches are ideal.
2) The converter operates in steady state.
3) The output inductance Lois such that, in conjunction with output voltage Vo, it can be represented as an ideal current source (Io).
4) The resonant inductor Lr stores sufficient energy to complete the charging and discharging of the resonant capacitors C1, C2,C3, and C4(Fig. 4), with value Cr, during the switching transitions and to polarize the intrinsic diodes of the switches.
5) The passive components are considered free from parasitic effects.
6) The auxiliary bus capacitance CC is much larger than Cr and is capable of keeping the voltage unchanged during a switching cycle. Thus, the auxiliary bus capacitors can be represented by voltage sources.

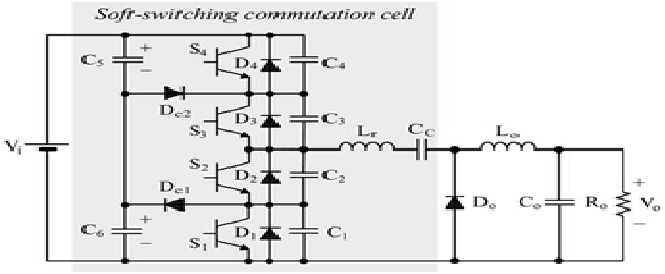

Figure. 4:Three-level ZVS PWM buck–buck converter.

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A. Converter Operation

Depending on the intervals between the turn-off of the switches and the value of the resonant capacitors (Cr), the converter can operate in nine different operation modes.For all cases, the converter operates under ZVS, maintaining its static-gain characteristic. The differences are noted only in a few operation stages for very short durations. In order to simplify the stages, the voltages across capacitorsC5 and C6are considered balanced and equal to Vi/2. The resonant capacitor is chosen so that Cr> Cr limit If a voltage imbalance across capacitors C5andC6were considered, the number of operation stages would increase, but the ZVS of the four transistors would be maintained The description of the operation stages is summarized shortly, and they are shown in Fig. 5

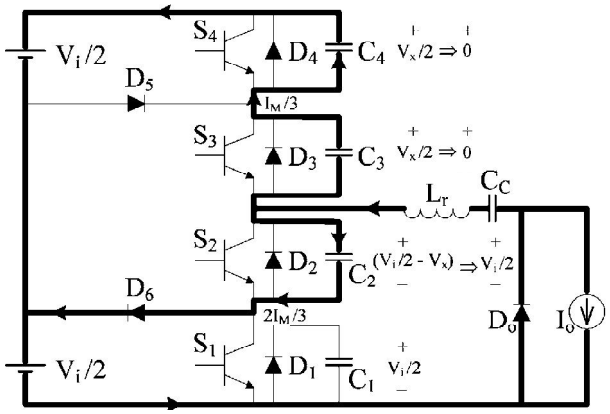

Figure 5: Operation stages of the three-level ZVS buck–buck converter.

There are 12 stages of operation. In First stage [t1–t2]: The Switches S1and S2are ON. The current through inductor Lris negative. Diode Do is forward-biased. In Second stage [t2–t3]: Switch S1is turned off, but S2is ON. The current is divided between the resonant capacitorsC1, C3, and C4.. The voltage across capacitorC1increases from zero to Vx (cf., Fig. 7), which is less than Vi/2, and the voltages across C3and C4decrease from Vi/2to (Vi/2 − Vx/2). Voltage Vx depends on the interval between the turning off of switches S1and S2.In Third stage [t3–t4]: SwitchS2 is turned off, and the current through the four resonant capacitors is IM/2.When the voltage across capacitorC1 reaches Vi/2.In Fourth stage [t4–t5]: A current division becomes positive and switches S3and S4start to conduct In Fifth stage [t5–t6]: Diodes D3and D4are forward-biased. Thesediodes conduct the current through inductor Lr. In Sixth stage [t6–t7]: The resonant inductor current becomes positive and switches S3and S4start to conduct. Seventh stage [t7–t8]: starts when the resonant inductor current equals Io. The diode Do is reverse-biased. In thisEighth stage[t8–t9], S4 is turned off and the voltage acrossC4increases from zero to Vx, and depends on the interval between the turn-offs of switches S3and S4. When switchS3turns off, the next operation stage begins. Occurs as in the second stages. This stage ends as the voltages across capacitors C3and C4reach zero. In Ninth stage [t9–t10]: The current through the four resonant capacitors is ILr/2.when the voltage across C4 reaches Vi/2 the stage ends. Tenth stage[t10–t11]: The voltage across C1and C2 continues to decrease until it reaches VC c/2. In this Eleventhstage [t11–t12]: diode Do is forward-biased.Twelfth stage [t12–t1]: Diodes D1and D2are forward-biased and conduct the resonant inductor current. After this stage, the circuit is ready to return to first stage again. Fig. 7 presents the main waveforms of the converter, and the preceding description is considered for a single switching cycle. Each operation interval is described using this figure. From the analysis, the necessary condition for ZVS to occur is that the switch is turned on only when its parallel capacitor is discharged. In other words, to achieve zero losses in the Switching intervals, the drive signals of switches S1and S2 (VG 1, G2) should transition between t12and t1, and the drive signals of S3and S4 (VG 3, G4) should transition betweent5andt6. The voltage Vxof Fig. 7 is smaller than VC c/2 and depends on the turn-off intervals.

B. Static Gain Characteristic

To simplify the derivation of the input-to-output voltage gain characteristic, the very short time intervals (between t2and t5 and from t8to t11) are neglected in the following. Fig. 6 can be redrawn as shown in Fig. 7.Note that duty

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cycle D is defined as the interval between the turn-offs of switches S1and S2and the turn-off of switches S3andS4. Based on assumptions, the static transfer characteristics of the two- and three-level buck–buck converters are the same. The average current through capacitor CC, iCc, is computed

$$i_{Cc}(t)=i_{Lr}(t)=\int_0^{\Delta 1}\left[\frac{(V_i-V_{cc})}{L_r}t+I_M\right]dt$$

$$+\int_0^{DT_s-\Delta 1}(I_O)dt+\int_0^{(1-D)Ts}\left[\frac{-V_{Cc}}{L_r}t+I_0\right]dt=0 \quad (4)$$

Where

$$I_M=I_0-\frac{V_{Cc}}{L_r}(1-D)T_s \quad (5)$$

and

$$\Delta 1=\frac{(I_M+I_O)L_r}{(V_i-V_{Cc})} \quad (6)$$

The normalized load current or normalized resonant inductance “Ln” is defined by

$$L_n=L_r\frac{I_0}{V_iT_s} \quad (7)$$

The average value of the average current across CC is zero because the system is under steady-state operation. Thus, by integrating (5) and substituting (6)–(8) into (5), the expression for the relationship between voltages VCc and Vi is obtained

$$V_{Cc}=\frac{2L_nV_i}{2L_n+(1-D)^2} \quad (8)$$

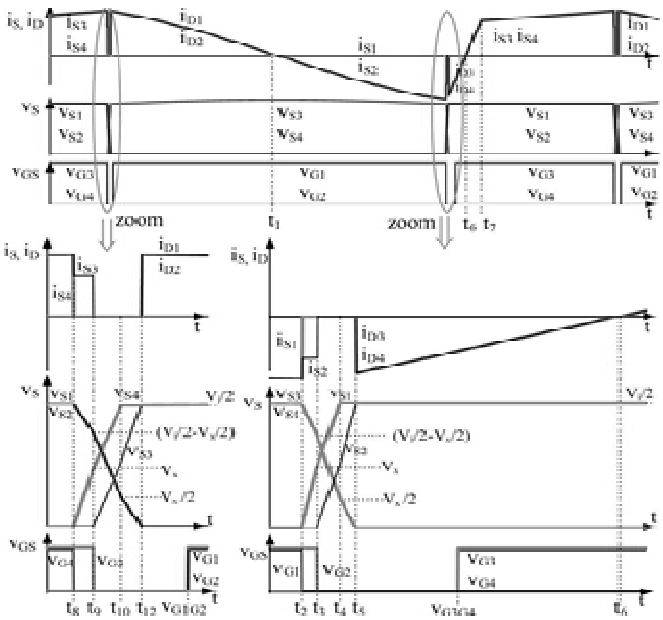

Figure6: Main waveforms of the three-level ZVS buck–buck converter

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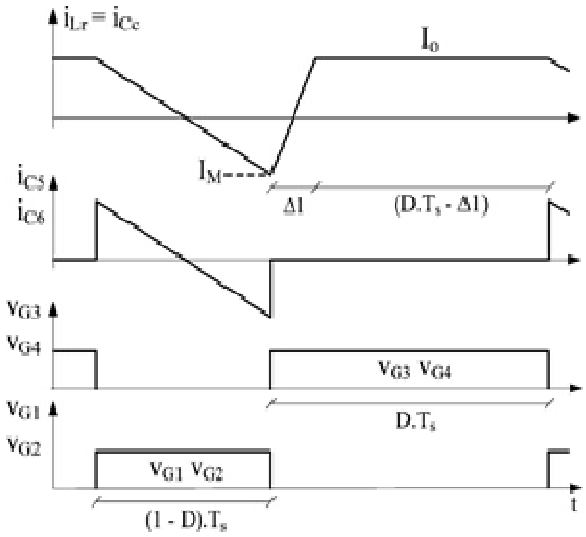

Figure7: simplified waveforms of the three level buck converter below:

The static gain is given by
Vo= DVi− VCc. (9)
If the system operates in steady state, the gain characteristic is obtained from the sum of the voltages since the average value of the voltage across inductor Lr is null.Defining the relationship between input and output voltage as

$$q = \frac{V_s}{V_i} \quad (10)$$

and substituting (9) and (11) into (10) gives

$$q = D - \frac{2L_n}{2L_n + (1 - D)^2} \quad (11)$$

IV. CONCLUSION

This paper has presented a family of high-efficiency buck-type dc–dc converters suited for high-voltage applications. The proposed converters combine the advantages of a reduction of the voltages across the switch, which was achieved using a three-level commutation cell, with decreased switching losses obtained from a ZVS technique. A comparison between the proposed topology and the two-level ZVS buck–buck converter shows that the voltages across the switches are 50% lower. The three-level converter provides two extra bidirectional current switches and an additional capacitor for the auxiliary bus when compared to the two-level converter even though the voltage ratings for these devices are halved as well. The three-level technique provides more gate driver circuits, thus illustrating another disadvantage of using two-level topologies. In a closed-loop application, the control of the two clamping voltages needs to be implemented, and, thus, requires more circuit complexity and extra voltage sensors. Consequently, the proposed converter is thought to be a suitable solution in applications where theswitch technology poses a limitation to the available voltageratings, no insulation is needed, and a high efficiency at highswitching frequencies is required. A further modification has been introduced to the proposedtopology for the achievement of ZVS operation for the output diode as well. The proposed buck–buck converter can be extended to corresponding insulated topologies (forward-buck) that are able to reduce the active switches' voltage ratings while providing ZVS. Further extensions are possible which generate five-level dc–dc converters that reduce the maximum switched voltages to 25% of the original forward

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topology. Another advantage of the forward-buck converter in relation to other converters, such as the forward- boost, is that capacitor Cc of the buck clamping circuit is already placed in series with the transformer, which prevents saturation of the capacitor. For three-level half-bridge and full-bridge converters with ZVS, the different types of three-level clamping solutions presented here cannot be directly employed.

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