ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2015

Settling Time Analysis of Thermometer Code Encoder by Mux's Combination

Akanksha Srivastava, Sonam Verma

Assistant Professor, Dept. of EEE, Lingayas University, Faridabad, Haryana, India.

VLSI Trainer, Real Time Signals Technologies, Bengaluru, Karnataka, India.

ABSTRACT: Settling time is an important parameter. It measures that how much time is required for stable output change. Comparator and thermometer coder encoder are responsible parameters of Flash ADC performance. In this paper, settling time of thermometer code encoder by mux combination is measured.
It is implemented on Cadence virtuoso tool.

KEYWORDS: ADC, Flash ADC, Thermometer code converter, settling time.

I. INTRODUCTION

Analog to digital converter works as a bridge to convert analog data into digital form. High speed ADC's are mostly used in signal processing applications. Flash ADC requires only one clock to process data. Flash ADC is the fastest ADC in all ADC. A chain of comparators and an encoder circuit is required in Flash ADC. To convert analog data in n no of digital code it requires 2^n-1comparators [1, 2]. In comparators a reference voltage is required which changes the analog particular input into high or low signal. A series of zeros for low signals and a series of ones for high signal is generated from the chain of comparators in flash adc. To convert series of zero and one an encoder system is required [6].

II. THERMOMETER CODE

As the series of zero and one by which continuation sequence of either zero or one is used to count input in digital number is thermometer code. In Flash ADC's the chain of comparators generate one and zero are one of thermometer code [7,8]. To convert thermometer code into digital code an encoder circuit is used. There are different circuits which converts thermometer code in digital as Wallace tree, combination of mux's [4] etc.

III. THERMOMETER CODE ENCODER BY MUX'S COMBINATION

Multiplexers are data selectors. They are parallel to serial converters. In mux, which data is to be transferred from input to output is selected by selection line. Figure 1 is the symbol of 2:1 mux. When Sel is zero B is transferred to z and at Sel is one A is transferred to Z.

$$Z = A.Sel + B\ Sel' \qquad [1]$$

To convert fifteen inputs (C1 to C15) into four output lines, total elever 2:1 mux's are required. In first series of seven mux's all inputs are passed form 2:1 mux's in which C8 work as selection line as well as output (X3). After seven mux's, outputs next series of three mux's are connected. Output of middle mux's is connected as selection line as well as output line (X2). Output line of second mux's series are connected in the input of mux. Middle od mux's output of second mux is work as an input line for last mux and as well as output line (X1). At the last mux's output is X0 decribe in figure 2.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2015

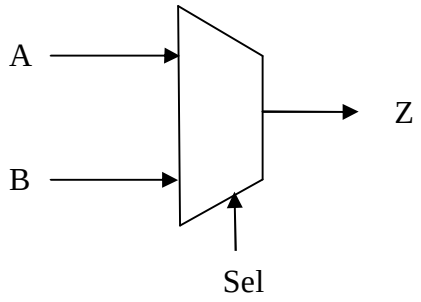

Figure 1 2:1 mux

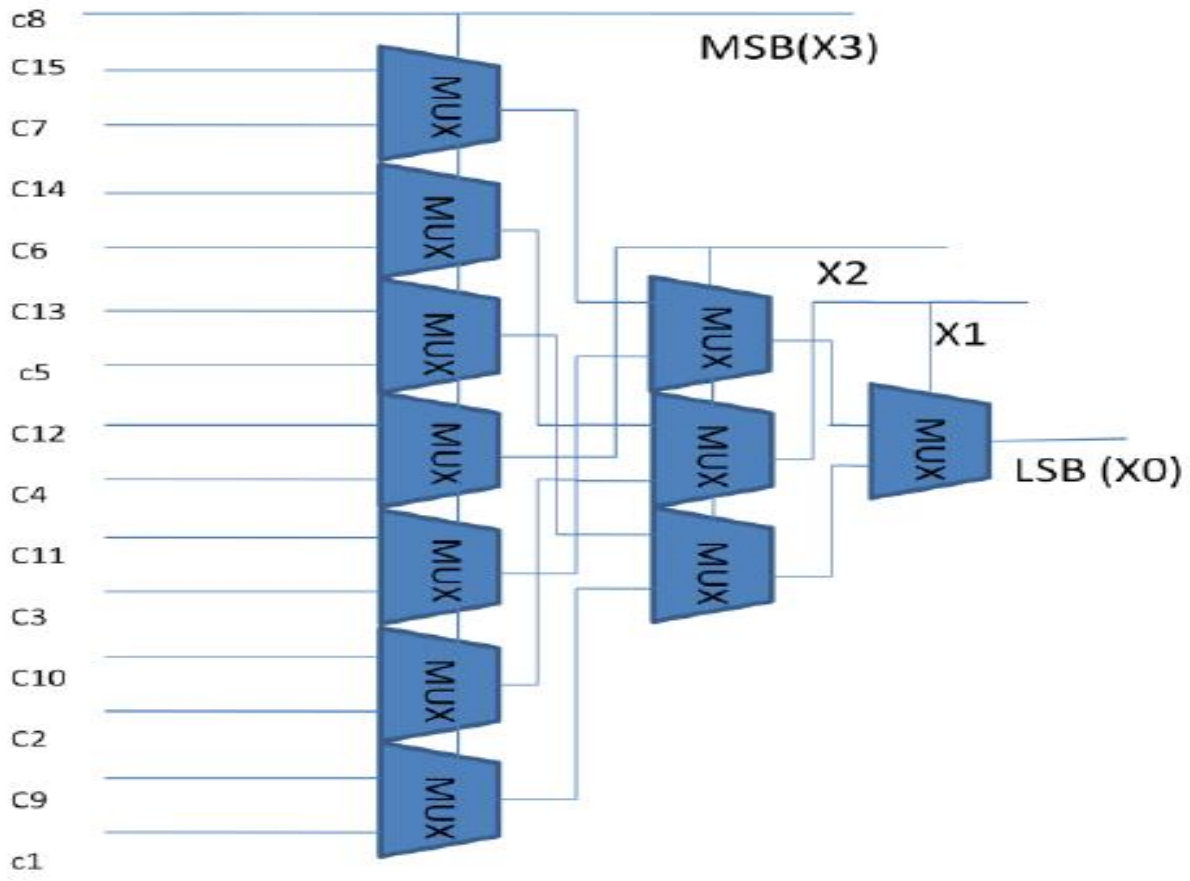

Figure 2 4 bit thermometer code encoder by mux's combination [3].

Table 1 is the truth table of 4 bit mux encoder system. C1 to C15 are inputs and X0 to X1 are outputs. Table 1 shows all the output for all possible inputs. Figure 3 is the snapshot of 4 bit mux encoder system implemented on cadence-virtuoso tool.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2015

C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	X3	X2	X1	X0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 1. 4 bit thermometer code encoder by mux's combination[3]

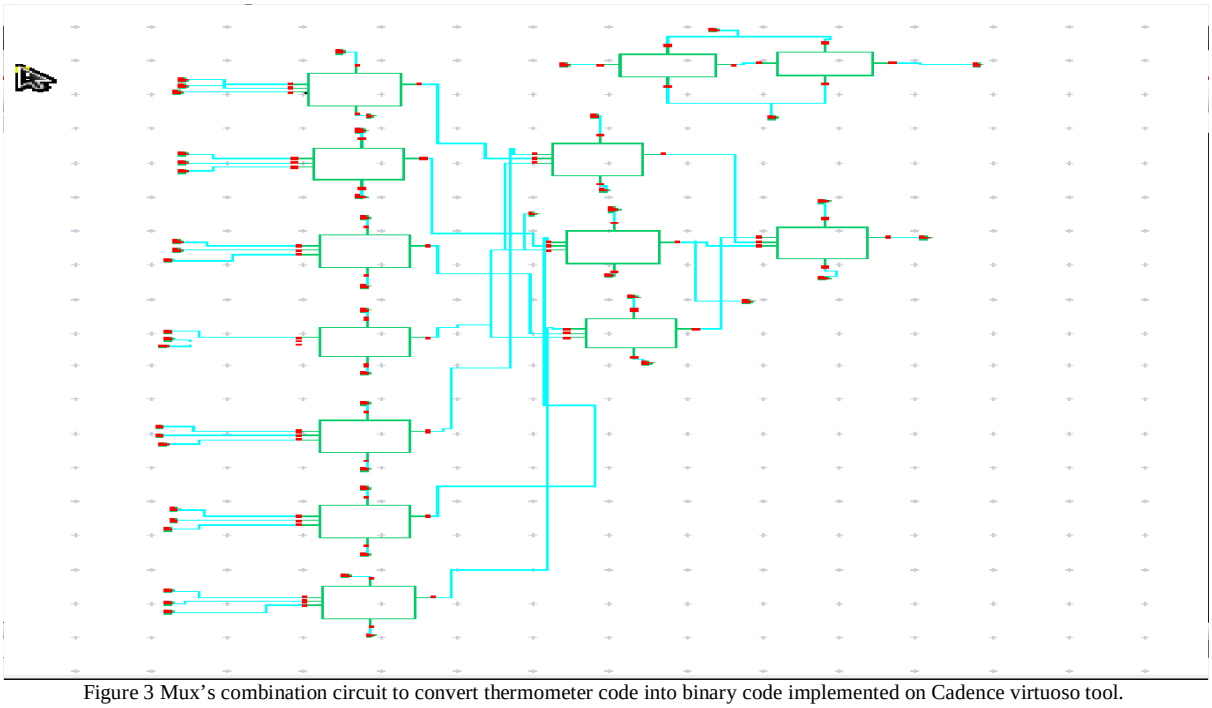

Figure 3 Mux's combination circuit to convert thermometer code into binary code implemented on Cadence virtuoso tool.

IV. RESULT ANALYSIS

The time required to stable the output when input is changed is called settling time. Settling time also includes propagation delay. It is the difference of the time to change from one state to another state.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2015

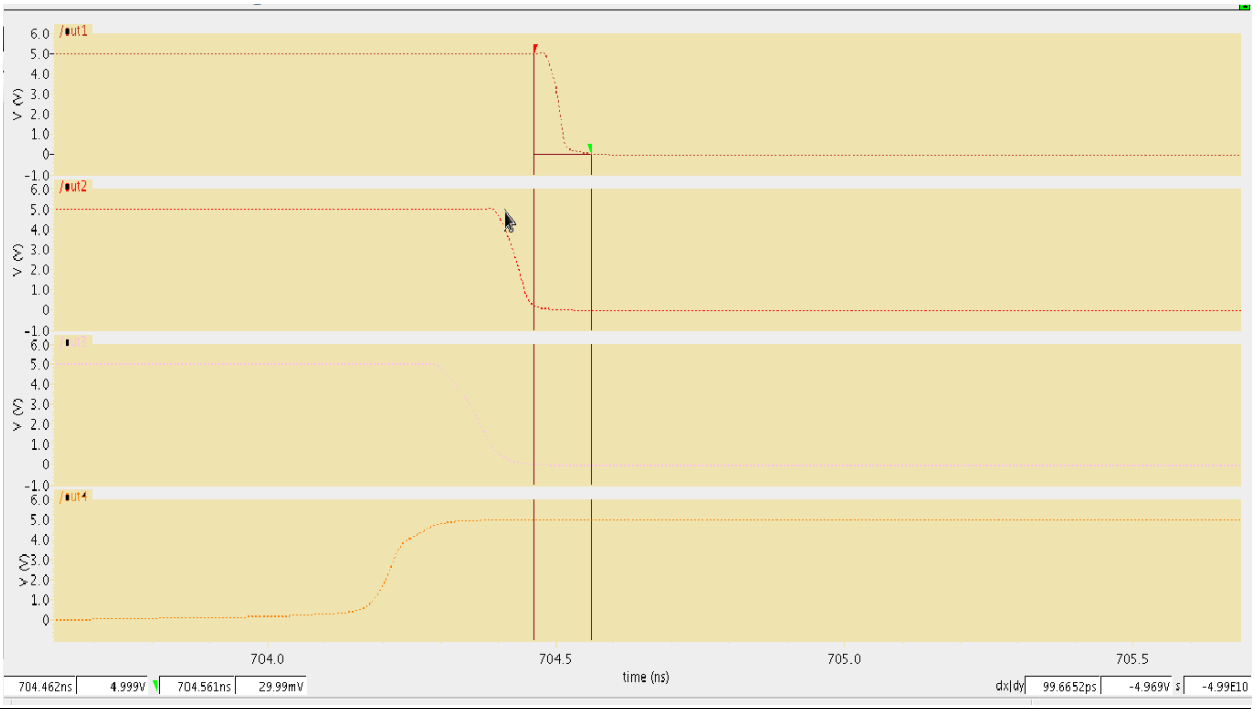

Fig 4 Output waveform timing is calculated for OUT1

Figure 4 is the output waveform of OUT1. In it the change of high to low is calculated. The time required to stable output change is 99.66ps.

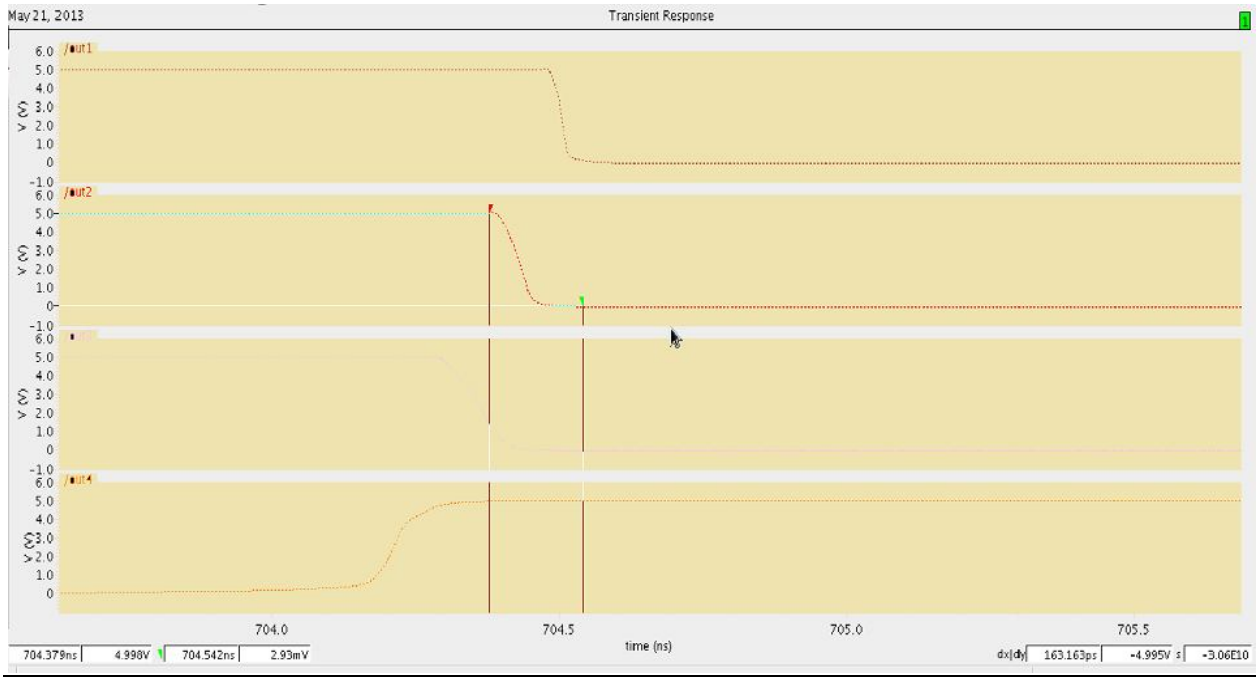

Fig 5 Output waveform timing is calculated for OUT2

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2015

Figure 5 is the output waveform of OUT2. In it the change of high to low is calculated. The time required to stable output change is 163.163ps.

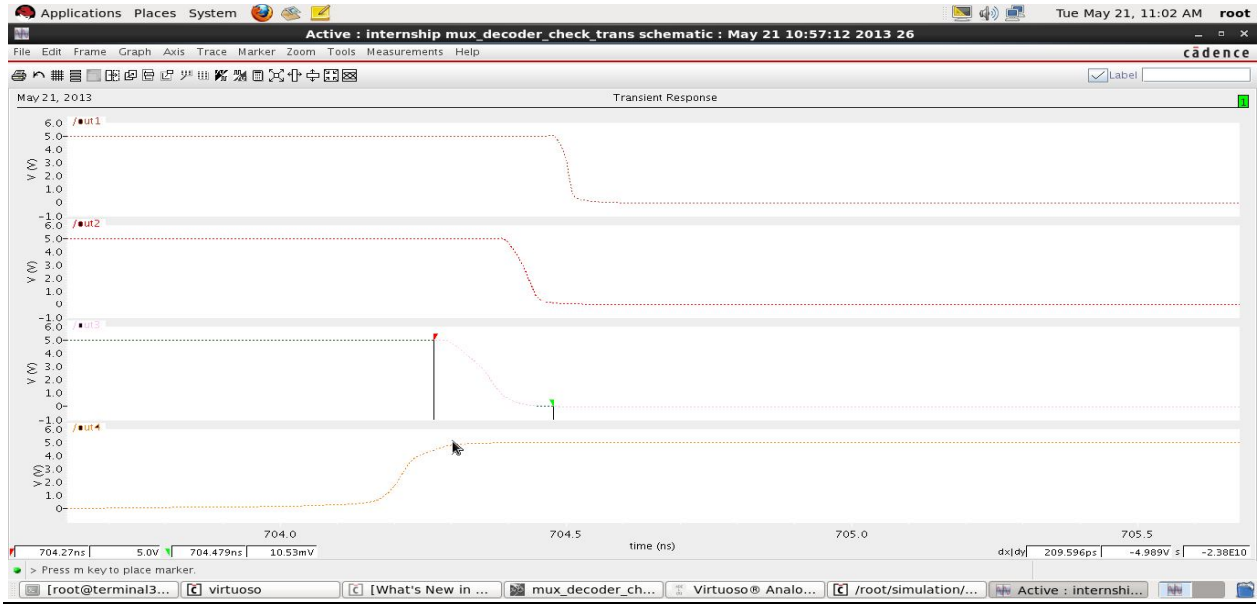

Fig 6 Output waveform timing is calculated for OUT3

Figure 6 is the output waveform of OUT3. In it the change of high to low is calculated. The time required to stable output change is 205.596ps.

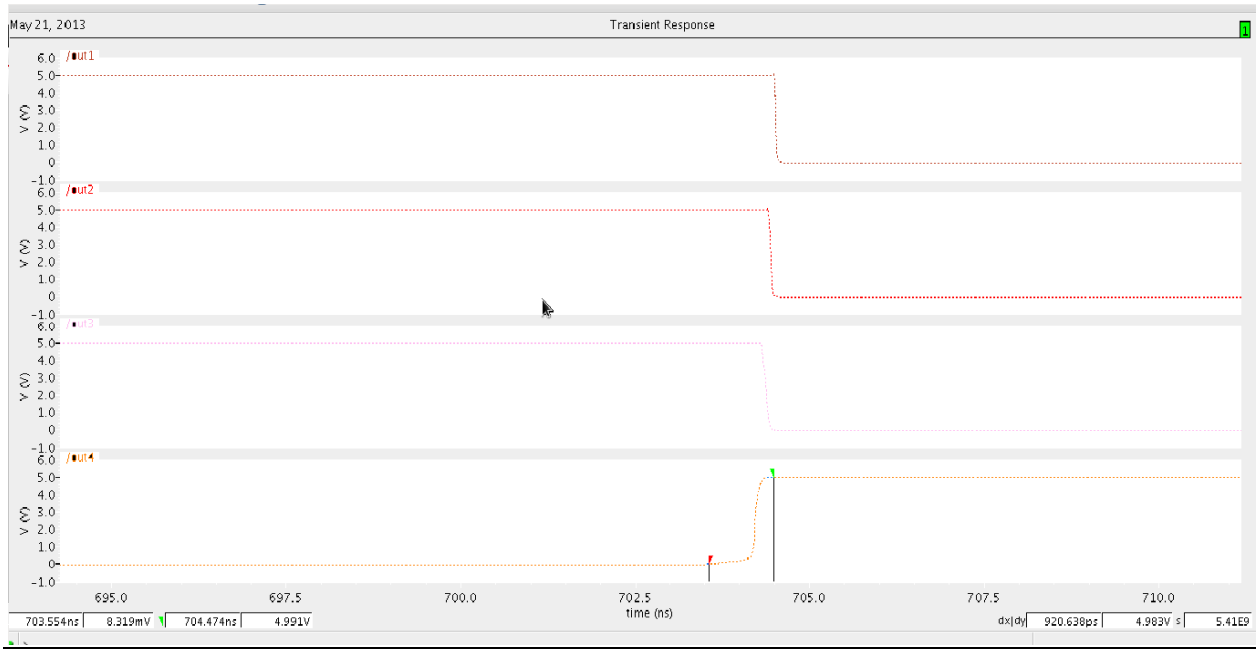

Fig 7 Output waveform timing is calculated for OUT4

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 6, June 2015

Figure 7 is the output waveform of OUT4. In it the change of high to low is calculated. The time required to stable output change is 920.638ps.

From figure 4,56,7 a final table is created. Total settling time required is .920 ns.

OUT	V1(V)	V2(V)	T1(NS)	T2(NS)	V(V)	SETTLING TIME T(nS)
Out1	4.999	29.9m	704.462	704.591	4.96	.099
Out2	4.998	2.93m	704.379	704.542	4.995	.163
Out3	5	10.53m	704.27	704.479	4.989	.209
Out4	8.319u	4.991	703.553	704.473	4.983	.920

Where V1 (v) is voltage and T1 (ns) is time in nano second at initial stage (before input is changed), V2 (v) is voltage and T2(ns) is time in nano second at final stage (after input is changed). V (v) is difference of V1 (v) and V2 (v) and T (ns) is time difference between T1 (ns) and T2 (ns). T (ns) is the settling time for output line.

REFERENCES

[1] Timmy Sundström," Design of High-Speed, Low-Power, Nyquist Analog-to-Digital Converters" Department of Electrical Engineering Linköping University, SE-581 83 Linköping, Sweden Linköping 2009 ISBN 978-91-7393-486-2 ISSN 0280-7971.
[2] B. Razavi, "Deign of Analog CMOS Integrated Circuits," Tata McGraw-Hill, Delhi, 2002.
[3] Arunkumar P Chavan Rekha G P Narashimaraja,"An Efficient Design of 3bit and 4bit Flash ADC", *International Journal of Computer Applications (0975 – 8887) Volume 61– No.11, January 2013*
[4] F. Kaess, R. Kanan, B. Hochet and M. Declercq, "New Encoding Scheme For High-Speed Flash ADC's," IEEE Proc.Circuits and Syst., vol. 1, pp. 5-8, June 1997.
[5] Erik Säll, Mark Vesterbacka and K. Ola Andersson "A STUDY OF DIGITAL DECODERS IN FLASH ANALOG-TO-DIGITAL CONVERTERS" unpublished.
[6] Channakka lakkannavar, Shrikanth k. Shirakol, Kalmeshwar n. Hosur design(2012). Implementation and analysis of flash ADC architecture with differential amplifier as comparator using custom design approach. International journal of electronics signals and systems (ijess) issn: 2231- 5969, vol-1 iss-3.
[7] B. Razavi, Principles of Data Conversion System Design, IEEE Press, 1995.
[8]K. L .Lin, T.van den Boom, Stevanovic. N, "Basic design guide for CMOS folding and interpolating A/D converters Overview and case study", IEEE International Conference on Circuits and Systems, vol.1, pp. 529 – 532, 1999.

BIOGRAPHY

Akanksha Srivastava is an Assistant professor in the Electrical and Electronics Department, Lingayas University, Haryana, India. She received Master of Technology (M.tech) degree in VLSI, 2014 from Amity University, Noida, India. Her research areas are ADC, VLSI, cryptology etc.

SONAM VERMA has completed her Bachelor of Engineering degree in ECE from Dronacharya College of Engineering, Greater Noida, affiliated to Uttar Pradesh Technical University, Uttar Pradesh, India in the year of 2012 and Master in Technology done with VLSI Design from Amity University, Noida, India in the year of 2014. Her research areas are ADC, VLSI, memory controller etc.