ISSN(Online): 2320 - 9801
ISSN (Print) : 2320 - 9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2016

FPGA Implementation of CORDIC for FFT Applications

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ABSTRACT: This paper presents a FPGA implementation of Coordinate Rotation Digital Computer(CORDIC) for FFT application implemented in pipeline architecture to generate sine and cosine angles. CORDIC is a grouping of only additions and shifts. It can be efficiently implemented hardware.the proposed algorithm further approximates the way of computing rotation angle based on FFT in order to reduce the usage of Read-Only-Memory(ROM)table and improve the speed. The coding is done using Very High Speed Integrated Circuit Hardware Description Language (VHDL) and synthesis is done using Xilinx 14.5 on Spartan 6 Board. The proposed CORDIC was compared with existing CORDIC to obtain minimized number of slice LUT's, improve speed of execution and angle rotation increases.

KEYWORDS: CORDIC, FFT, SHIFTER, FPGA, VHDL, LUT.

I. INTRODUCTION

CORDIC or Coordinate Rotation Digital Computer is a simple and hardware efficient algorithm for the execution of different elementary, especially trigonometric, functions. instead of using calculus based methods such as polynomial or rational functional approximation, it uses simple shift, add, subtract and table look up operation to achieve the objectives. CORDIC(Coordinate Rotation Digital Computer) also known as the digit by digit method and volder's algorithm, it is a simple and efficient algorithm to calculate hyperbolic and trigonometric functions. It is commonly used when no hardware multiplier is available such as simple microcontroller and FPGA's as the only operations it need are addition, substraction, bitshift and table lookup. The beauty of CORDIC is its potential for unified solution for a large set of computational tasks involving the estimate of trigonometric and transcendental functions, calculation of multiplication, division, square-root and logarithm, solution of linear systems, QR-decomposition, and SVD, etc. Moreover, CORDIC is implemented by a simple hardware during repeated shift-add operations. Latency of computation, however, continues to be the major problem of the CORDIC algorithm, since they do not have competent algorithms for its parallel implementation. But, CORDIC on the other hand is naturally suitable for pipelined designs, due to its iterative behaviour, and small cycle time compared with the conventional arithmetic. For high throughput applications, efficient pipelined-architectures with multiple-CORDIC units could be developed to take the advantage of pipeline ability of CORDIC, because the digital hardware is getting cheaper along with the progressive device-scaling. Another way to use CORDIC efficiently, is to transform the computational algorithm into independent segments, and to implement the individual segments by different CORDIC processors.

II. LITERATURE SURVEY

Milos D.Ercegovac [1] Presented several modifications to the CORDIC method in order to improve speed and efficiency of its implementation. the main contributions are 1)The introduction of redundant (Carry -free) addition to replace time-consuming conventional additions 2) the use of on-line arithmetic to reduce the communication bandwidth, maximize the overlap between successive operations, and replace area –expansive shifters by delays. No attempt has been made at this time to estimate the savings in the area since no VLSI realizations are done. Ren-xi Gong et al., [2] proposed that the designing of a CORDIC algorithm based radix-4 FFT processor is primarily intended to be used in power harmonic signal processing. the processor is implemented in field programmable gate array and it is

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characteristics of high efficiency, low cost, convenient implementation and short development cycle .for realizing the basic butterfly operation for the FFT the CORDIC algorithm does not need storing twiddle factors and angles saves a lot of hardware compared to its counterparts employing other techniques. pooja choudhary et al., [3] modified that there is reduction in area and power. The FFT processor based on CORDIC is implemented .the key idea is replacing the sine and cosine twiddle factors in conventional FFT architecture by iterative CORDIC rotations which allow the reduction in Read-only memory. the use of CORDIC in FFT results it provides a complex multiplication but they realized that complex multiplier is not efficient in terms of area and power. Huan li et al., [4] proposed that in this method it reduce the hardware costs and improve operational performance because to modify they just needs a simple shift and add-subtract to achieve the calculation of multiple transcendental function. pramod meher et al., [5]are proposed two area –efficient algorithms and architectures on CORDIC such as 1) algorithm eliminates ROM and requires only low-complexity barrel shifters. 2)it eliminates barrel shifters completely.both the algorithms devour a lower percentage of FPGA device components in compare to preceding algorithms. shaoyun wang et al., [6] provide a wide spectrum of architectures, a coordinated and full design and complexity, the figures of merit characterizing architectures performance. Javier valls et al., [7] they show that redundant arithmetic operators require a 4 to 5 times larger area than the conventional ones. on FPGA implementation the speed advantages of the full-custom design has been lost due to the longer routing delays caused by the increase of the fan-out and the number of nets of the operator. Nihel neji, et.al [8] proposed in this paper a low cost sequential architectures for the implementation of CORDIC algorithm in two computation modes such as sin/cos, sinh/cosh and arctan. It suited for serial operation that performs conversion between polar and rectangular coordinates systems. To reduce iteration delay we used some combinatory blocks. kailash Chandra ray [9] proposed that windowing techniques are widely used for preprocessing of samples before FFT in real time spectral analysis to minimize spectral leakage. In this paper CORDIC based VLSI architecture for implementing Kaiser-bessel window is proposed for real time applications. The parallel pipelined techniques has been adopted to ensure high throughput. Yidong Liu, et.al.,[10] they present that a modified CORDIC cell unit is proposed for parallel architecture and implemented on FPGA. Taylor series is used as the theory basis for the approximation of angle rotation and it reduces the usage of ROM. Thus area and power is reduced due to partial usage of ROM storage.

III. PROPOSED MODEL

DIF-FFT

The decimation_in_frequency(DIF) radix_2 partitions the DFT computation in to odd_indexed and even indexed outputs,which can each be computed by shorter length DFTs of dissimilar combinations of input samples. Recursive application of this decay to the shorter length DFTs results in the full radix_2 decimation _in_frequency FFT.the figure below shows the first stage of the 8-point DIF algorithm.

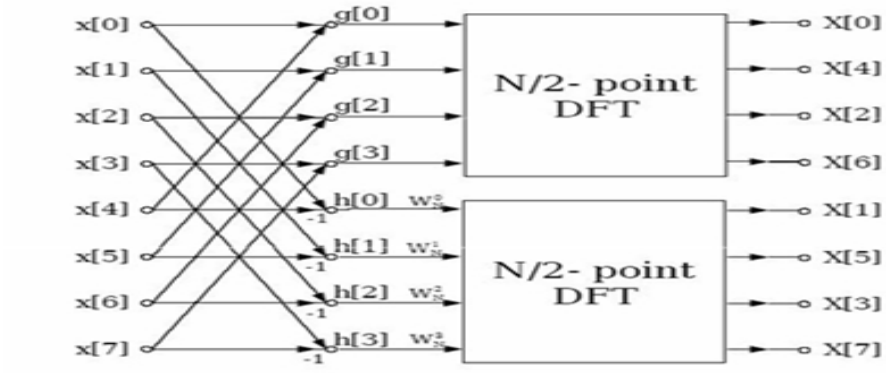

Fig 1:First stage of 8-point DIF algorithm

However the decimation causes shuffle in data.the entire process involvevs $v=\log_2 N$ stages of decimations, where each stage involves N/2 butterflies of the type shown in figure below.

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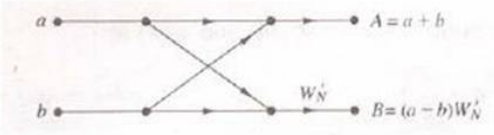

Fig 2: Butterfly structure

Here $W_N = e^{-j2\pi/N}$ is the Twiddle factor.
Consequently, the computation of N-point DFT via this algorithm requires (N/2) $\log_2$ N complex multiplications. For illustrative purposes,the eight point DFT algorithm is shown in below figure. bit reversed order with respect inputs. Furthermore, if we abandon the requirement that the computations occur in place, it possible to have both input and output in the normal order.

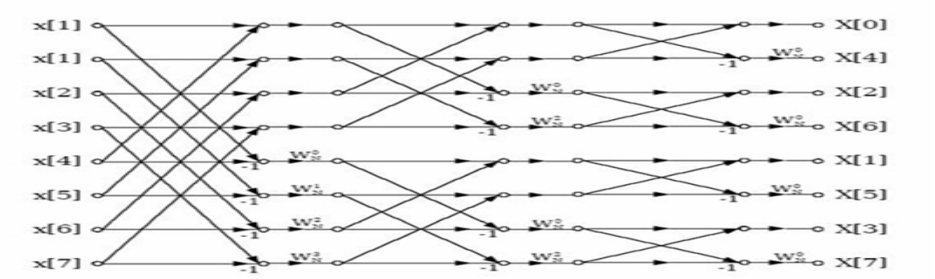

Fig 3: SFG of Computation of 8 point DFT using DIF FFT

The Fig 4 shows the basic hardware stage for single CORDIC iteration. After each iteration by using barrel shifters the number of shifts incremented.have an bit output precision (n+1) CORDIC iterations are needed.

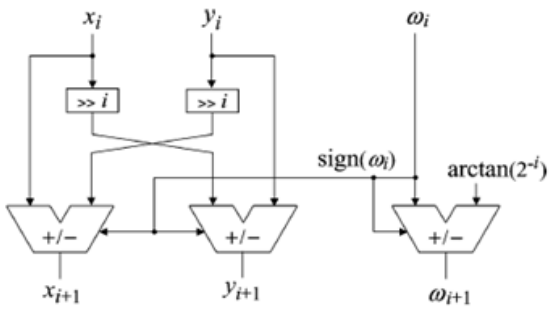

Fig 4: Hardware Implementation of CORDIC iteration

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IV. RESULTS AND DISCUSSIONS

a) RTL simulation and output waveform of CORDIC

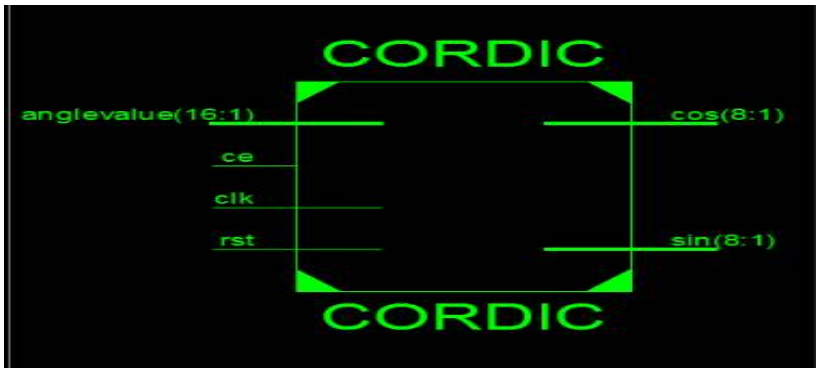

Fig 5: RTL of CORDIC

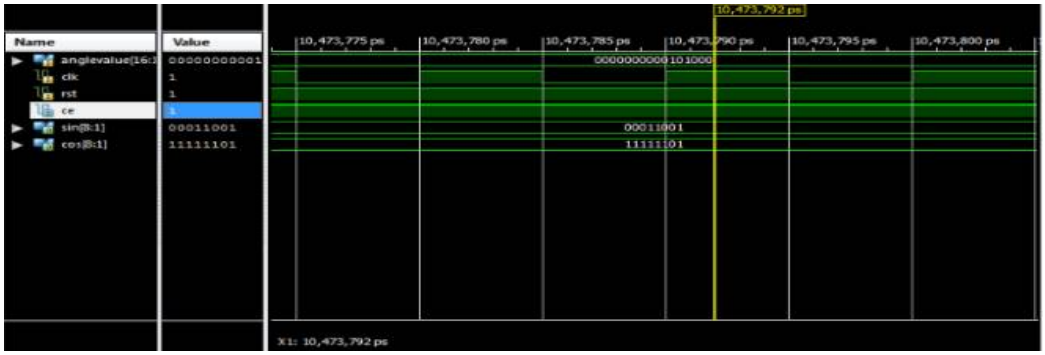

Fig 6: Output Waveform of CORDIC

The CORDIC consist of angle as input which is 16 bit, sin and cos as output which is 8 bit. If reset is zero then output is not generate if reset signal is high then output waveform generates with respective angle and clock enable is one.

b) RTL, simulation and output waveorm FFT

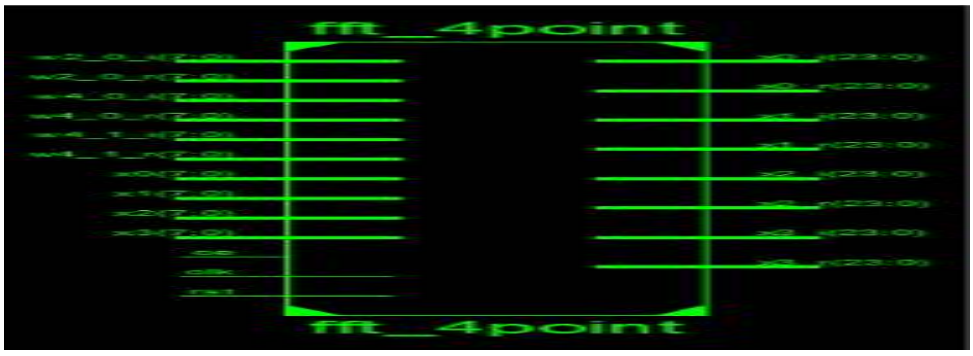

Fig 7: RTL of FFT

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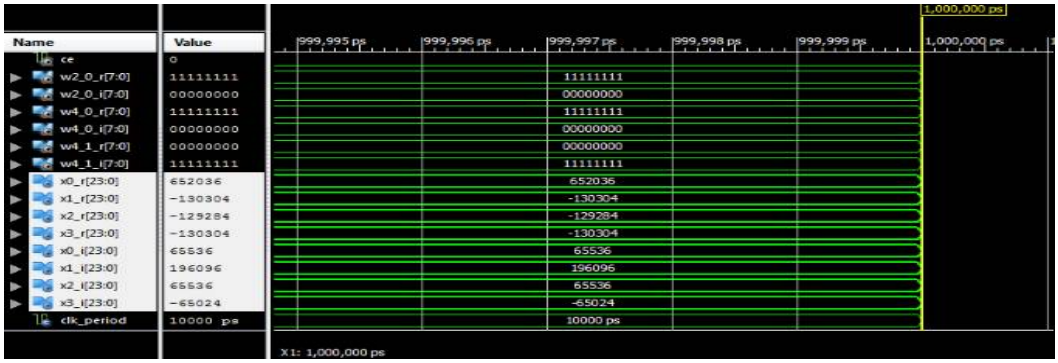

Fig 8: Output Waveform of FFT

The FFT consist of four inputs which is 8 bits and output is generated in real and imaginary which is 24 bits. For example each x0 gives real and imaginary value.fig 7 gives the RTL of FFT and fig 8 gives the simulation result of FFT.

c) RTL simulation and output waveform of CORDIC software

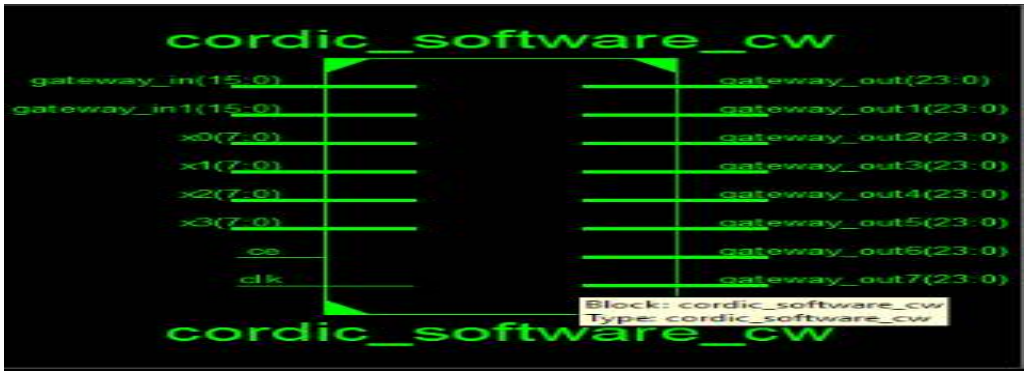

Fig 9: RTL of CORDIC software for FFT application

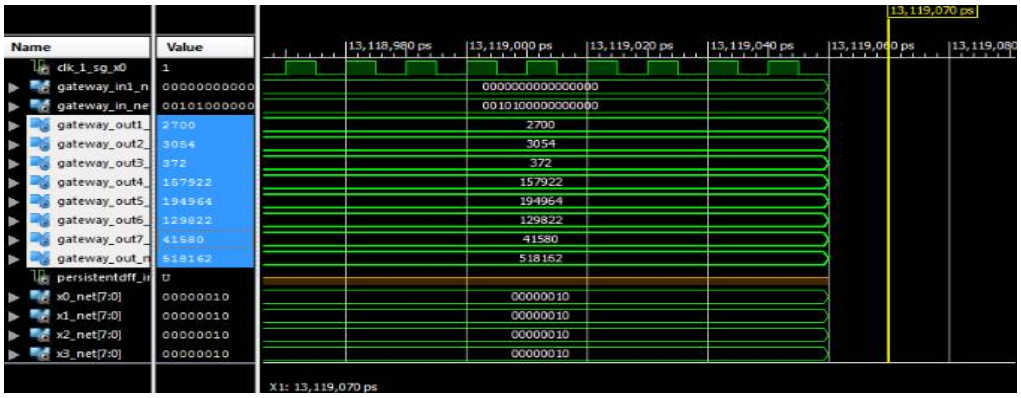

Fig 10: output waveform of CORDIC software for FFT application

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Fig 9 gives the RTL of CORDIC software it is a interfacing of CORDIC and FFT. Here gateway input is taken as 16 bit and x0 to x3 input is taken as 8 bit ofter interfacing it gives the output as 24 bit.And fig 10 gives the output waveform of cordic software.

TABLE 1: NUMBER OF SLICE LUT'S COMPARISION OF EXISTING AND PROPOSED DESIGN

AUTHOR	Number of Slice LUT's
Yidong Liu et al.,[10]	2986
Scaling free CORDIC[11]	1658
Proposed method	800 out of 27288

Area of existing methods are more and in proposed method the area is less utilized which is 800 out of 27288 number of slice LUT's and speed is increases up to 77.86MHz.

V. CONCLUSION

In this work, FPGA implementation of CORDIC for FFT application proposed for pipeline architecture and implemented on FPGA . FFT is used as the theory basis for the approximation of angle rotation.the modified architecture reduces the ROM storage for θ . number of slice LUT's less used compared to existing. Area utilized is less and also improve the speed of processor as 77.86MHz .rotation of angle is up to 0 to 180°.

ACKNOWLEDGEMENT

I thank, the management, Principle, HOD and staff of VLSI and ES Department, Visvesvaraya Technological University (VTU), Belagavi, Karnataka, India and my special thanks to my guide Dr.T.C.Thanuja, head of department of VLSI and ES for encouraging me for this work.

REFERENCES

[1] MILOS D.ERCEGOVAC, Redundant and On-line CORDIC; Application to matrix Triangularization and SVD, IEEE Trans. Comput., vol.39, no.6,pp. 725-740,june 1990

[2] Ren-Xi Gong, Ling-Ling Xie ,FPGA Implementation of a CORDIC based Radix -4 FFT processor for Real-time harmonic analyzer, seventh international conference on natural computation,ICNC 2011,

[3] pooja choudhary , Dr.Abhijit karmakar ,CORDIC based implementation of fast fourier transform , computer and communication technology (ICCCT), 2011 2nd international conference on 15-17 sept 2011,pages: 550-555

[4] Huan Li, Yan Xin,Modified CORDIC algorithm and its implementation based on FPGA,intelligent networks and intelligent systems(ICINIS) 2010, pp.618-621

[5] pramod k.meher, k.sridharan (2009) ,Efficient CORDIC algorithms and architectures for low area and high throughput implementation, IEEE Trans. Circuits syst. II, Vol.56, no.1,pp.61-65.

[6] shaoyun wang, vincenzo piuri, A unified view of CORDIC processor design, circuits and systems, 1997, in application specific processors, E.E. Swartzlander jr.(ed.), kluwer, pp.121-160

[7] Javier valls, martin kuhlmann, keshab k.parhi ,Efficient mapping of CORDIC algorithms on FPGA, signal processing systems,2000

[8] Nihel neji, et.al ,FPGA implementation of the CORDIC algorithm for fingerprints recognition systems,international journal of computer applications(2013),vol 63-No 6.

[9] kailash Chandra ray , et al.,CORDIC based VLSI architecture for implementing Kaiser-bessel window in real time spectral analysis ,journal of signal processing systems February 2014, vol 74, pp 235-244

[10] Yidong Liu, et.al.,A modified CORDIC FPGA implementation for wave generation, Circuits Syst Signal Process (2014) 33:321–329.