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Performance Analysis of Low Power DDR3 SDRAM Memory Control Unit

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ABSTRACT: Memory controllers are digital circuits that control data transport to and from the main memory unit. Due to its high speed and pipelined architecture, Double Data Rate Synchronous Dynamic Random-Access Memory (DDR SDRAM) is employed in computer architectures. DDR SDRAM is an improvement over regular SDRAM. It allows data flow on both clock cycle edges, increasing the data throughput of memory devices. The proposed study focuses on the implementation of a low-power DDR SDRAM controller with high speed. The clock gating technique is used to reduce power. The suggested DDR SDRAM controller's performance is assessed at 133MHz clock frequency, burst length of 8, 128-bit data interchange at both clock cycle edges, and read Column Address Strobe (CAS) latency 2. Thus, the total power reduction attained with the suggested methodology is 2.502%, which is greater than the power reduction reported in earlier work [13] with a single power reduction technique. The suggested design is modelled in VHDL, and simulation and synthesis are performed with the Xilinx tool.

KEYWORDS: Double Data Rate, Synchronous Dynamic Random-Access Memory, Power Reduction, Clock gating, Verilog/VHDL.

I. INTRODUCTION

The two primary issues in the design of any electronic equipment are high operation speed and low power consumption. In modern computer systems, processors-I/Os access data using one or more memory controllers. Memory controllers are digital circuits that control the flow of data to and from main memory. Memory controllers, in particular, are designed to handle read and write operations on Dynamic Random-Access Memory (DRAM), as well as refresh logic, which is performed on a regular basis to keep data on DRAM.

DRAM operates in an asynchronous mode, meaning it responds only when the control input changes. They are only capable of handling one request at a time [5]. SDRAM (Synchronous Dynamic Random-Access Memory) operates at a quicker rate than DRAM. It can run more effectively because it is synchronized with the processor's clock. SDRAM's internal pipelined architecture is responsible for its fast operating speed. The phrase pipeline architecture refers to the technique through which SDRAM accepts new instructions before the preceding one has completed processing [6]. This internal pipelined architecture adheres to the 2n rule of prefetch architecture, and space is reserved for the column address, which must be changed every clock cycle for high speed operation and total random access [8].

DDR SDRAM is an upgraded version of standard SDRAM. It enables data flow on both clock cycle edges, increasing the memory device's data speed. DDR SDRAM operates using differential clock signals: CLK and CLK', as well as a data probe signal (DQS) for burst mode data transfer [1][2]. At the positive edge of CLK, all commands (address and control signals) are issued. DQS is a strobe signal utilized by the memory controller and DDR SDRAM during write and read operations. Both the input and output signals, as well as the clock signal CLK, are referenced at the DQS edges. DDR SDRAM read/write operations use a burst mode method, which allows data to be accessed from several locations. Data access begins with the ACTIVE command, which is followed by the READ or WRITE command. DDR SDRAM has four banks, each with a number of rows. Rows of this type are separated into columns, with each column having 64 bits of data. The size and internal organization of DDR SDRAM are determined by the number of rows and columns [1].

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Higher transfer speeds are feasible with DDR SDRAM interface compared to single data rate (SDR) SDRAM because the data and clock signals are timed precisely. To achieve the needed timing accuracy, strategies such as phase-locked loop (PLL) and self-calibration must be utilized during implementation[3][4].To reduce the clock frequency, the interface allows data to be transferred on both the rising and falling edges of the clock cycle. The main advantage of utilizing a lower frequency is that it reduces the signal integrity requirements on the circuit board when connecting memory to the controller [1].

II. METHODOLOGY

DDR SDRAM Interface is made up of two parts: DDR SDRAM Controller and DDR SDRAM. Signals from the user interface (Bus Master) are fed into the controller, and the controller's output is fed into the DDR SDRAM. Figure 1 depicts the DDR SDRAM interface block diagram.

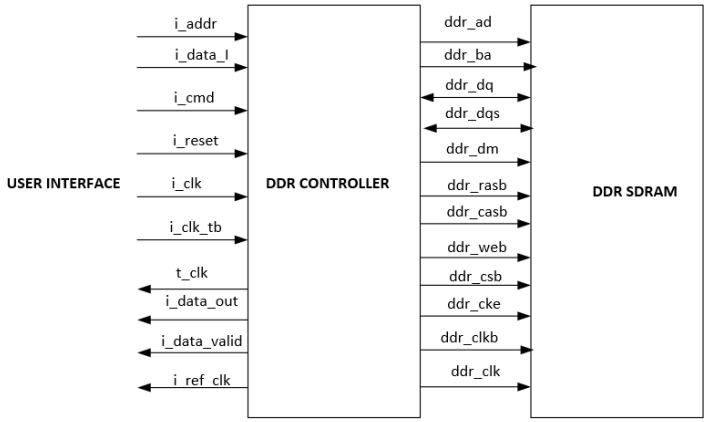

Fig. 1 Block Diagram of DDR SDRAM

The architectural model of a DDR SDRAM module has many blocks for initialization and issuing read/write commands. In previous efforts, Delay Locked Loop (DLL) was employed to create clock [4][2]. In this work, Phase Locked Loops (PLL) were used because they provide frequency multiplication, allowing slower or faster clock trains to be generated from the system clock, whereas DLL does not provide frequency multiplication and instead uses adjustable delay lines to align the output clock pulse with the reference clock pulse [14]. In order to synchronize with the user interface clock, frequency must be multiplied. Thus, clk is used to synchronize the system clock with the user interface clock, while clk2x is used to transport data during read/write operations.

The architecture of DDR SDRAM is shown in Fig. 2. It consists of the following modules-

- Main Control Module
- Signal Generation Module
- Data Path Module
- PLL block

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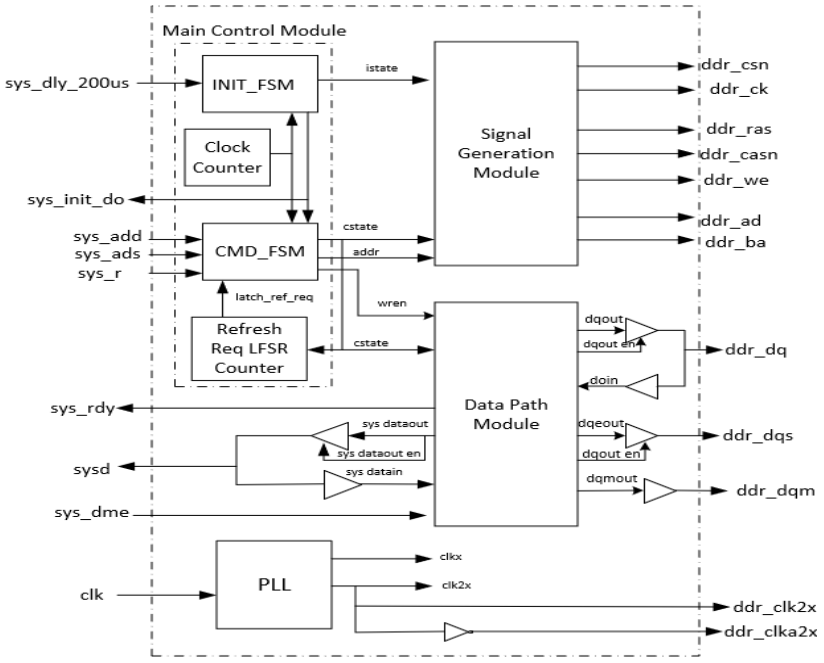

Fig. 2 Architecture of DDR SDRAM Controller

DDR SDRAM operates at fast speeds thanks to the DDR architecture. In the case of DDRAM, a 2n prefetch architecture is utilized, which allows two data bits to be obtained for one clock pulse at the input/output pins for a single read or write operation.

The main control module is in charge of initializing the memory controller by sending initialization and command signals. The istate and cstate signals are the initialization and command signals created by the two finite state machines' system interface control signals. The signal generation module generates address and command signals depending on istate and cstate. The PLL block is in charge of providing clock signals to all DDR SDRAM submodules. Data route module performs read and write operations between bus master and DDR SDRAM.

A. Main Control Module:

DDR SDRAM Controller requires initialization parameters to function. Two finite state machines are included in the primary control module to provide initialization and command signals to the memory controller. Access to memory will be granted after two finite state machines send signals. The submodules of the primary control module are as follows.

- Initialization_FSM
- Command_FSM
- Counter module

Initialization_FSM: Initialization_FSM uses a series of operations to initialize DDR for regular memory access. Initialization_FSM is a mealy state machine, which means that data is sent at the positive (or negative) edge of the clock cycle, and outputs are sampled only on the active clock edge. The operation of a state machine begins when the reset signal becomes low. Figure 3 depicts Initialization_FSM.

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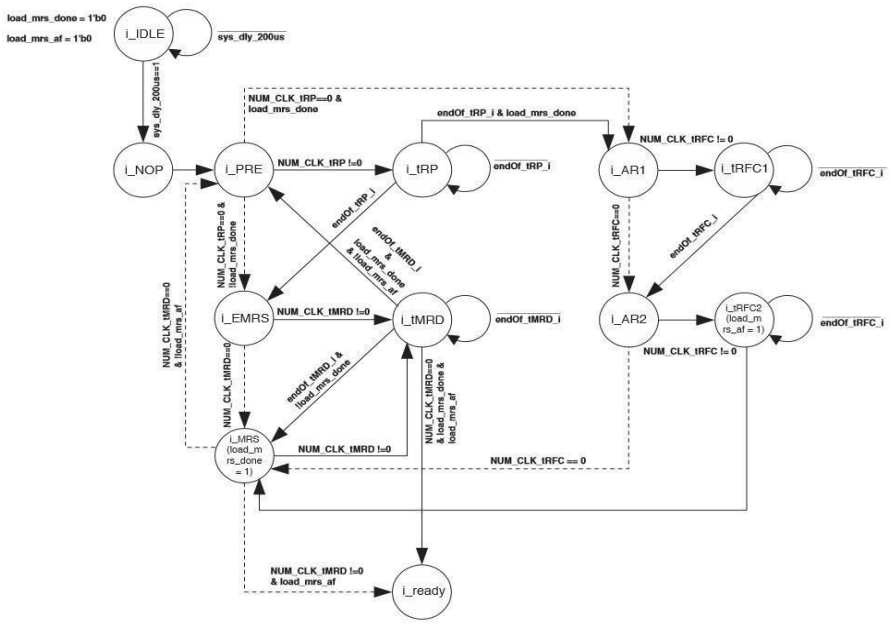

Fig.3 Initialization_FSM

When the reset signal is set to logic low, the finite state machine, regardless of its current state, enters the i_IDLE state. The system remains idle in the i_IDLE state and does not conduct any operations.

The controller waits for the clock to stabilize for a period of time. The clock stabilization period in our situation is around 200us.When the clock signal stabilizes, the reset signal rises from its low condition. The presence of an active high on sys_dly_200us shows that the clock has been stabilized. Following this, the initialization of the finite state machine begins. The Initialization_FSM transitions from i_IDLE to i_NOP. The i_NOP (No Operation) state is introduced to prevent undesired commands from being registered during the i_IDLE or wait phases. It has no effect on any ongoing operations. FSM switches from i_NOP to i_PRE on the next clock cycle. PRECHARGE command is created in the i_PRE state and applied to all banks in the device. Depending on the situation that triggers the particular bank, this command can open the row in all banks or disable the row of bank. After generating PRECHARGE orders, the finite state machine proceeds to the next stage, which involves generating two AUTO REFRESH commands to refresh the SDDRAM memory. The AUTO REFRESH instruction is issued whenever a refresh is required. To execute the AUTO REFRESH command, all banks must be idle. Commands for refreshing are issued twice. Once the memory has been refreshed, the FSM proceeds to the next state, i_MRS state [2].

The LOAD MODE REGISTER instruction is delivered in the i_MRS state to setup the SDDRAM controller for operation. This, like the AUTO REFRESH command, will be applied to all banks when they are idle and will wait until tMRD meets the subsequent executable command to be sent. After finishing the i_tMRD delay, Initialization_FSM advances to the next stage, i_ready. Memory access operations commence at this point. To signify that initialization is complete, the signal sys_INIT_DONE is set to high.

1. Command_FSM: Command_FSM is in charge of read/write operations. The logic levels on sys_R_wn indicate read/write operations: logic high indicates a read operation, logic low indicates a write operation. Figure 4 depicts the Command_FSM.

During a read operation, the state machine transitions from c_reada to c_cl after a specified interval. Following this stage, the machine transitions to c_rdata to transmit data from SDRAM to the bus master. When the data transfer is complete, the state machine returns to c_idle. During write operations, the FSM transitions from c_writea to c_wdata to transfer data from the bus master to SDRAM and then returns to c_idle [4].

2. Counter: For consecutive Read or Write operations, this counter is included. In the case of consecutive Read/Write operations, the burst count number determines when the next Write or Read instruction is given. DDR controllers provide high performance memory for systems that require access to an external device with the fastest throughput and lowest latency achievable.

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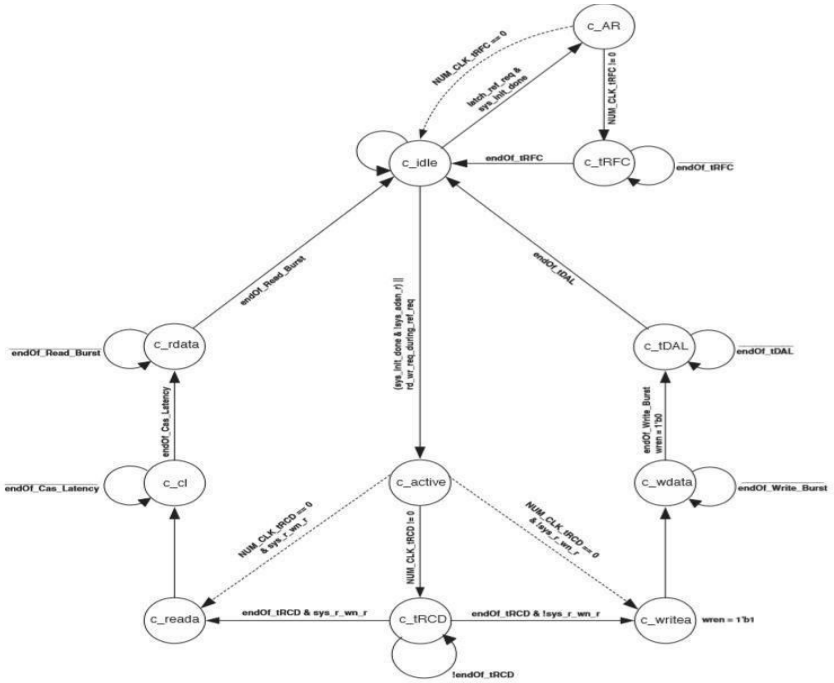

Fig.4 Command_FSM

B. *Signal generation Module:* This module generates command signals to the DDR SDRAM. Fig. 5 indicates the signalgeneration module.

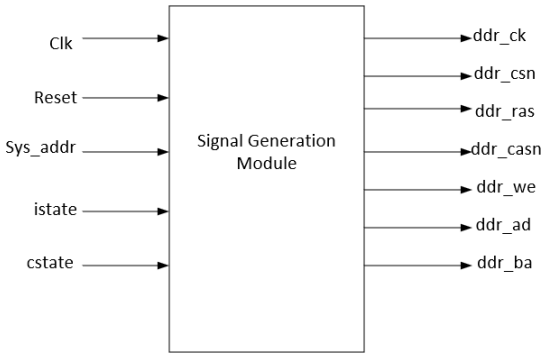

Fig. 5 Signal Generation Module

Signal ddr_ad is for selecting the address, ddr_csn and ddr_ras are for selecting particular row and column address. These signalsare managed by the value of istate and cstate from the main control module.

C. *Data Path Module:* Data path module is responsible for transmitting the data to the memory. The main functionality of data path module is storing the write data and evaluating the values for read data path. Data transfer between DDR SDRAM and user interface takes place at both the positive edge and negative edge of the clock signal. Because of this reason there is timing requirement for generating and sampling the write data and read data respectively.

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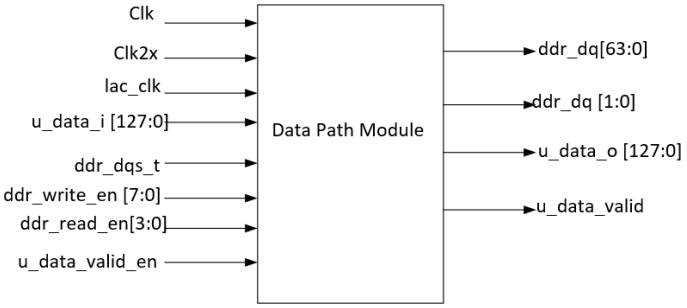

Fig. 6 Data Path Module

D. PLL Block: Phase locked loop block is required in design to generate clk (133MHz) and clk2x (266MHz). PLL is also responsible for generating the ddr_clk and ddr_clkn. The reason for including clk2x from PLL is to manage the read/write datapath delay.

III. POWER REDUCTION TECHNIQUE:

Clock gating is a power reduction technique used in synchronous circuits to reduce dynamic power. Low toggling rate significantly minimizes dynamic power usage. To eliminate wasteful switching activities, clock gating selectively disables the clock to specific blocks of design. Clock gating approaches include gate-based clock gating, latch-based clock gating, flipflop-based clock gating, and adaptive clock gating. Adaptive clock gating is thought to be more effective than previous strategies since it overcomes drawbacks such as glitch recurrence and huge area usage. In our architecture, adaptive clock gating is used in the PLL block, which feeds clock to all of the DDR SDRAM controller's other blocks.

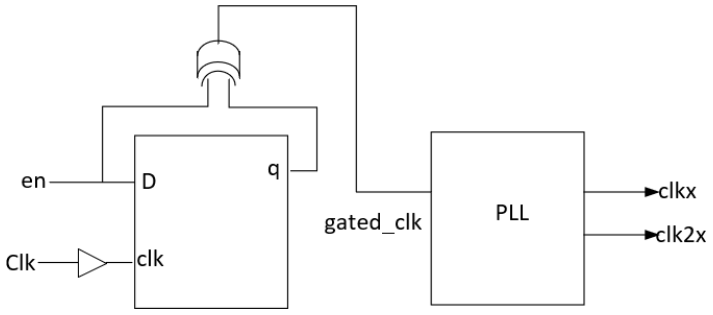

Fig. 7 Gated clock circuit for PLL

The gated clock signal is generated by XOR and flipflop in the adaptive clock gating technique, as shown in Fig. 7. The enable signal of the controller is fed into the flipflop. When the enable signal changes, i.e., when the present input and present output change, the gated_clk value changes to 1. This gated_clk signal is fed into the PLL block, which generates the ddr_clk and ddr_clkn signals. The use of this technology in design reduces dynamic power usage.

IV. RESULTS

To reduce power consumption, the DDR SDRAM Controller employs clock gating. Table.1 compares the power consumption of DDR SDRAM controllers designed with and without clock gating. When compared to a DDR SDRAM implementation without clock gating, the version with clock gating results in lower dynamic, signal, logic, and I/O power levels.

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	Dynamic Power(W)	Signals (W)	Logic (W)	I/O (W)	Total Power(W)	Total Power reduction in percentage
Without Clock gating	21.731	4.785	3.313	14.632	44.551	-
With Clock gating	21.714	4.779	2.310	14.625	43.428	2.5207%

Table. 1 Comparison table for power consumption with and without clock gating design

Thus, using the proposed methodology, it is conceivable to reduce power by more than the amount reduced in earlier work. Table 2 shows the utilization data, which shows that DDR SDRAM implemented with clock gating consumes less LUTs, registers, and bonded IOBs..

	Slice LUTs (134600)	Slice Registers (256241)	Bonded IOB (500)
Without clock gating	864	1347	368
With clock gating	874	1345	355

Table. 2 Utilization Report comparison with and without clock gating design

Simulation result of DDR SDRAM Controller during read operation is shown in Fig. 8. Simulation waveform of DDR SDRAM Controller during write operation is shown in Fig.9 These simulation results are obtained from Xilinx simulator.

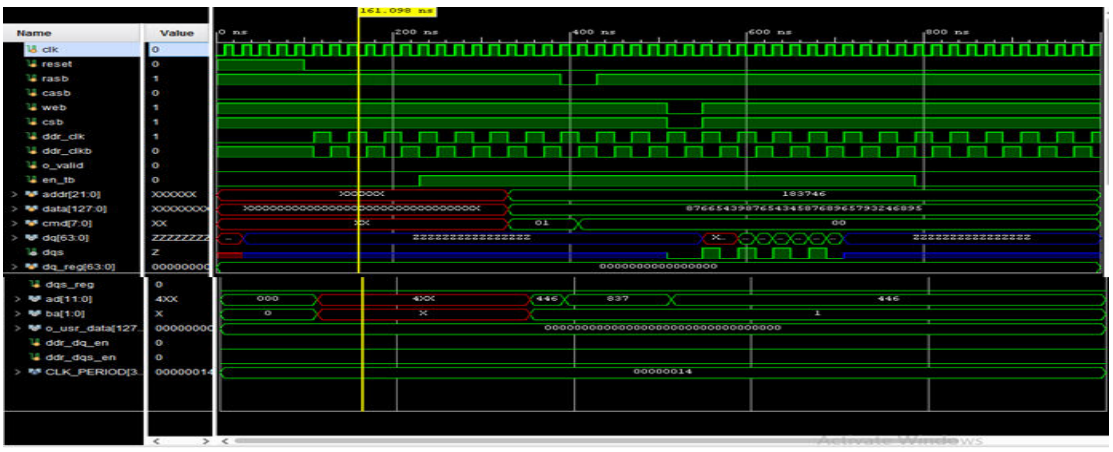

Fig. 8 Simulation waveform of controller during read operation.

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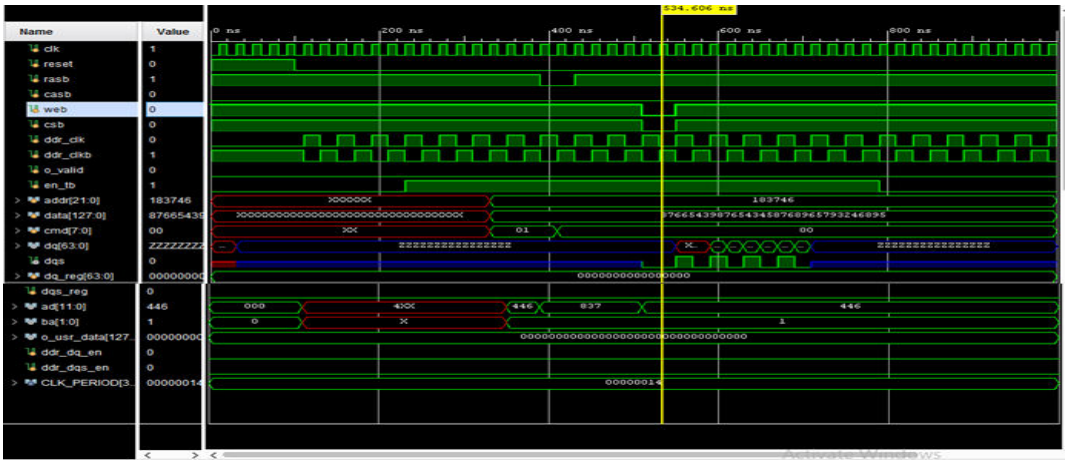

Fig. 9 Simulation waveforms of controller during write operation.

V. CONCLUSION

The proposed DDR SDRAM controller can be used for real time applications. It is implemented for operating frequency of 144 MHz.Phase Locked Loop (PLL) has been used instead of Delay Locked Loop (DLL) to achieve frequency multiplication clkx and clk2x, where clkx is used for synchronizing system clock with user interface clock and clk2x is used for transferring of data during read/write operations. Using PLL in design also has advantage of generating faster frequency multiplication thus achieving the high speed. Power reduction technique clock gating has been used in design to achieve reduction in dynamic power consumption. The proposed design is modelled using Verilog HDL, simulated and synthesized using Xilinx tool.

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