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Design and Implementation of Floating Point Complex number Multiplier Using Modified Vedic Algorithm

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ABSTRACT: The main purpose of this project is to Design and implementation floting point complex number multiplier by using Vedic Mathematics. The term 'Vedic' is obtained from the word 'Veda' which means the store-house of all knowledge. Mathematics, from the Veda provides one line, and super fast methods with a quick cross checking systems..Vedic Mathematics is a mathematical extention of 'Sixteen Simple Mathematical formulae.For implementation of Floating point multiplier we can use Vedic Multiplication Technique. Minimum delay in multiplication of all types of numbers, either small or large Multiplication has been achieved by using The Urdhva-Tiryagbhyam Sutra .Which is performed by vertically and crosswise method. The partial products and sums are generated in one step which reduces the carry propagation from LSB to MSB. Hence it improves the performance of the design for high speed Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics have been modified. Vedic Multiplication Technique is been used to implement Floating point multiplier**.** Design and Implementation of floting point complex number multiplier using IEEE 754 standard and vedic sutras is been illustrated. Multiplier is being implemented by using Xilinx9.1i Synthesis Tool.

KEYWORDS*:* Vedic Mathematics , Urdhva- Tiryagbhyam Sutra , floting point complex number multiplier

I. INTRODUCTION

Performance of any system depends on the performance of its multiplier, because the multiplier is the slowest element in the system. For most the DSP applications the executional time has been dominated by multiplication so there is need of high speed multiplier. Also it consumes most of the area. Hence, for reducing the area and increasing the speed of the multiplier are the major our major design issue. But, both speed and area are opposite to one another because improving speed results in larger areas.Hence we require a new spectrum of multipliers. The backbone of many digital signal processing algorithms is the Complex number operations which mostly depend on extensive number of multiplication. It involves four real number multiplication and one additions and one subtractions . For performing such real number multiplication, the carry needs to be move from the LSB(least significant bit) to MSB(most significant bit) when binary partial products are been added.Due to which The overall speed is drop down by the addition and subtraction after binary multiplication.The basic functions used in digital signal processing (DSP) application is the Binary floating point numbers multiplication. Binary Floating point numbers are represented by the IEEE 754 standard format(single and double format). The Single precision format consists of 32 bits and the Double precision format consists of 64 bits. The multiplier for the floating point numbers are represented in IEEE 754 format which can be divided in four different units :-(1)Mantissa Calculation Unit (2)Exponent Calculation Unit (3)Sign Calculation Unit and Control Unit. This project proposes the design of 8,16 bit Vedic multiplier, design of 8,16 bit complex Vedic multiplier, design of 8,16 bit signed Vedic multiplier, design of 8,16 bit floating point Vedic multiplier based on vertical and crosswise structure of Ancient Indian Vedic Mathematics.. This gives chance for modular design where smaller blocks can be used to design the bigger one.

This article contents are. Section 2, related work on the topic. In Section. 3, simulation results. In section 4, conclusion of project.

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II. RELATED WORK

A.*The vedic multiplication :*

It is based on the Urdhva- Tiryagbhyam Sutra. The proposed complex number multiplier use the Vedic multiplication formulae Which has been used for the multiplication of two numbers in decimal formso that the proposed algorithm must be compatible with the digital hardware.

B. *Urdhva Tiryakbhyam sutra*

It generally means "Vertically and crosswise" multiplication. using this sutra is performed by vertically and crosswise, vertically means straight above multiplication and crosswise means diagonal multiplication and taking their sum. The feature of this method is any multi-bit multiplication can be reduced down to single bit multiplication and addition.

For understanding the Vedic Multiplier (Urdhav-Triyak method) let us consider a multiplier A[n] of size 'n' words similarlyconsider a multiplicand B[m] of size 'm' words, where A and B are given by equation 1 and 2**.**

$$A[n] = \sum_{i=0}^{m-1} ai * X^{i} \qquad \text{Eq.1}$$

$$B[m] = \sum bi * X^{i} \qquad \text{Eq 2}$$

Now after taking the Product of A and B we get :

$$P[n+m] = A[n] * B[m] \qquad \text{Eq.3}$$

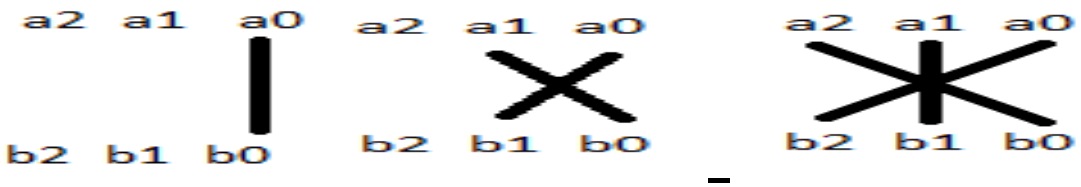
C. *Floating Point Multiplication:*

Generally in IEEE 754 format the multiplier for the floating point numbers can be divided in four units:-Mantissa Calculation Unit,Exponent Calculation Unit,Sign Calculation Unit and Control Unit. The representation of floating point number in standard format is (−1) S 2E (b0 · b1b2 … bp−1). Now Consider the multiplication of two floating point numbers A and B, where A = -19.0 and B = 9.5. The normalized binary representation are A = -1.0011x24 and B = 1.0011x23.

IEEE representations of operands in Sign Exponent Mantissa are:

A = 1 10000011 00110000000000000000000
B = 0 10000010 00110000000000000000000

whole performance of the Floating Point Multiplier is depends on the performance of Mantissa calculation Unit..The Vedic Multiplication method is been chosen for the implementation of the unsigned multiplier for multiplication of 24x24 BITs. It gives good result result in terms of power and speed. The Vedic multiplication system basically consist of 16 Vedic sutras .It describes the natural ways of solving whole range of mathematical problems. Out of these 16 Vedic Sutras the Urdhva-Tiryagbhyam sutra is been used . In this method the partial products are generated simultaneously which itself reduces delay and makes this method fast.



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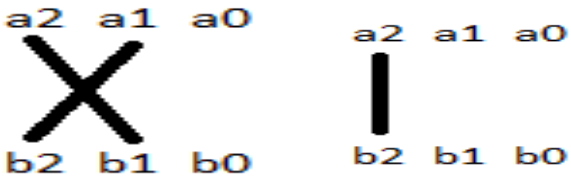

Fig. The Vedic Multiplication method

III .PROPOSED ALGORITHM FOR FLOATING POINT

The binary floating-point number is represented by 3 terms a sign bit, a significand bit and the exponent. Consider two numbers Operand A and Operand B, such that

Operand A=sign A & eA & fracA Operand B=sign B & eB & fracB

Where , fracB are the exponents and significands of the numbers, respectively. Now following steps explains the detailed description of the algorithm

1. If we make ea or eb equals to 0, then it will be '0', otherwise it will be '1'. Here 33 bits are needed to store the number, 8 for the exponent, 24 for the significand and 1 for the sign.

2. we obtain the result as: Sign =signA xor signB, e = eA + eB, Frac = fracA x fracB

The sign of the result is just the XOR of the two sign bits.

3. The product of two 24-bit numbers can be 48-bit wide. But only, 24 bits can be accommodated for the significand. Therefore, by using the methods of rounding(Round-to-nearest-even, round-up, round-down and round-to-zero) is been used. So the 48-bit result is rounded up to 24 bits.

4. For normalization there must be a leading '1' in the significand bit of any floating-point number .To make the MSB '1' in the result, the bits are shifted left, and with each shift, the exponent is incremented by 1.

5. The result is assembled into the 32 bit format, and neglect the 24th bit .

IV PSEUDO CODE

Step1. if the product is 0, the exponent must be set to the largest negative value which, in the biased case, is 0

Step 2. , if the resulting exponent is too large in magnitude, an exponent overflow is said to have occurred, which cannot be corrected, hence, an overflow indicator must be tuned on

Step 3. Finally, denormalized numbers and NaNs must be given special attention.

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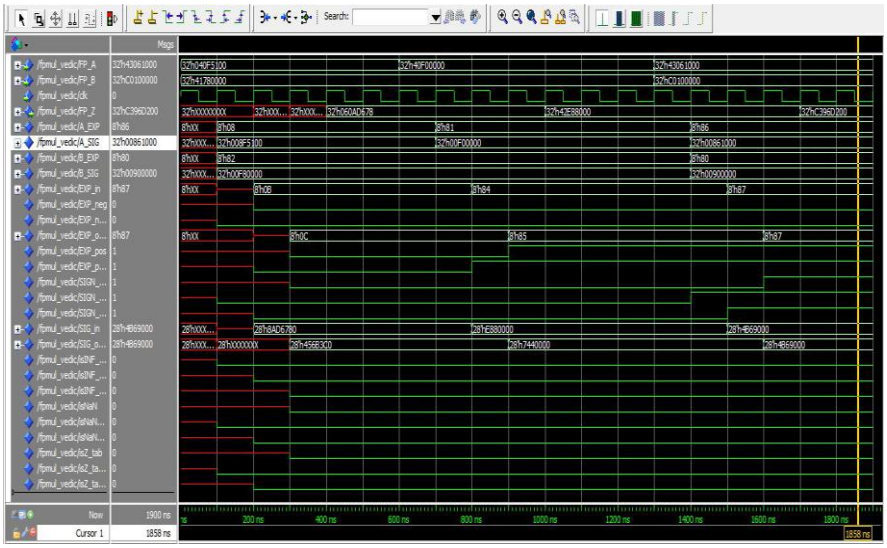
V. SIMULATION RESULTS

Logic synthesis and simulation was done using EDA (Electronic Design Automation) tool in XilinxISE9.1i.



Simulation Result of Floating point

First i had taken any two inputs like A and B.These are consider as the multiplier and multiplicand.I perform multiplier using Vedic Algorithm between these two inputs. Here 'A' is unsigned floating point number and 'B' is Signed Floating Point Number.Value of A is convert to binary format after normalize. Then I have to convert it into IEEE-32 floating point format and then then convert it into hexadecimal format. Similarly we convert the B.The result which will be a hexadecimal number is store in another output.

VI. CONCLUSION

The Floating Point numbers are very useful in the recent period of digital design based systems . Vedic method of multiplication based design is been used. It has been seen that floating point number multipliers are much faster than the conventional multipliers. So for large input number the complexity gets reduced and compatibility also gets increased. Furthermore to reduce the delay and hardware requirement we used Urdhva-Tiryagbhyam sutra algorithm for multiplication of Floating point numbers

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BIOGRAPHY

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