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Design and Implementation of Low Power Phase Lock Loop Using Sense Amplifier

Anurag Bhatt, Gajendra Sujediya

M. Tech. VLSI Scholar, RIET Jaipur, India

Assistant Professor, RIET Jaipur, India

ABSTRACT: PLL with redesigning of individual blocks like- PFD is designed using edge triggered D flip flop to reduce area and static phase error, CP is designed using current mirrored structure to minimize the current mismatch with increased output voltage and VCO has been designed using self bias differential ring oscillator to achieve low jitter operation of PLL. The PLL is designed using 180 nm CMOS technology for high performance with 1.0 V power supply

I. INTRODUCTION

PLL is simple feedback system that compares the output phase with the input phase and produces the output frequency which is proportional to the input phase difference. Since its invention in1932, the basic phase locked loop has remained nearly the same but its implementation in different technologies and for different applications continues to challenge designers. A PLL serving the task of clock generation in a microprocessor appears quite similar to a frequency synthesizer used in a cell phone.

PLL is used to recover a signal from a noisy communication channel, generate stable frequencies or distribute clock timing pulses in microprocessors. The PLL based frequency synthesizer plays a very significant role in direct frequency modulator, frequency demodulator and the regeneration of the carrier from the input signal in the wireless communications. PLL is used for clock and data recovery circuit in the broadband data communication network, which is used to recover the data from the NRZ clock and data re-timed decision.

Phase lock loop design

II. BASIC PLL CIRCUIT

A PLL is a feedback system that compares the output phase with the input phase. The comparison is performed by a ‘phase comparator’ or ‘phase detector’. The basic elements of a Phase locked Loop (PLL) are a Phase detector (PD), Low Pass Filter (LPF) and a voltage controlled oscillator (VCO) in a feedback loop.

The role of Phase detector is to compare the phase of Vout and Vin and then generating an error. Thus PD detects a phase error between the reference signal and the output signal of PLL. And the error detection range can be extended with PFD. The input phase errors are detected by Phase-Detector (PD) or Phase - Frequency Detector (PFD). These errors (phase or frequency errors) are converted into current or voltage to control the output frequency of Voltage Controlled Oscillator (VCO) by charge pump in a charge - pump PLL. According to that error, VCO frequency varies until the phases are aligned, i.e. the loop is locked. The phase detector (PD) output, VPD, consists of a high-frequency components (undesirable), dc component (desirable) and the control voltage of the oscillator must remain quiet in the steady state, i.e. the PD output must be filtered. A Low pass filter is interpose between the PD and The VCO which is used to suppress the high-frequency components of the Phase Detector (PD) output and presenting the dc level to the oscillator.

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Fig. 3.1 shows the basic block diagram of PLL.

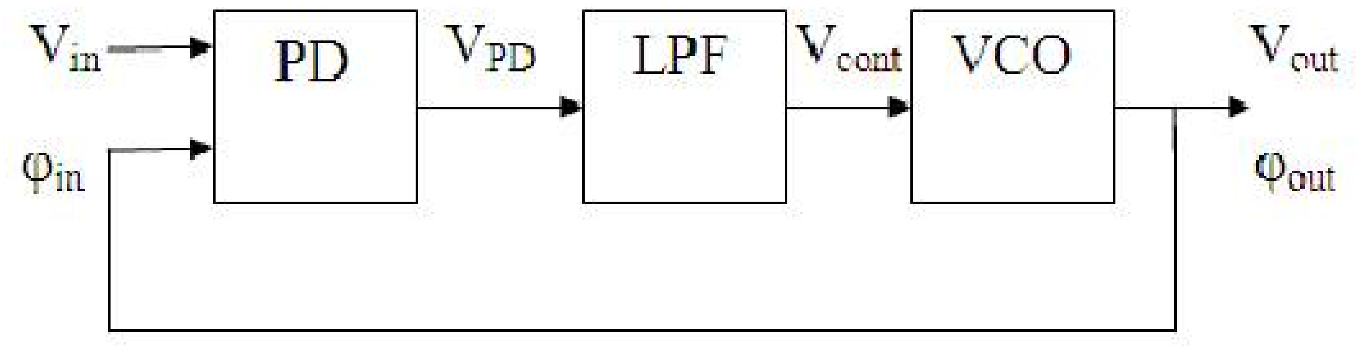

Fig. 1.1 Basic block diagram of PLL

Design and implementation PLL

A phase locked loop is a closed loop system that causes one system to track with another. The designing of PLL is done using tanner tool with 1.0 V power supply. The PLL is used for frequency synthesis application in this dissertation, so the block diagram will be taken as frequency synthesizer. Thus the basic block of PLL consists of five fundamental blocks, namely, PFD, CP, LPF, VCO and FD. The proposed PLL is designed to achieve the following properties

. Reduced locking time
. Low power dissipation
. Delay reduction
. Transistor Count

These design criteria are often I conflicts and improving one particular aspect of the design constrains the other. So each sub block of PLL has been designed in this chapter to satisfy all these properties.

Differential Charge Pump

In differential charge pump two outputs of PFD namely UP and DN are given to the two differential switches. Each switch has two inputs with one inverted input. The circuit requires two current sources for each switch. When the power supply is provided then the circuit gives differential output voltage of the two switches. The design of the differential charge pump is shown in figure 4.4.

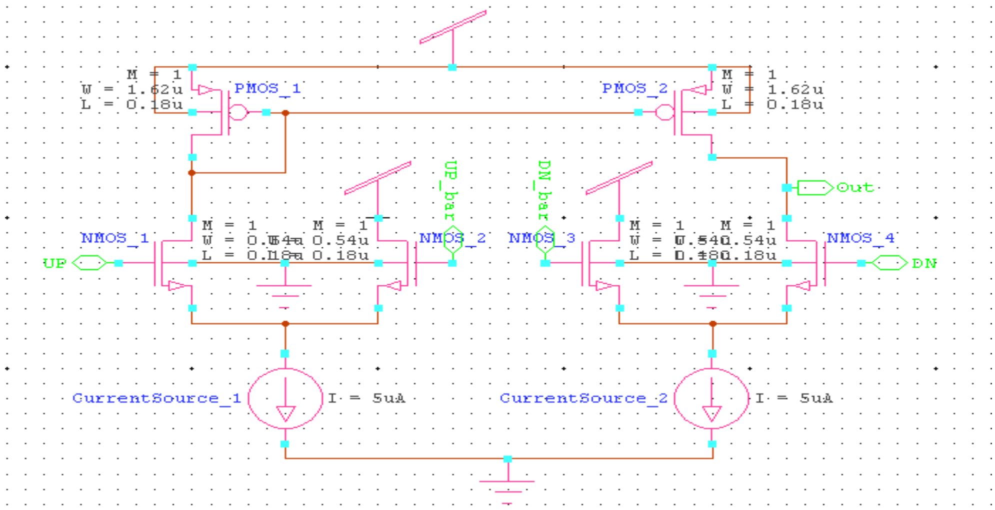

Fig. 1.2 Schematic design of differential charge pump

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Differential state is less sensitive to the leakage current and its output voltage is higher than basic charge pump but lesser then supply voltage so the purpose of using the charge pump is not solved. This differential charge pump suffers from some other drawbacks also like higher power dissipation because of two current sources, delay problem due to inverted input, current mismatch problem.

Voltage Controlled Oscillator

The voltage controlled oscillator is used to generate a specific frequency signal. This VCO is designed using self bias differential ring oscillator as shown in figure 4.11. In this figure, the MOSFETs M2 and M3 operate as inverter while MOSFETs M1 and M4 operate as current sources. The current sources limit the current available to the inverter or it can be said that the inverter is starved for the current. So this type of oscillator is called current starved VCO.

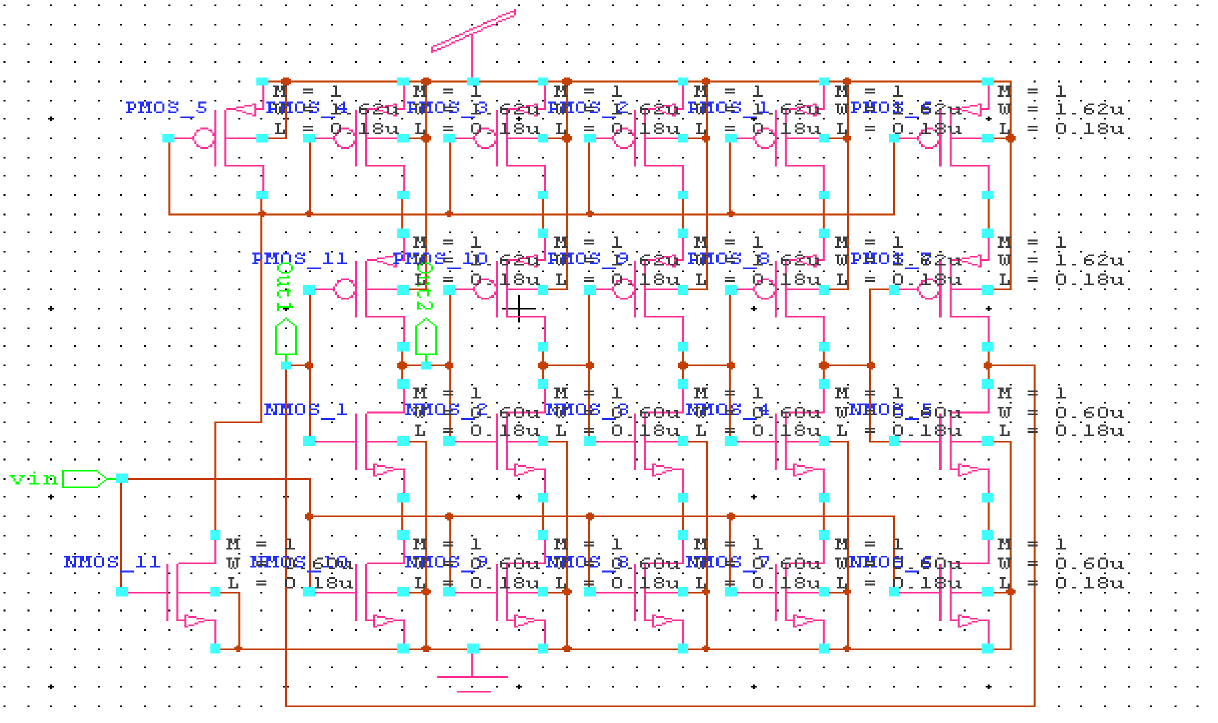

Fig. 1.3 Schematic design of ring voltage controlled oscillator

Here the drain currents of MOSFETs M5 and M6 are the same and are set by the input control voltage. The other transistors M7 to M22 are added just to form the 5-Stages of ring oscillator because it gives better VCO characteristic and frequency range.

. Phase Locked Loop using Sense Amplifier

In this dissertation the PLL is designed using sense amplifier, so the sub blocks used are PFD, CLSA, LPF, VCO and FD. By using the combination of all above sub blocks a PLL is designed as shown in figure 1.4.

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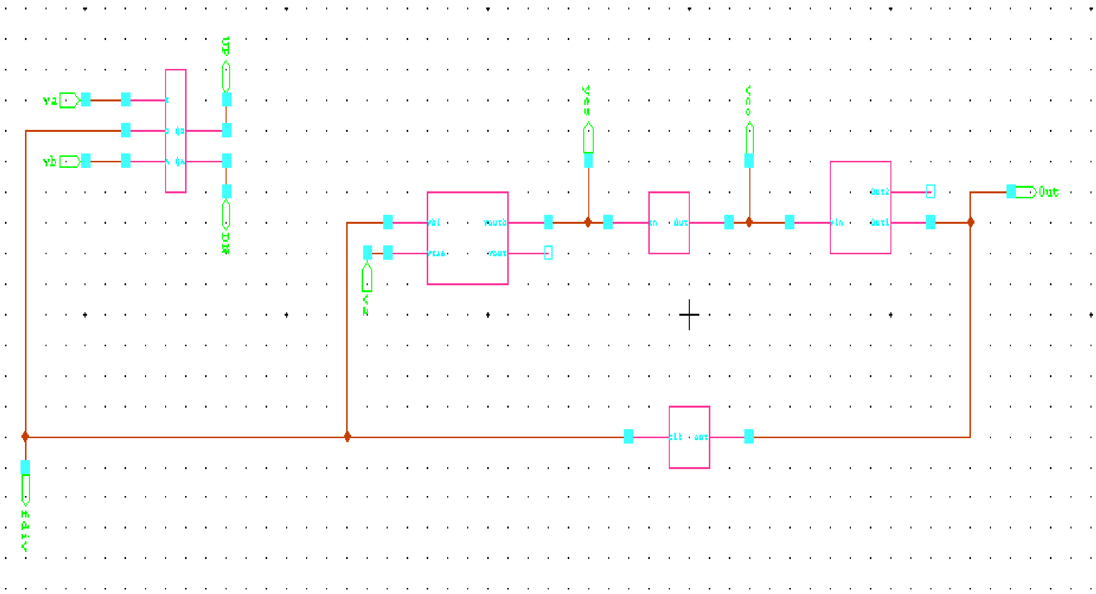

Fig.1.4 Schematic design of PLL using sense amplifier

simulation result and analysis

Proposed Phase Locked Loop using Sense Amplifier

The second order PLL using sense amplifier gives locking time of 0.49 µs. The simulation waveform of second order PLL using sense amplifier as shown in figure

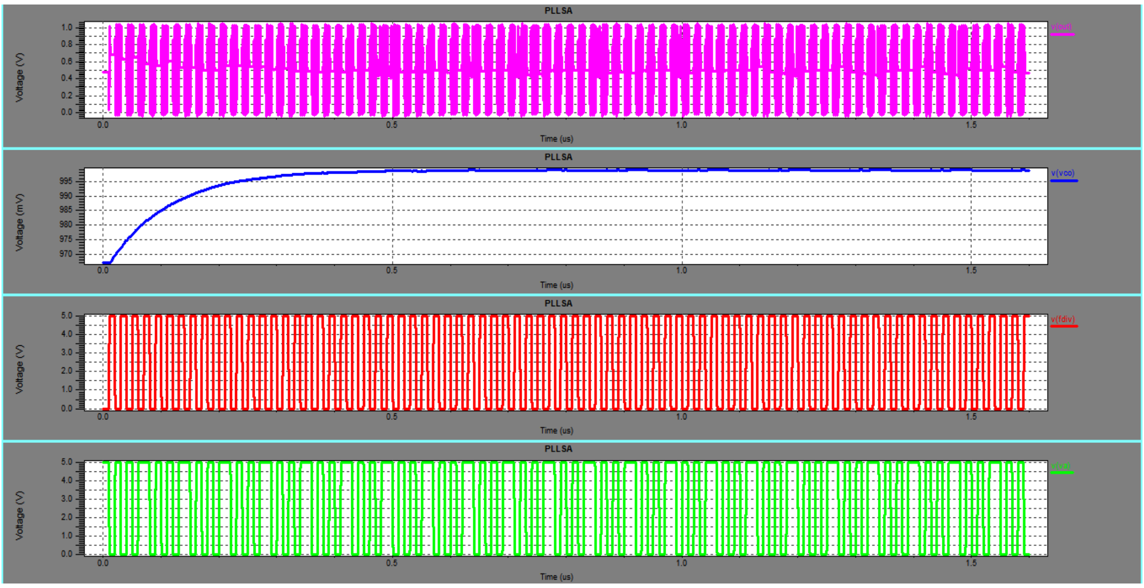

Fig1.5 Simulation of Sense Amplifier PLL

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IV. CONCLUSION AND FUTURE WORK

CONCLUSION

The present work studies the important charge pump and PLL architectures and their performance. In this project, a high speed CMOS sense amplifier for PLL application has been designed and simulated using the 180 nm CMOS technology. Thus this project simulates and analyses some of the major reported sense amplifier architectures for fast locking and less transistor count compared with the design of PLL using charge pump.

I feel confident that my design works properly. Furthermore, I have met the specifications as stated in the introduction. However, I have chosen the values such that we have most of the above features satisfactorily.

FUTURE WORKS

Sense locking time of the PLL is reduced by increasing the order of PLL. Therefore the future work of this project is to design third order PLL using sense amplifier.

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