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Study the Development and Operation of Discrete Vertical Drain Lateral-Diffused MOS (VDMOS) Power Transistors

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ABSTRACT: Due to scaling limitations, a conventional MOSFET cannot be used in high power applications. So for increasing RF application demand, a MOSFET was created known as VDMOSFET. This paper gives a brief review of VDMOSFET's construction and its working. Various parameters affecting its operation have also been discussed.

KEYWORDS: VDMOS, Threshold voltage, Gate oxide thickness, Threshold implantation, Channel doping

I. INTRODUCTION

A conventional lateral MOSFET structure cannot be easily scaled for high power applications due to two main reasons. First, a large spacing between drain and source is required to achieve a high voltage blocking capability. To get this, channel length must exceed the thickness of the space charge (SC) region on the channel side of the drain junction to avoid punch through. This results in wastage of larger surface area of the semiconductor using a lateral structure to reinforce the high drain voltage and to avoid punch through. Also having a longer channel will increase channel resistance and reduce the current rating of the device. Second, in the lateral MOSFET structure metallisation becomes complicated because all the connections i.e. source, drain and gate are created on the same upper surface. Both effects consume more area, resulting in a low silicon utilization factor. Due to these reasons, the simple lateral MOSFET structures are seldom used as power distinct devices. Conventional mosfets cannot be used for power applications by simply decreasing channel length of the device. Fig1 shows the diagram of conventional lateral mosfet.

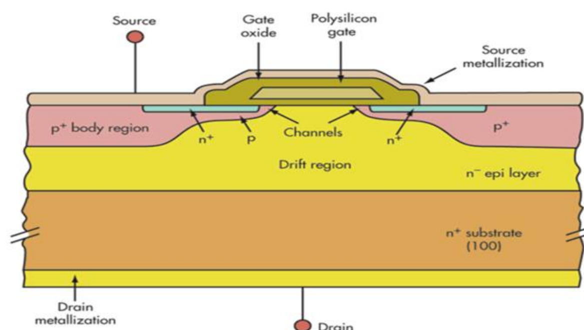

Fig. 1 The cross-sectional view of a conventional MOS transistor

II. DEVELOPMENT OF POWER MOS DEVICES

To eliminate two disadvantages of using a conventional lateral mosfets as power mosfets a distinctive mosfet was developed. First commercially created power device is VMOSFET i.e. V shaped groove mosfet. In this structure, the drain contact was formed on the substrate .The current flows vertically from drain to source. To create the V-shaped

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groove in the semiconductor surface after the p-body region and n+ diffusion an anisotropic etch was used. By connecting many individual devices in parallel during the metallization process a large current rating can be achieved. From the two sources (each sides of the groove) each gate of the vmosfet controls the current. Fig 2 shows the structure of vmosfet.

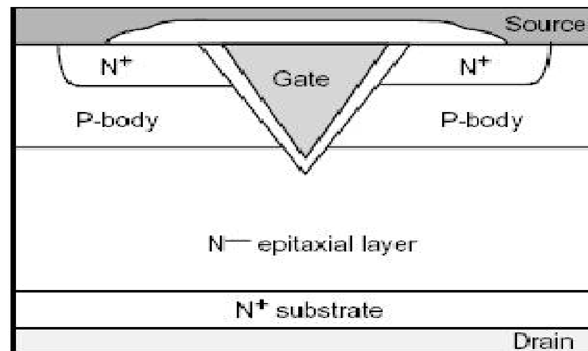

Fig. 2. Cross-sectional view of a VMOSFET [6]

As the current is overfilling at the spike of gate, it can decrease the useful current rating of the device as well as the voltage rating. This problem can be lowered by using the truncated vmosfet. Fig 3 shows the structure of truncated vmosfet.

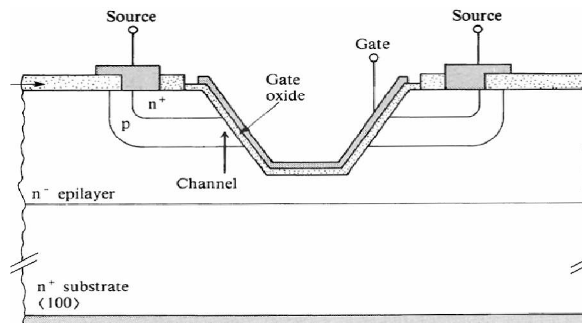

Fig. 3. The cross-sectional view of a truncated VMOSFET[7]

To expound two closely placed pn junctions at different depths below the silicon surface a vmosfet utilizes two successive diffusion steps. This dual diffusion technique can be used laterally in the same manner. The device structure called LDMOS. In this structure the channel length does not depend on the lithography step as in conventional lateral mosfets; rather it depends on the diffusion processes. Fig 4 shows the cross sectional view of LDMOS.

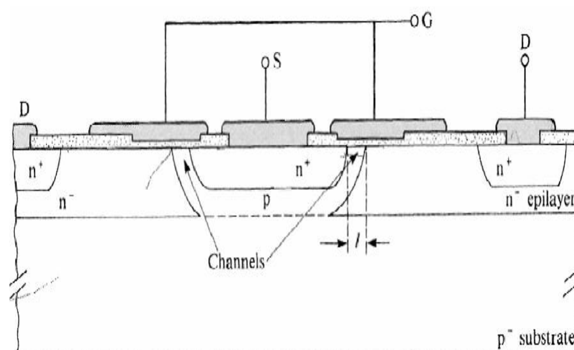

Fig. 4. The cross-sectional view of a LDMOS [7]

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The power mosfet design incorporates the proposal of VMOSFET and LDMOS. This structure is known as the vertical-diffused mosfet. The vdmos structure exploits the dual diffusion technique to determine the lateral surface channel length as in LDMOS and supports the drain voltage vertically in the n- epilayer as in VMOSFET. The electrons first flow laterally from the source through the channel and then flow vertically down through the n- epilayer to the substrate drain contact. Fig 5 shows the complete structure of vdmosfet.

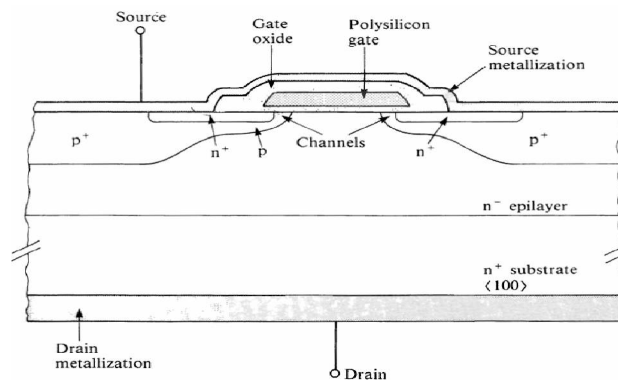

Fig. 5. The cross-sectional view of a VDMOS [7]

III. DEVICE CHARACTERISTICS: STATIC OPERATION

VDMOS characteristics are much like those of conventional mosfets. It has four distinct operation regions formed between the source (formed by n+ diffused region) and the substrate (n+ drain region) when it is working in active mode. Region A is the surface layer of the body region. At a given gate voltage the channel will form at this region. Region B is the surface layer of the body region between the source diffusions. Region C is the regions between body regions. Region D is the drain drift region in the epilayer. Any blocking voltages are developed across the region D whereas region A controls the flow of current in the device [7]. Fig 6 is showing all active regions of vdmos.

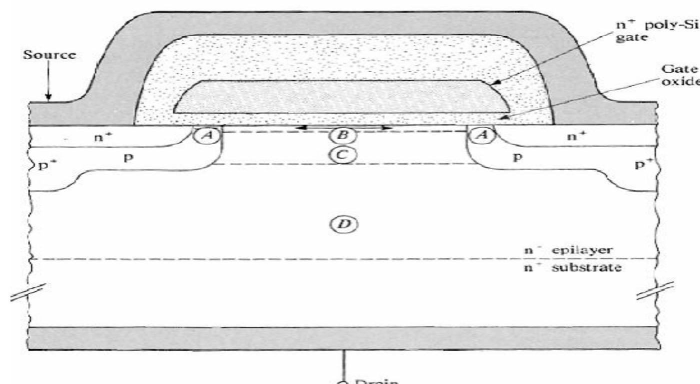

Fig. 6. The cross sectional view of a VDMOS showing the active region.[7]

A. *Threshold Voltage:*

A threshold voltage (V_T) of a mosfet is defined as the minimum gate voltage required for the inversion of the channel between source and drain. In vdmos, the main factors that modulate V_T are gate oxide thickness (t_{ox}) and peak surface concentration (N_A) in the channel. Since the peak body concentration of vdmos occurs near the source end, V_T is determined at the source end of the channel [7]. Positive charges such as mobile ions in the gate oxide can cause

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change in V_T. So, it is important to grow the gate oxide layer under extremely clean condition. Threshold voltage has negative temperature coefficient. Fig 7 is showing the variation in V_T in accordance with N_A and Q_{ox} at room temperature.

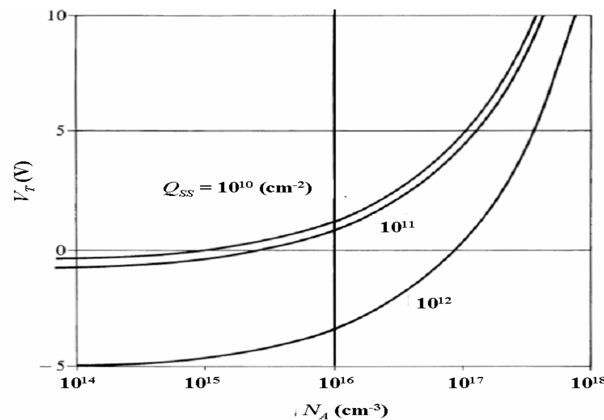

Fig. 7. The effect of N_A and Q_{ox} on V_T at room temperature

B. *On Resistance*

The total on state resistance ($R_{DS(on)}$) of a vdmos is defined as the sum of various different resistances i.e. the resistance of the inverted channel (R_{CH}), the spreading resistance of the accumulation region formed in the surface of the epilayer (R_A), the resistance of the bulk semiconductor – the drain region (R_{D0}), and the resistance of the substrate (R_{Sub}).

$$R_{DS(on)} = R_{CH} + R_A + R_{D0} + R_{SUB}$$
eq. (1)

where R_D and R_J, affects the on state resistance more at high voltages because higher resistivity (low doped) and thickness values in the epilayer are required for higher voltage devices. R_{SUB} can be ignored at higher voltages. R_{CH} affects more R_{DS} at lower voltages. At lower value of $R_{DS(on)}$, on-state power loss is minimum and current rating is maximum of the device. It results with superior power-switching performance since the voltage drop from drain to source is also minimized for a given value of drain-to-source current [4]. $R_{DS(on)}$ is dependent on the temperature as the mobility of holes and electrons decreases as temperature increases

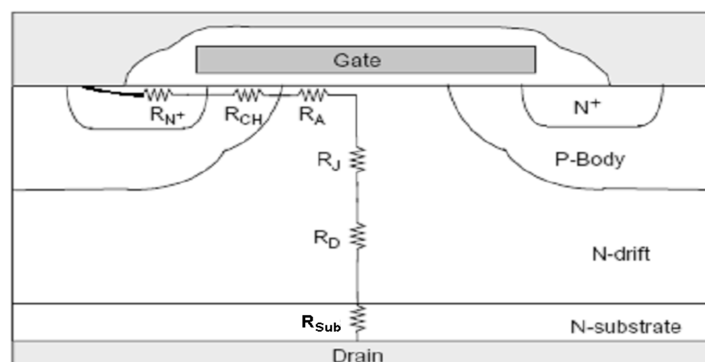

Fig. 8. A VDMOS transistor showing its internal resistances ($R_{DS(on)}$)[6]

C. *Breakdown Voltage*

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Breakdown voltage (B_{VDSS}) is the maximum voltage between drain to source that a MOS transistor can hold without causing avalanche breakdown of the pn junction formed at the body-drain region in the off-state. There are five important elements that controls breakdown i.e. avalanche, reach-through, punch-through, Zener and dielectric breakdown [6].

Voltage blocking in vdmos is structured between the p- body region and the n- epilayer region (region C and D in Fig. 6). In the case of an n-channel, enhancement mode vdmos, almost all the blocking voltage (breakdown voltage limit) is supported by n-epilayer that is why B_{VDSS} depends doping profile and thickness of n-epilayer. To produce a higher breakdown voltage, both the resistivity and the thickness of the n- epilayer need to be increased [12]. Fig.9 shows the effect of doping concentration and thickness for the n- epilayer on the B_{VDSS}.

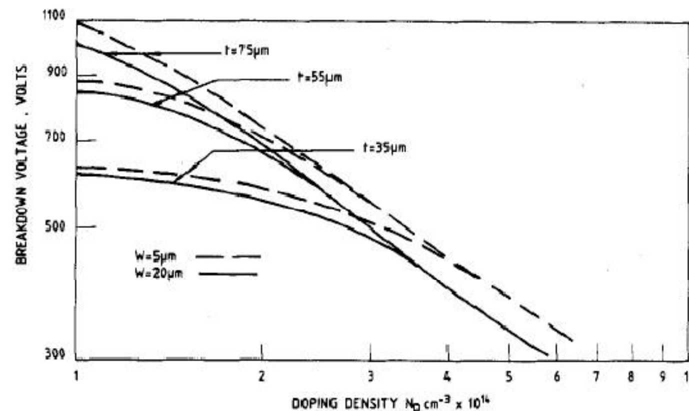

Fig. 9. B_{VDSS} vs. doping concentration density and thickness of n- epilayer

Breakdown voltage also depends on the shape of the junction and the structure of the region where the junction encounter the semiconductor surface. This is due to the change in electric field at the edge of junctions. As the electric field is increased, the breakdown voltage of a device decreases.

IV.CAPACITIVE ELEMENTS & DYNAMIC BEHAVIOR

The high frequency interpretation of a vdmos is decided by the time required to create voltage changes across capacitances. That is why having knowledge about the internal capacitance of a vdmos is important. The capacitances incorporate C_{GS} (the capacitance between gate electrodes to the source region; independent of applied voltage), C_{DS}(the capacitance between the n+ drain to source region; inversely proportional to the square root of V_{DS}), and C_{GD} (the capacitance between the gate electrodes to the n+ drain region is a nonlinear function of voltage due to variation in n-depletion). Three capacitances mostly used are the input capacitance (C_{ISS}), the output capacitance (C_{OSS}), and the reverse transfer (or Miller) capacitance (C_{RSS}). C_{ISS} is the parallel combination of C_{GD} and C_{GS}. C_{OSS} is the parallel combination of C_{DS} and C_{GD}. C_{RSS} is same as C_{GD}.

C_{OSS} is mainly a junction capacitance of a diode formed between the p- body region and the n epilayer. The value of this capacitance is highest when no V_{DS} is applied. When the drain voltage is increased, the depletion width increases, which results in decreasing of the capacitance fast because capacitance is inversely proportional to distance between the plates. C_{ISS} does not vary when drain to source/body bias is changed. This capacitance is mostly developed between source metal interconnects to gate material. For a low input capacitance value, the oxide thickness can be increased. In spite of small in value, gate to source overlap capacitance and gate to channel capacitance also contribute to C_{ISS} [16]. Although C_{RSS} has the lowest capacitance value among the three capacitances and have the greatest effect on RF performance. It provides a negative feedback loop between the output and the input of the circuit, which can roll off the frequency response.

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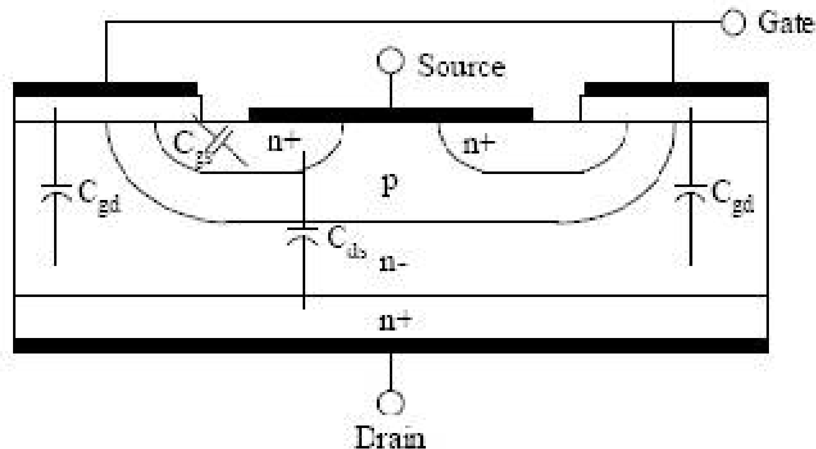

Fig. 10. The Internal capacitances of a vdmos [17]

The maximum operating frequency of power MOS transistors can be found using equation

$$f_{max} \leq \frac{1}{\pi(ton+toff)} \quad \text{eq. (3)}$$

where ton is the overall turn-on time and toff is the overall turn-off time [1]. Before the device begins to turn on, C_{ISS} must be charged to the threshold voltage and discharged to the certain voltage before the device turns off. For this reason, C_{ISS} has a direct effect on the turn-on and turn-off time of the device. If C_{GS} and C_{GD} can be reduced, it is possible to work in the high frequency regime. Fmax is directly proportional to G_{FS} and inversely proportional to C_{ISS}. Fig 10 shows the internal capacitance of vdmos.

V. VDMOS PARASITIC BJT

A vdmos has a parasitic BJT as an internal element of its structure. The n+ source terminal correlates with the n-type emitter, the p- body region correlates with the p-type base, and the n-type drain correlates with to the n-type collector. Vdmos will completely short –circuit if the parasitic BJT turns on. So it must be made certain that the parasitic device is in cut-off mode at all times. By shorting the source (emitter) and body (base) regions, parasitic device conquers in static mode of operation resulting in stopping the device from ever creating an emitter-base voltage [7]. However, the parasitic BJT can commence during the high-speed switching operation of the vdmos. The rate of the rise of the V_{DS} can be very high in the inductive load circuits.

There is a voltage drop between the drain and the source region when the rate of increasing V_{DS} is large at turn off state of high-speed switching device which creates a displacement current through C_{BD} (the capacitance between the base of the BJT and the drain of the MOSFET) which is induced by charging and discharging of capacitor. This induced current now transfers to R_{BB}. If the voltage drop across R_{BB} exceeds about 0.6 V, it is sufficient to make forward bias the base-emitter junction of BJT which results in turning on the parasitic BJT [7]. Due to this, the breakdown voltage of the vdmos is limited to that of the open base breakdown voltage of the BJT. Vdmos will enter the avalanche state if the applied V_{DS} is higher than the open base breakdown voltage of BJT and may be demolished if the current is not limited externally [3]. Fig 11 shows the cross section of vdmos showing parasitic BJT.

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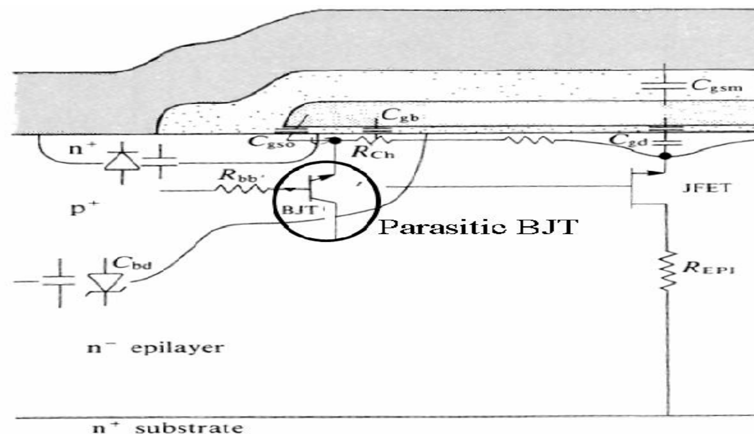

Fig. 11. The cross-section of a VDMOS showing a parasitic BJT

VI. CONCLUSION

The parasitic BJT effect in vdmos can be reduced by implanting higher doping diffusion in p-region which reduces the R_{BB} value. This extra implantation has no effect on the other characteristics of the device. This extra implant is known as UIS (unclamped inductive switching) implant. It is used to verify the vdmos operation and resistance against this parasitic effect.

REFERENCES

1. V. Benda, J. Gower , and D. A. Grant, Power Semiconductor Devices: Theory and Applications, Chichester: John Wiley & Sons, Inc, 1999.
2. K. S. Oh, "IGBT Basics 1: Application Note 9016," Fairchild Semiconductor, February 2001.
3. V. Barkhordarian. "Power MOSFET Basics: AN1084," International Rectifier, July 2000.
4. "Understanding Power MOSFETs: Application Note An-7500," Fairchild Semiconductor, October1999.
5. C. G. Jambotkar. "Power Field Effect Transistor." U.S. Patent 4,145,700, March20, 1979.
6. K. S. Oh, "MOSFET Basics: AN9010" Fairchild Semiconductor, July 2000.
7. D. A. Grant and J. Gowar, Power MOSFET: Theory and Applications, New York: John Wiley & Sons, Inc, 1989.
8. Y. Tarui, Y. Hayashi, and T. Sekigawa, "Diffusion self-aligned MOST: A new approach for high speed devices." Proc. Conf. Solid State Devices 1, 105 110,1969.
9. P. H. Wilson. "A Novel High Voltage RF Vertical MOSFET for High Power Applications," IEEE, pg 95-100, 2002.
10. M. Trivedi and K. Shenai. "Comparison of RF Performance of Vertical and Lateral DMOSFET," IEEE, pg 245-8, 1999.
11. "The RF MOSFET Line. RF Power Field-Effect Transistor: N-Channel Enhancement-Mode," Tyco Electronics.
12. "Power Semiconductor Applications," Philips Semiconductors, pg 21.
13. D. A. Neamen. Semiconductor Physics and Devices. Boston: McGraw-Hill, 2003.
14. M. N. Darwish and K. Board. "Optimization of Breakdown Voltage and On- Resistance of VDMOS Transistors," IEEE Transactions on Electron Devices, Vol. ED-31, No. 12, pg 1769-1775, 1984.
15. J. Dodge. "Power MOSFET Tutorial," Application Note: APT-0403, pg. 1-12, March 2006.
16. S. K. Leong. "Obtaining DMOS Power RF Transistor Information from Published Data Sheets." RF featured technology, pg. 26-32, 1993.
17. A. Grimaldi, A. Schiliaci, A. Vitanza, and E. Romano. "Ruggedness Improvement of RF DMOS Devices: AN1232," July 2000.
18. F. Frisina. "Fabrication of VDMOS Structure with Reduced Parasitic Effects," U.S. Patent 6,391,723, May 21, 2002.
19. L. A. Goodman and A. M. Goodman. "Method for Making Vertical MOSFET with Reduced Bipolar Effects," U.S. Patent 4587,713, May 13, 1986.
20. C. Contiero, A. Andreini, and M. Galbiati. "Self-Aligned Process for Fabricating small DMOS Cells," U.S. Patent 4,774,198, Sep. 27, 1988.
21. J. D. Plummer, M. D. Deal, and P. B. Griffin. Silicon VLSI Technology .Fundamentals, Practice and Modeling. New Jersey: Prentice Hall, 2000.

BIOGRAPHY

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