ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2016

A Review on Fully Utilized Architecture for FM0, Manchester and Miller Encoding Using SOLS Technique

S.P.Ramekar[1], Dr.P.N.Chatur[2]

M. Tech Student. Department of ENTC , Government College of Engineering, Amravati, Maharashtra, India[1]

Head of Department, Department of CSE, Government College of Engineering, Amravati, Maharashtra, India[2]

ABSTRACT: The dedicated short-range communication (DSRC) is an emerging technique in the intelligent transportation system. The DSRC standards generally adopt FM0 and Manchester codes for secure communication, dc-balance and enhancing the signal reliability. But because of the coding-diversity between FM0 and Manchester codes the potential to design a fully reused VLSI architecture for both is restricted. Hence, proposed method adopts similarity oriented logic simplification SOLS technique which merges architecture together and synchronize the operation. The technique proposed is an integrated architecture of FM0, Manchester encoding to overcome various drawbacks of traditional method. This deduced architecture of FM0 and Manchester coding would well support the DSRC standards. The performance of this method will be evaluated on Xilinx FPGA Spartan-3E kit. Proposed work not only develops a fully reused VLSI architecture, but also provides an effective performance compared with existing works.

KEYWORDS: Dedicated Short Range Communication (DSRC), FM0, Manchester, Miller, Similarity Orientation Logic Simplification (SOLS).

I. INTRODUCTION

Over the last two decades, the United States Department of Transportation (USDOT) has conducted extensive research on the effectiveness of vehicle-based collision counter measures for rear-end, road departure, and lane change crashes. Field Operational Tests (FOTs) of rear-end and road departure collision warning systems have shown measurable benefits in reduction of crashes. However, vehicle-to-vehicle (V2V) wireless communications and vehicle positioning may enable improved safety system effectiveness by complementing or in some instances, providing alternative approaches to the traditional, autonomous sensing based safety equipment.

Dedicated short range communication is a medium range communication protocol. This protocol is mainly used for intelligent transportation system. DSRC block diagram is shown in figure 1. This is used for applications such as message sending and broadcasting among automobiles for safety issues and public information announcement such as blind spot, intersection warning, inter-cars distance and collision-alarm.

DSRC also supports vehicle to sideway communication, which includes Electronic Toll Collecting (ETC). With ETC, the toll collecting is electrically accomplished with the contactless IC-card platform. Moreover, the ETC can be extended to the payment for parking-service and gas-refueling. Thus, the DSRC system plays an important role in modern automobile industry. The upper and bottom parts are dedicated for transmission and receiving respectively. This Transceiver is classified into three basic modules: microprocessor, baseband processing and RF front-end.

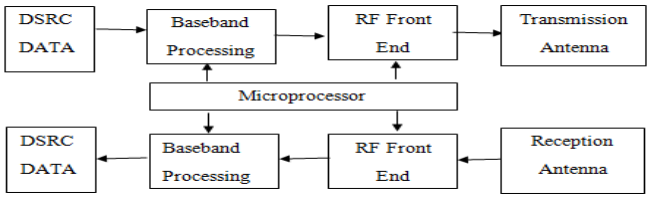

Figure 1: DSRC system architecture

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2016

The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization and encoding. The RF front end transmits and receives the wireless signal through the antenna. The DSRC standards have been established by several organizations in different countries. The data rate individually targets at 500 kb/s, 4 Mb/s and 27 Mb/s with carrier frequency of 5.8 and 5.9 GHz.

Table 1: Profile of DSRC Standards for America, Europe and Japan

	Europe	America	Japan
Organization	CEN[1]	ASTM[2]	ARIB[3]
Data Rate	500 kbps	27 Mbps	4 Mbps
Carrier Frequency	5.8 Ghz	5.9 Ghz	5.8 Ghz
Modulation	ASK, PSK	OFDM	ASK
Encoding (Downlink)	FM0	Manchester	Manchester

1. European Committee for Standardization
2. American Society for Testing and Materials
3. Association of Radio Industries and Businesses

The modulation methods incorporate amplitude shift keying, phase shift keying and orthogonal frequency division multiplexing. Comparison of DSRC in different countries is shown in table 1. Generally, the waveform of transmitted signal is expected to have zero mean for robustness issue and this is also referred to as dc-balance. The transmitted signal consists of arbitrary binary sequence, which is difficult to obtain dc-balance. The purpose of FM0 and Manchester codes is to provide the transmitted signal with dc-balance. Both FM0 and Manchester codes are widely adopted in encoding for downlink.

II. CODING PRINCIPLES OF FM0, MANCHESTER AND MILLER ENCODING

A. FM0 encoding

FM0 encoding is also called as bi-phase space encoding scheme. In FM0 encoding of the signal to be transmitted is done according to the following rules as shown in figure 2.

1) For representing logic '0' level, it inverts the signal at the mid of the symbol.
2) For representing logic '1' level, it gives constant voltage occupying an entire bit window.
3) It inverts the phase of the baseband signal at the boundary of each symbol.

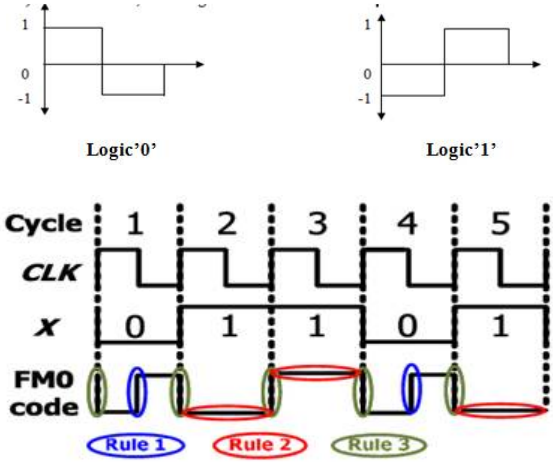

Figure 2. FM0 basis Functions and FM0 encoding example[1]

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2016

B. Manchester Encoding

Manchester code be first developed by G.E. Thomas at 1949. It is also called as phase encoding scheme. In Manchester encoding, the encoding of the signal to be transmitted is done according (Figure 3) to the following rules,

1) A '1' is noted, when low to high transition occurs.
2) A '0' is noted, when high to low transition occurs.

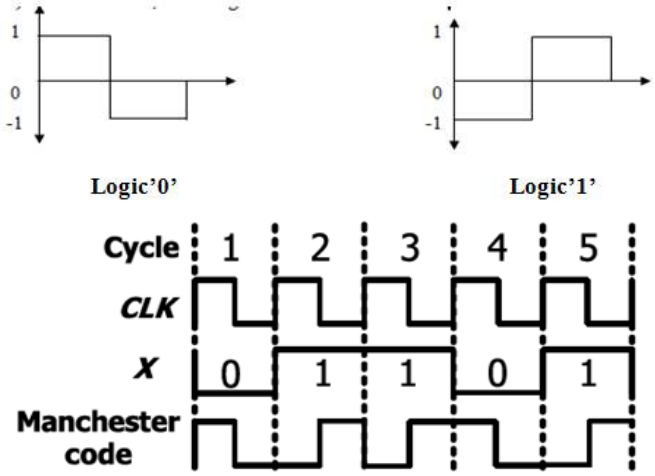

Figure3. Manchester basis Functions and encoded signal [1]

C. Miller encoding

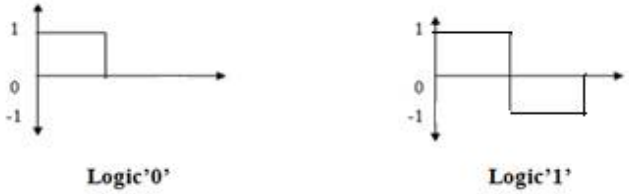

Figure4. Miller basis Functions[3]

The fully reused VLSI architecture using the similarity oriented logic simplification (SOLS) technique for both FM0, Manchester encodings is proposed in this synopsis. The SOLS technique eliminates the limitation on hardware utilization by two core techniques, area compact retiming and balance logic-operation sharing. The SOL technique improves the hardware utilization rate for both FM0 and Manchester encodings.

III. RELATED WORK

To promote intelligent and smart transportation services into our daily life the dedicated short range communication is an advanced technique. Data encoding techniques like FM0 and Manchester encoders are used to promote communication among vehicles. These encoding techniques generally works at transistor level hence the transmitted signal reach with dc-balance, enhance the signal reliability. In existing works the design has the limitation that it does not support fully reused VLSI architectures. To rectify these problems, the FM0 and Manchester encoders are needed to be design with SOLS technique to achieve high speed and fully reused VLSI architectures for DSRC application systems.

1. The literature [1] proposes the fully reused VLSI architecture of FM0/Manchester encoding using similarity oriented logic simplification (SOLS) technique for Dedicated short range communication. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2016

2. The literature [2] derives application level reliability metrics of various safety applications with worst-case settings and vehicular environments based on an accurate analytical model in one dimension vehicular communication networks.
3. The literature [3] gives a review of emerging vehicle safety wireless communications due to the occurrence of many accidents when distant objects or roadway impediments are not detected quickly.
4. The literature [4] analyzed to reduce the number of components. Using the both code to reduce the power, delay, area in DSRC. The power consumption is 29392.843nW forManchester and fm0 encoding, and area is 203μM².
5. The literature [5] provides joint detection and verification of frequency shift keying (FSK) modulation and demodulation (MODEM), Manchester coding and decoding (CODEC) schemes are proposed for dedicated short range communication (DSRC) systems over high mobility fading channels.
6. The literature [10] proposes a modified Manchester and Miller encoder that can operate in high frequency without a sophisticated circuit structure.

INITIAL HARDWARE ARCHITECTURE OF FM0 AND MANCHESTER ENCODING:

The hardware architecture of Manchester encoding is as simple as XOR operation. However, the hardware architecture for FM0 is not as simple as that of Manchester.

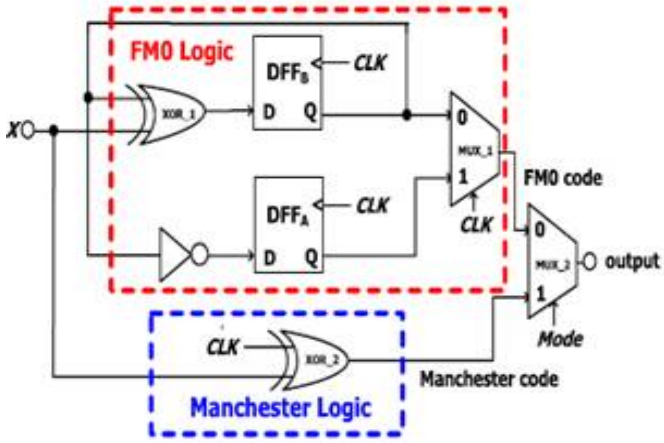

Figure 5. Initial Hardware architecture of FM0 and Manchester encoding[1]

Initial hardware architecture of FM0 and Manchester encoder is shown in the figure 5. The top part is the hardware architecture of FM0 encoder and the bottom part is hardware architecture of Manchester encoder. The Qa and Qb store the state code of the FM0 code. The Mux_1 is to switch Qa and Qb through selection of clock (CLK) signal. The determination of which coding is adopted depends on the mode selection of Mux_2, where the mode=0 is for FM0 code and mode=1 is for Manchester code. Truth table of FM0 code is as shown in table 2.

Therefore equations for output of Manchester encoder is given as,

$$o/p = x * clk$$

and output equation for FM0 encoding is given as,

$$A(t) = \overline{B(t-1)}$$

$$B(t) = X \oplus B(t-1)$$

With both A(t) and B(t), the Boolean function of FM0 code is denoted as

$$o/p = CLK\ A(t) + \overline{CLK}\ B(t)$$

To evaluate the hardware utilization, the hardware utilization rate (HUR) is defined as

$$HUR = \frac{\text{Active components}}{\text{Total components}} \times 100\%.$$

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2016

Table 2: TRANSITION TABLE OF FM0

Previous-state		Current-state			
		$A(t)$		$B(t)$	
$A(t-1)$	$B(t-1)$	$X=0$	$X=1$	$X=0$	$X=1$
1	1	0	0	1	0
1	0	1	1	0	1
0	1	0	0	1	0
0	0	1	1	0	1

The active components mean the components that work for FM0 or Manchester encoding. The total components are the number of components in the entire hardware architecture no matter what encoding method is adopted. The HUR of FM0 and Manchester encodings is listed in Table 3.

TABLE3: HUR of FM0 and Manchester encoding[1]

Coding	Active components (transistor count) / Total components (transistor count)	HUR
FM0	6 (86) / 7 (98)	85.71%
Manchester	2 (26) / 7 (98)	28.57%
Average	4 (56) / 7 (98)	57.14%

For both encoding methods, the total components are 7, including MUX−2 to indicate which coding method is activated. For FM0 encoding, the active components are 6 and its HUR is 85.71%. For Manchester encoding, the active components are 2, comprising XOR−2 and MUX−2. Its HUR is as low as 28.57%. On average, this hardware architecture has a poor HUR of 57.14% and almost half of total components are wasted. The transistor count of the hardware architecture without SOLS technique is 98, where 86 transistors are for FM0 encoding and 26 transistors are for Manchester coding. On average, only 56 transistors can be reused and this is consistent with its HUR.

IV. PROPOSED ALGORITHM

Above problem can be solve by using similarity oriented logic simplification method(SOLS). The purpose of SOLS technique is to design a fully reused VLSI architecture for FM0 and Manchester encodings. The SOLS technique is classified into two parts: area-compact retiming and balance logic-operation sharing.

A. Area-Compact Retiming

Illustration of area-compact retiming on FM0 encoding technique is shown in Fig

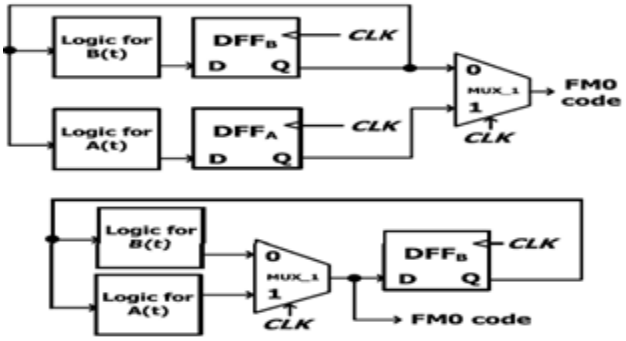

Fig.6. FM0 encoding with area compact retiming[1]

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2016

For FM0, the state code of each state is stored into DFFA and DFFB. But the architecture requires a single 1 bit flip-flop to store the states. Removal of DFFA causes the logic fault of FM0 code due to non-synchronization between A(t) and B(t). DFFB is relocated after mux_1 to avoid logic faults. The transistor count of the FM0 encoding architecture without area-compact retiming is 72 and that with area-compact retiming is 50. The area-compact retiming technique reduces 22 transistors. Thus the area-compact retiming relocates the hardware resource to reduce 22 transistors.

B. Balance Logic-Operation Sharing

The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. It is illustrated in the Fig 7.

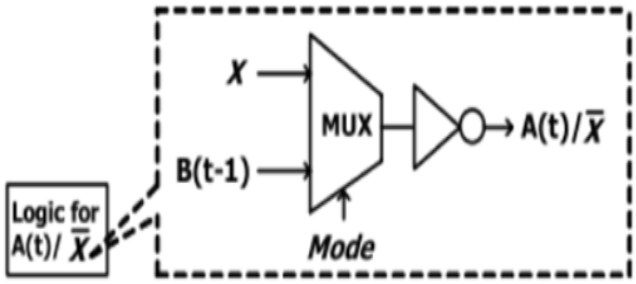

Fig7. Balance Logic operation sharing[3]

As seen before FM0 encoding is given by following equations,

$$FM0 = CLK\ A(t) + \overline{CLK}\ B(t)$$

And Manchester encoded output is given by,

$$X \oplus CLK = CLK\ \overline{X} + \overline{CLK}\ X$$

The concept of balance logic-operation sharing is to integrate the $\overline{X}$ into A(t) and X into B(t) respectively. The logic for A(t)/$\overline{X}$ is shown in Fig.7. The A(t) can be derived from an inverter of B(t −1), and $\overline{X}$ is obtained by an inverter of X. The logic for A(t)/$\overline{X}$ can share the same inverter, and then a multiplexer is placed before the inverter to switch the operands of B(t −1) and X. The Mode indicates either FM0 or Manchester encoding is adopted. By analyzing the two core concepts of SOLS technique the VLSI architecture of FM0 and Manchester encoding is shown in Fig 8.

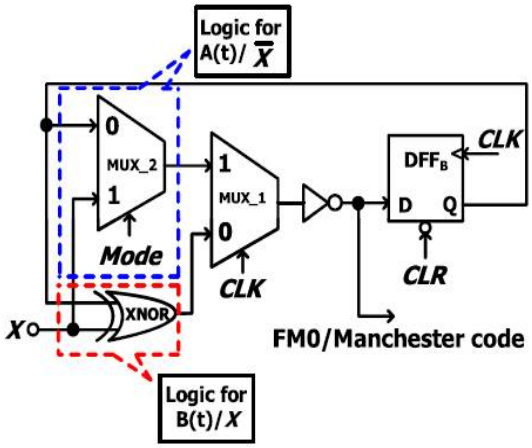

Fig.8:Balance computation time VLSI architecture of FM0 and Manchester encoding.[1]

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 2, February 2016

The computation time of MUX−2 is nearly equal to that of XOR in the logic for B(t)/X. The logic for A(t)/$\overline{X}$ also contains an inverter in the series of MUX−2. This unbalance computation time between A(t)/X and B(t)/X results in the glitch at the input of MUX−1, this can cause logic-fault on coding. To alleviate this problem in computation time, the architecture of the balance computation time between A(t)/X and B(t)/X is shown in Fig. 8. The XOR in the logic for *B(t)/X* is converted into the XNOR with an inverter, and then this inverter isshared with that of the logic for *A(t)/X*. This shared inverter is given backward to the output of MUX−1. Thus, thelogic computation time between A(t)/X and B(t)/X is morebalance to each other. The adoption of FM0 or Manchestercode depends on Mode and CLR signal. The CLR furtherperforms the individual function of a hardware initialization.If the CLR is simply obtained by inverting Mode, this leads to aconflict between the coding mode selection and the hardwareinitialization. To avoid this, both Mode and CLRare separately allocated to this design froma system controller. Whether FM0 or Manchester code isadopted, allthe logic component of the proposed VLSI architectureare utilised. Every component is active in both FM0 andManchester encodings. Therefore, the HUR of the proposedVLSI architecture is greatly improved.
Using balance logic operation sharing and area compact retiming together initial architecture of FM0 and Manchester encoding can be optimize to fig.8. It is more utilized as compared to conventional architecture as conventional architecture contains 7 hardware block whereas balance computation architecture contains 5 blocks with hardware utilization ratio of 100%.

V. CONCLUSION AND FUTURE WORK

As Manchestor,FM0 and Miller are the only techniques which can be used for DSRC applications, the programming diversity between this technique make it difficult achieve 100% hardware utilization. Using SOLS technique this can be achieved. SOLS technique uses balance logic operation sharing and area compact retiming. 100% utilization is possible by using Manchester and FM0 together but adding miller encoding with it can reduce the utilization ratio.

REFERENCES

1. Yu-Hsuan Lee, Cheng-Wei Pan,"Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications", 10.1109/TVLSI.2014.2299532.
2. Wenfeng Li, Jun Wu, Xiaomin Ma and Zhifeng Zhang, "On reliability requirement for BSM broadcast for safety applications in DSRC system", IEEE CONFERENCE publication on Intelligent Vehicles Symposium Proceedings, pp. 946 – 950, 2014.
3. M. Abinaya , T. SuganyaThevi," Evaluation of Various Forms of DSRC System- A Review", IJESRT, ISSN: 2277-9655, [Abinaya, 3(11): November, 2014].
4. Mr.S.Prakash, K.Umadevi, Dr.V.Nagarajan," Area Efficient Encoding Technique For Reducing Power In DSRC", ISSN: 2349-7017,ISSN: 2349-7017, Volume 1 Issue 3 (September 2014)
5. J.-H. Deng, F.-C. Hsiao, and Y.-H. Lin, "Top down design of joint MODEM and CODEC detection schemes for DSRC coded-FSK systems over high mobility fading channels," in Proc. Adv. Commun. Technol. Jan. 2013, pp. 98–103
6. J. B. Kenney, "Dedicated short-range communications (DSRC) standards in the United States," Proc. IEEE, vol. 99, no. 7, pp. 1162–1182, Jul. 2011.
7. F. Ahmed-Zaid, F. Bai, S. Bai, C. Basnayake, B. Bellur, S. Brovold, et al., "Vehicle safety communications—Applications (VSC-A) final report," U.S. Dept. Trans., Nat. Highway Traffic Safety Admin., Washington, DC, USA, Rep. DOT HS 810 591, Sep. 2011.
8. A. Karagounis, A. Polyzos, B. Kotsos, and N. Assimakis, "A 90nm Manchester code generator with CMOS switches running at 2.4 GHz and 5 GHz," in Proc. 16th Int. Conf. Syst., Signals Image Process., Jun. 2009, pp. 1–4.
9. Y.-C. Hung, M.-M. Kuo, C.-K. Tung, and S.-H. Shieh, "High-speed CMOS chip design for Manchester encoder," in Proc. Intell. Inf. Hiding Multimedia Signal Process., Sep. 2009, pp. 538–541.
10. J. Daniel, V. Taliwal, A. Meier, W. Holfelder, and R. Hertwich, "Design of 5.9 GHz DSRC-based vehicular safety communication,"IEEE Wireless Commun. Mag., vol. 13, no. 5, pp. 36–43, Oct. 2006.
11. P. Benabes, A. Gauthier, and J. Oksman, "A Manchester code generator running at 1 GHz," in Proc. IEEE, Int. Conf. Electron., Circuits Syst., vol. 3. Dec. 2003, pp. 1156–1159.

BIOGRAPHY

Swapnil Pandurang Ramekarcompleted his B.E. in ENTC from JSPM's RSCOE, Pune university, currently he is pursuing M.Tech from GCOEA Amravati.

Dr. P. N. Chaturhas received his M.E.degree in Electronics Engineering from Govt. College of Engineering Amravati, India and Ph.D degree from Amravati University. His area of research includes Artificial Neural Network, Data Mining, Data Stream Mining and Cloud computing. Currently he is Head of Computer Science and Engineering Department at Govt. College of Engineering Amravati, Maharashtra Indi India. At present he is engaged with large database mining analysis and stream mining.