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Survey Paper on Multiplier-less 1-D Discrete Wavelet Transform based on ROM

Ankit Pathak, Prof Bharti Chourasia

M Tech. Scholar, Dept. of Electronics and Communication, SCOPE College of Engineering, Bhopal, India

Head of Dept, Dept. of Electronics and Communication, SCOPE College of Engineering, Bhopal, India

ABSTRACT: Conventional distributed arithmetic (DA) is popular in field programmable gate array (FPGA) design, and it features on-chip ROM to achieve high speed and regularity. In this paper, we describe high speed area efficient 1-D discrete wavelet transform (DWT) using 9/7 filter based distributed arithmetic (DA) Technique. Being area efficient architecture free of ROM, multiplication, and subtraction, DA can also expose the redundancy existing in the adder array consisting of entries of 0 and 1. This architecture supports any size of image pixel value and any level of decomposition. The parallel structure has 100% hardware utilization efficiency.

KEYWORDS: - 1-D Discrete Wavelet Transform (DWT), DA, Low Pass Filter, High Pass Filter, Xilinx Simulation.

I. INTRODUCTION

The well-known image coding standards, namely, MPEG-4 and JPEG2000 have adopted 1-D DWT as the transform coder due to its remarkable advantages over the other transforms. For lossy and lossless compression, Daubechies 9/7 orthogonal filter is used as the default wavelet filter in JPEG 2000. Efficient implementation of 1-D DWT using 9/7 filters in resource-constrained hand-held devices with capability for real-time processing of the computation-intensive multimedia applications is, therefore, a necessary challenge. Multiplier-less hardware implementation approach provides a kind of solution to this problem due to its scope for lower hardware-complexity and higher throughput of computation.

Several parallel and pipeline systems that meet the computational requirements of the discrete wavelet transform have been proposed. Some of them need multiprocessor to implement it and the system is complex, time consuming, and costly [1]. The Field programmable gate array (FPGA) provides us a new way to digital signal processing [2].

Several designs have been proposed for the multiplier, multiplier-less implementation of 1-D DWT based on the principle of multiplier based design (MBD) distributed arithmetic (DA) canonic signed digit (CSD), [1]–[3]. The structure of distributes the bits of the fixed coefficients instead of the bits of input samples. Consequently, the adder-complexity of the structure of depends on the DA-matrix of the fixed coefficients [2].

Canonic signed digit (CSD) are popular for representing a number with fewest number of non-zero digit. The CSD representation of a number contains the minimum possible number of nonzero bits, thus the name canonic. The CSD representation of a number is unique and CSD numbers cover the range (-4/3, 4/3), out of which the value in the range {-1, 1} are of greatest interest.

Martina *et al* [5] have approximated the 9/7 filter coefficients and performance of a hardware implementation of the 9/7 filter bank depends on the accuracy of coefficients representation. By that approach, they have significantly reduced the adder-complexity of the 9/7 DWT. Gourav *et al* [7] have suggested an LUT-less DA-based design for the implementation of 1-D DWT. They have eliminated the ROM cells required by the DA-based structures at the cost of additional adders and multiplexors.

Some of them need Rom to implement it and the system is complex, time consuming, and costly [4] The adder-complexity of this structure is significantly higher than the other multiplier-less structures. In this paper, we have proposed an efficient scheme to derive DA-based bit-parallel structures, for low-hardware and high-speed computation DWT using 9/7 filters [4].

The remainder of the paper is organized as follows: New efficient distributed arithmetic based computation of 1-D DWT using 9/7 filter is presented in Section II. The proposed structures are presented in Section III. Hardware and time complexity of the proposed structures are discussed and compared with the existing structures in Section IV. Conclusion is presented in Section V.

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II. DISTRIBUTED ARITHMETRIC (DA)

Let us consider the following sum of products [4]:

$$R = \sum_{k=1}^{L} X_k \times Y_k \qquad (1)$$

Where X_k are fixed coefficients and they Y_k are the input data words. Equation (1) can be expressed in the form of a matrix product as:

$$R = \begin{bmatrix} X_1 & X_2 & \dots & X_L \end{bmatrix} \begin{bmatrix} Y_1 \\ Y_2 \\ . \\ Y_L \end{bmatrix} \qquad (2)$$

Both X_k and Y_k are in two's complement format. The two's complement representation of X_k may be expressed as

$$X_k = -X_k^M 2^M + \sum_{i=N}^{M-1} X_k^i 2^i \qquad (3)$$

Where $X_k^i = 0$ or 1, and $i =$ N, N+1… M and X_k^M is the sign bit and X_k^N is the least significant bit (LSB).
Equation (3) can be expressed in matrix form as:

$$X_k = \begin{bmatrix} 2^N & 2^{N+1} & \dots & 2^M \end{bmatrix} \begin{bmatrix} X_k^N \\ X_k^{N+1} \\ . \\ -X_k^M \end{bmatrix} \qquad (4)$$

Similarly Y_k can be represented in two's complemented format as:

$$Y_k = -Y_k^X 2^X + \sum_{i=W}^{X-1} Y_k^i 2^i \qquad (5)$$

Where $Y_k^i = 0$ or 1, and $i =$ W, W+1, …,X and Y_k^M is the sign bit and Y_k^N is the least significant bit (LSB).

Now on combining equations (1) and (3), we get-

$$R = -(R^M .2^M) + \sum_{i=N}^{M-1} (R^i .2^i) \qquad (6)$$

Where

$$R^i = \sum_{k=1}^{L} X_k^i Y_k \,,\ i = \text{N, N+1… M}$$

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III. PROPOSED ARCHITECTURE

In this paper, we have proposed a high speed area efficient multiplier-less 1-D 9/7 wavelet filters based DA technique. 9/7 wavelet filters coefficient i.e. 9 low-pass and 7 high-pass wavelet filters coefficient are given in table1. We multiply the filter coefficients by 128 for simplification. The mathematical calculation for 1-D high pass filter output is explained by an example.

Table 1: Show high-pass and low-pass wavelet filters coefficient.

	Wavelet filters coefficients	Multiplied by 128	7 bit binary representation
h_0	0.60294901823	77	1001101
h_1	0.26686441184	34	0100010
h_2	0.07822326652	10	0001010
h_3	0.01686411844	2	0000010
h_4	0.026748757410	3	0000011
g_0	0.55754352622	71	1000111
g_1	0.29563588155	38	0100110
g_2	0.02877176311	4	0000100
g_3	0.045635881557	6	0000110

Where $h_0, h_1, h_2, h_3,\ h_4$ are the Low pass filter coefficients and g_0, g_1, g_2, g_3 are the High pass filter coefficients. If we take the high pass coefficients g_0, g_1, g_2 and g_3 multiply by r_1, r_2, r_3 and r_4 then we get the High pass output Y_H of the 9/7 filter as [6]:

$$Y_H = \begin{bmatrix} g_0 & g_1 & g_2 & g_3 \end{bmatrix} \begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{bmatrix} \qquad (7)$$

Where

$$r_1 = Y(n) + Y(n-6)$$
$$r_2 = Y(n-1) + Y(n-5)$$
$$r_3 = Y(n-2) + Y(n-4)$$
$$r_4 = Y(n-3)$$

Let r_1=1, r_2=2, r_3=3, r_4=4 then

$$Y_H = \begin{bmatrix} 71 & 38 & 4 & 6 \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} = 183 \qquad (8)$$

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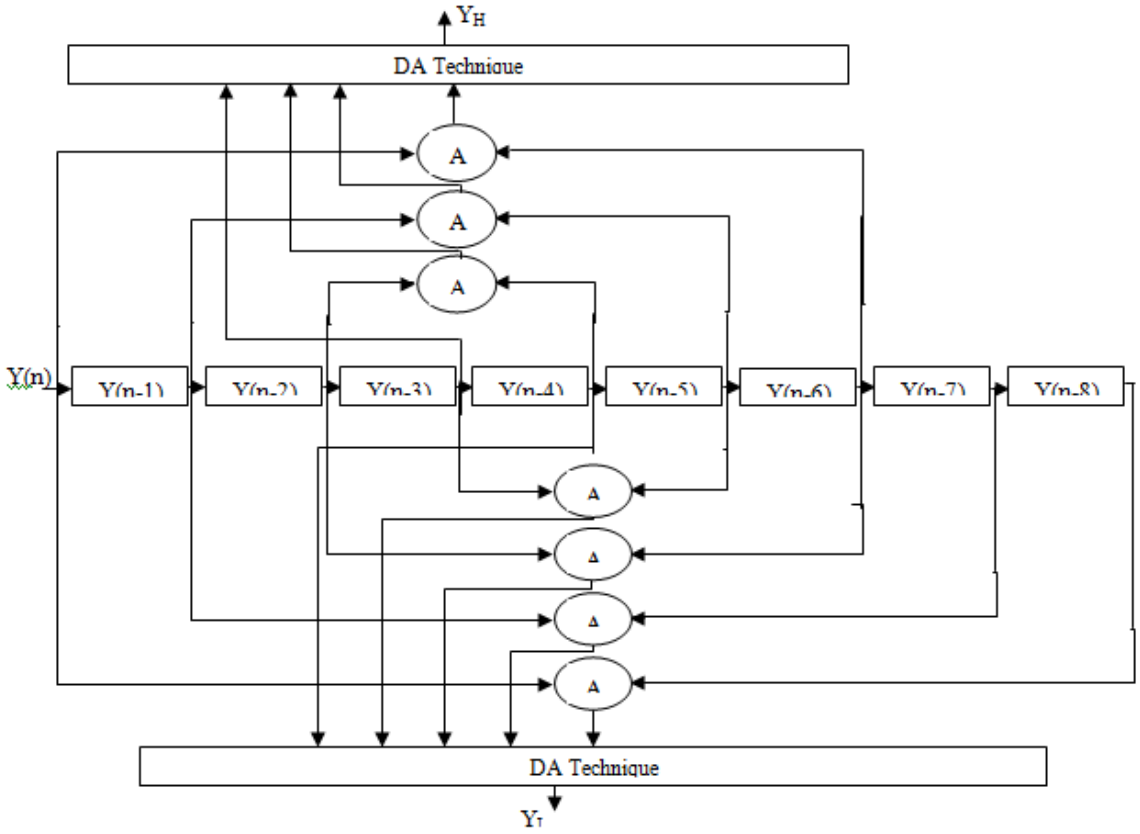

Figure 1: Proposed Multiplier-less 9/7 Wavelet filter using DA Technique

Now if we implement this with DA then

$$Y_H = \begin{bmatrix} 1000111 & 0100110 & 0000100 & 0000110 \end{bmatrix} \begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{bmatrix} \quad (9)$$

Now we can make the DA matrix by the filter coefficients as

$$[B_k] = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \quad (10)$$

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$$Y_H = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} r_1 \\ r_2 \\ r_3 \\ r_4 \end{bmatrix} = \begin{bmatrix} r_1 \\ r_1 + r_2 + r_4 \\ r_1 + r_2 + r_3 + r_4 \\ 0 \\ 0 \\ r_2 \\ r_1 \end{bmatrix} \quad (11)$$

In Figure 2, apply DA techniques step-1 all the input converts' binary number, Step-2 all the binary input applied to a adder array so,

$P_1 = 0001,$ $P_2 = 0111$

$P_3 = 1010,$ $P_4 = 0000$

$P_5 = 0000,$ $P_6 = 0010$

$P_7 = 0001$

The entire adder array input applied to MUX so, the entire adder array input $m(1)$

MUX (1) = 0001 =Y_p (0)

MUX (1) add MUX (2) = Y_P (1)

= 00001
= 01110
+ 01111

Output of the Y_P (1) again right shift 1-bit and adds MUX (3) so

= 001111
= 101000
+ 110111

Y_P (1) + MUX (3) = Y_P (2)

Output of the Y_P (2) again right shift 1-bit and adds MUX (6) so

= 000110111
= 001000000
+ 001110111

Y_P (2) + MUX (6) = Y_P (3)

Output of the Y_P (3) again right shift 1-bit and adds MUX (7) so

= 001110111
= 001000000
+ 010110111

Y_P (3) + MUX (6) = Y_P (4)

Total output Y_P (4) = 010110111 = 183

IV. CONCLUSION

We propose a novel distributed arithmetic paradigm named DA for VLSI implementation of digital signal processing (DSP) algorithms involving inner product of vectors and vector-matrix multiplication. Mathematical proof is given for the validity of the DA scheme. We demonstrate that DA is a very efficient architecture with adders as the main

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component and free of ROM (free memory), multiplication, and subtraction. For the adder array, a systematic approach is introduced to remove the potential redundancy so that minimum additions are necessary. DA is an accuracy preserving scheme and capable of maintaining a satisfactory performance even at low DA precision.

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