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Low-Power High Throughput ICT Architecture for H.264 Video Encoding

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ABSTRACT*:* H.264 is one of the latest Advanced Video Coding of International Telecommunication Union (ITU-T) and Moving Picture Group (MPEG) aimed at reduction in bandwidth and improve video quality [1]. In this proposed paper a low-power high throughput H.264/AVC Integer Cosine Transform is implemented. The proposed design is a parallel structure 2-D transform, eliminating the need for a transpose memory (row-column buffer). The proposed design consumes less power and gives output in a single clock. The Proposed algorithm and architecture is implemented using Verilog HDL V.2001 and RTL schematic of the proposed Integer Cosine Transform is done using CMOS technology. A throughput of 4 G-pixels/s with a 4.04K gate count was achieved.

KEYWORDS*: Lossy and lossless Compression,* Integer Cosine Transform (ICT), H.264/AVC core transform, Spatial redundancy, temporal redundancy, Parallel 2-D ICT.

I. INTRODUCTION

Uncompressed video take huge amount of storage data and bit rate exceed 1Gbps during transmission and hence videos must be compressed before they are stored or transmitted. Two types of compression techniques which exist are lossy and lossless compression. In lossless compression, no data is lost during the process of compression. In lossy compression some data is lost during the process of compression. Compression ratio of lossless methods such as LZW, Huffman encoding is too low and hence lossy compression is predominantly used. MPEG1, MPEG2, MPEG3, MPEG4 are few popular coding standards. MPEG4-Part 10 is popularly known as H.264. H264 is widely used in broadcast, internet, consumer electronics, mobile and security industries [1],[2]. It has a number of advantages compared to previous standards [3]. The H.264 AVC introduces a reduction of bit-rate by 50% compared to MPEG-2 video coding standard. It also is suited to encoding high quality video and is resistant to errors. The network abstraction layer enables transmission of H.264 encoded video bit streams across multiple networks.

In H.264 there are 3 operations on video frames which carry out compression in H.264 video encoder are predictor, transform/quantization and entropy encoding. While predictor and entropy encoder perform lossless compression, transform/quantization results in lossy compression. There are two types of redundancies in video frames namely spatial redundancy and temporal redundancy. While the former redundancy corresponds to redundancy in neighbouring pixel groups, later corresponds to redundancies present between successive video frames. The H.264 predictor makes use of intra prediction to remove spatial redundancy and inter prediction to remove temporal redundancy which exists between multiple frames in a video sequence. [8]

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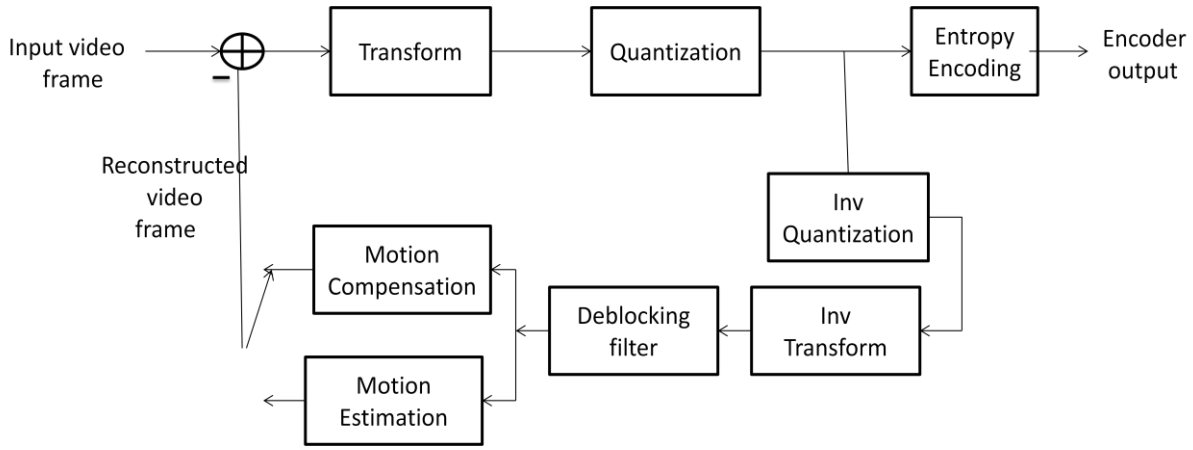

Figure. 1 H.264 Encoder block diagram

Figure. 1 represents block diagram of H.264 encoder .The input video frame and reconstructed video frames are subtracted from each other. Obtaining difference which is called as residue is subjected to ICT and quantization. Thus obtained quantised residue is finally subjected to entropy encoding.

The residue is passed on to the integer transform block, which performs conversion of pixel data from time domain to transform domain. It is then, quantised using a dynamically changing Quantization Parameter (QP). The quantised data is then entropy encoded using Variable length Huffman encoder. The coded frame along with control information is then transmitted to the decoder side at the receiver. Also, the encoded frame goes through an inverse path consisting of inverse quantization and inverse transform and is then added to the predicted frame to obtain the reconstructed frame. This is then filtered using an in-loop de-blocking filter and used for inter prediction. The video bit stream is processed in units of macroblock (MB) corresponding to 4X4 or 8X8 displayed pixels. In the encoder, a predicted macroblock is generated and subtracted from the current macroblock to form a residual macroblock; this is transformed, quantized and encoded. H264 uses the Y:Cr:Cb colour space, where only the luma (Y) and red and blue chroma (Cr, Cb) are transmitted. Y:Cr:Cb has an important advantage over RGB, in that the Cr and Cb components may be represented with a lower resolution than Y because the HVS is less sensitive to colour than luminance. This introduces data compression in chrominance components without having an obvious effect on visual quality.

Earlier standards such as JPEG, MPEG-2 Video and MPEG-4 Visual specify Discrete Cosine Transform (2-D DCT) to be applied to source or residual image data. However, the implementation of DCT on a practical processor requires approximations to certain irrational multiplication factors such as $\cos(a\pi/2N)$. This may causes the mismatch between encoder and decoder. In order to avoid this mismatch and to minimize computational complexity so as to be suitable for implementation using limited-precision integer arithmetic, in H.264, the transform and quantization processes are designed using a core transform i.e. an integer transform [9].

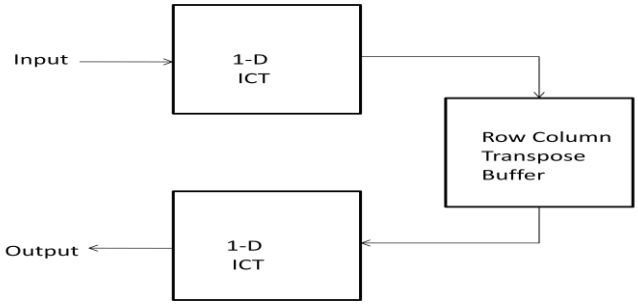

Figure. 2 Two Dimension – ICT module with Row column transpose buffer

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Figure. 2 represents a 2-D ICT with row column transpose memory buffer. This essentially consists of transistor memory with multiplexers which are used to obtain the transpose of the 4x4 residue matrix.

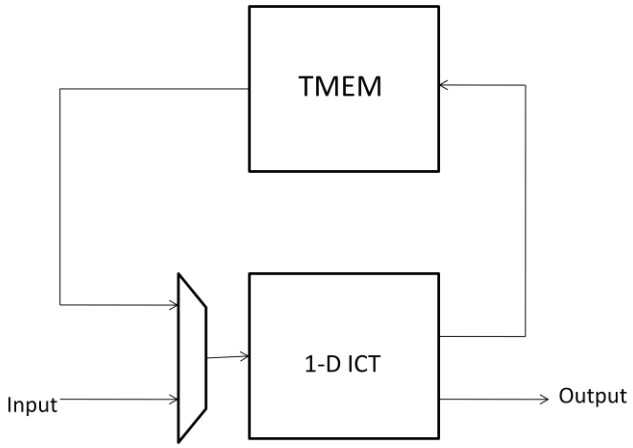

Figure 3. 2D – ICT module with Transpose memory module.

Figure.3 depicts 2D- ICT with one ICT core and a transpose RAM buffer. After subjecting the residue to 1D integer cosine transformation, the results are stored in transpose RAM. This is again subjected to second 1D transform by the ICT core module.

There have been different designs proposed to implement the ICT [4]. The popular methods are: direct 2-D and using a transpose buffer memory. [4] Implements ICT using a direct 2-D approach while [5] has used a transpose buffer memory by row-column decomposition method. The main disadvantage of using transpose buffer memory is that it does not facilitate single clock cycle execution, thus reduces the processing speed for each macro-block of residual image data. In this paper, we propose a low-power high throughput H.264/AVC Integer Cosine Transform that has a direct, 2-D architecture, eliminating the need for a transpose memory buffer. It outputs a transformed 4x4 macro-block for every clock cycle using parallel computation units. Multipliers are replaced by shifters resulting in a low power module. In Section II, we develop the mathematical equations used in design. The architecture and butterfly diagram of our proposed 2-D integer transform is given in Section III. We provide comparisons and discussions in Section IV and conclusions in Section V

II. MATHEMATICAL MODELLING OF INTEGER COSINE TRANSFORM

The equation for two dimensional Discrete Cosine transform of time domain signal f(x,y) for MxN points is given by

$$F(m,n)=\frac{2}{\sqrt{MN}}C(m)C(n)\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}f(x,y)Cos\left(\frac{(2x+1)m\Pi}{2M}\right)Cos\left(\frac{(2y+1)n\Pi}{2N}\right) \quad (1)$$

With C(m),C(n) = $\frac{1}{\sqrt{2}}$ for m,n=0 and C(m),C(n) =1 otherwise

2D DCT for 4x4 points is obtained from equation (1) as

$$2D\text{- DCT } [x] = A.X.A^t$$

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$$A=\begin{bmatrix} a & a & a & a \\ b & c & -c & -b \\ a & -a & -a & a \\ c & -b & b & -c \end{bmatrix}$$

With

$$a=\frac{1}{2}$$

$$b=\sqrt{\frac{1}{2}}\cos\left(\frac{\pi}{8}\right) =0.6532$$

$$c=\sqrt{\frac{1}{2}}\cos\left(\frac{3\pi}{8}\right) = 0.2706$$

This is used as a basic matrix to obtain the 2D- ICT of a 4x4 residue using the relation

$$ICT(X) = C.\ X.\ C^T \qquad (2)$$

The core transform matrix C is obtained by scaling the matrix A with a value of approximately 2.5 and rounding it to the nearest value, which results in

$$C=\begin{bmatrix} C1 & C1 & C1 & C1 \\ C2 & C1 & -C1 & -C2 \\ C1 & -C1 & -C1 & C1 \\ C1 & -C2 & C2 & -C1 \end{bmatrix}$$

Where C1= 1 and C2 =2.

Requirement of transpose buffer memory arises due to the presence of C^T term in equation (2). By avoiding C^T, we can eliminate the need for a transpose buffer memory. Equation (2) can be rewritten as

$$ICT\ (X) = (C.\ (C.\ x)^T)^T \qquad (3)$$

Thus the requirement of transpose buffer memory is eliminated.

Outputs Y(0) to Y(3) are related to inputs X(0) to X(3) as shown

Iteration 1:

A(0) =X(0)+X(3)

A(1) = X(1)+X(2)
A(2) = X(1)-X(2)
A(3) = X(0)-X(3)

Iteration 2:

Y(0) = A(0)+A(1)
Y(1) = A(2) + (A(3)<<1)
Y(2) = A(0)-A(1)
Y(3) = A(3) - (A(2)<<1)

Where A(0) to A(3) are intermediate results in the butterfly structure.

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III. ARCHITECTURE OF 1D CORE ICT MODULE AND 2D ICT MODULE

The butterfly structure of a 1-D ICT module is given in figure 4. From the core transform matrix C it is clear that only terms which are integral powers of 2 i.e. $\pm 2^i$ (i=0 or 1) exists. Hence all the multipliers can directly be replaced by shifters, greatly reducing the power requirement. Figure.5 illustrates the structure of the complete 2D ICT module without row column transpose buffer.. The first four and second four 1D transform units compute the transform value on alternate edges of the clock to output the 2D transformed value of the residual data.

The coding of the design has done using Verilog Hardware Descriptive Language and the Simulation of the proposed design was done using Incisive Unified Simulator (IUS)from Cadence EDA Tool .Figure.7 represents the input residue data to the 2D ICT module. The input matrix x[143:0] is subjected to 1D integer transform to obtain xy1[15:0] –xy15[11:0] as shown in figure.7 and figure.8. This is again transformed by the second set of 1D transform units to obtain the final 2D transformed data yy[14:0]-yy[14:0] as shown in the figure 9.

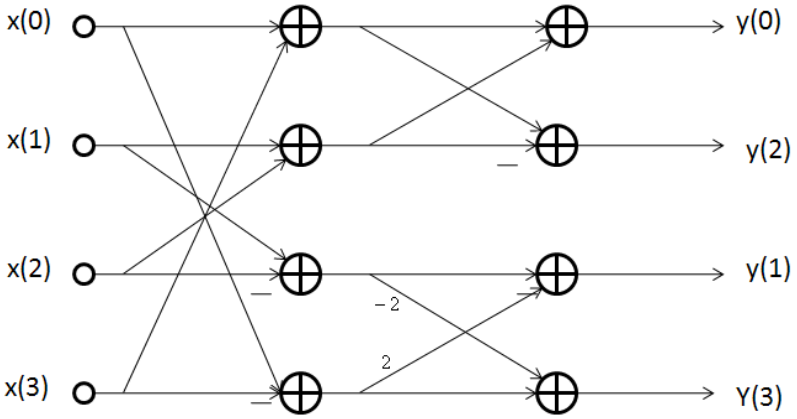

Figure 4. Structure of 1D core integer transform module

Figure.4 illustrate the butterfly diagram of 1D core Integer cosine transform. 1st pair of adders and subtractors are used to obtain A(0) to A(3). Shifters are then employed in place of multipliers. Second set of adders and subtractors are used to obtain the 1D transformed result Y(0) to Y(3).

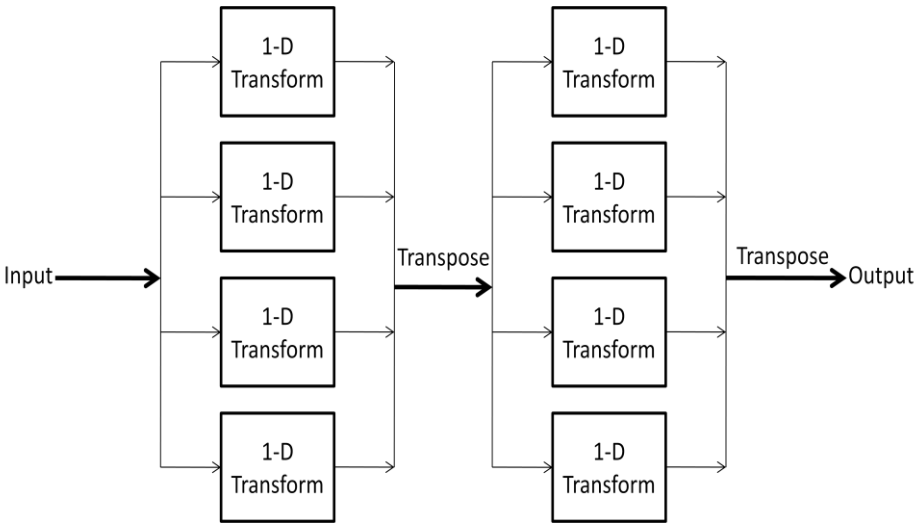

Figure 5. Structure of direct 2D transform without transpose buffer memory.

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The above figure 5 represents the block diagram of 2D ICT module. The first four and the second four D ICT modules work on alternate edges of the clock to produce the final result in a single clock cycle.

IV. RESULTS AND DISCUSSIONS

A 4x4 matrix of image data was simulated. Simulation results at each stage of computation are as discussed below.

a. Simulation results

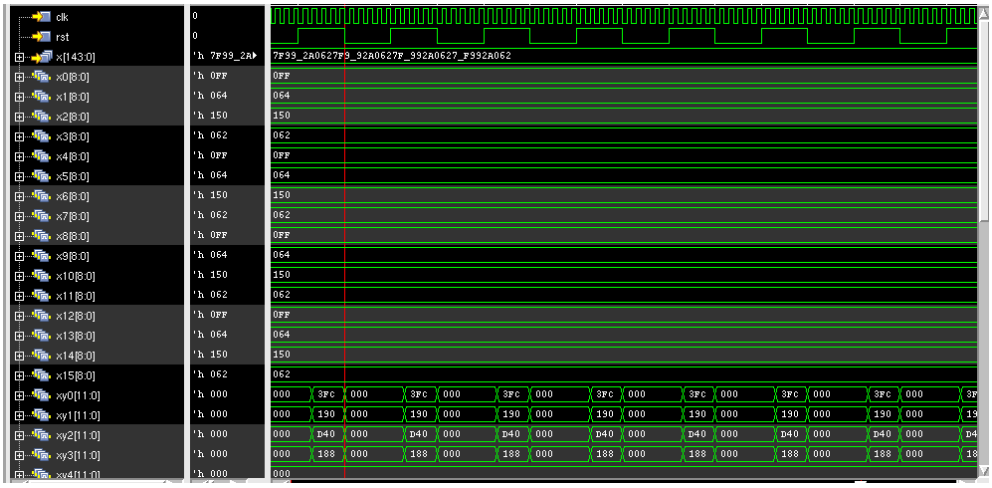

Figure 7 : Simulation result of input residue matrix and output of first 1D transform units.

The above figure 7 shows the input values for the sixteen residues. Each of the sixteen residues is of nine bit value. Most significant bit of each of the residue is represents the sign. This indicates by what value the pixel has be changed between successive frames. It is form of differential coding along with the predictor, and Huffman coding modules, enables H.264 to achieve higher compression ratio.

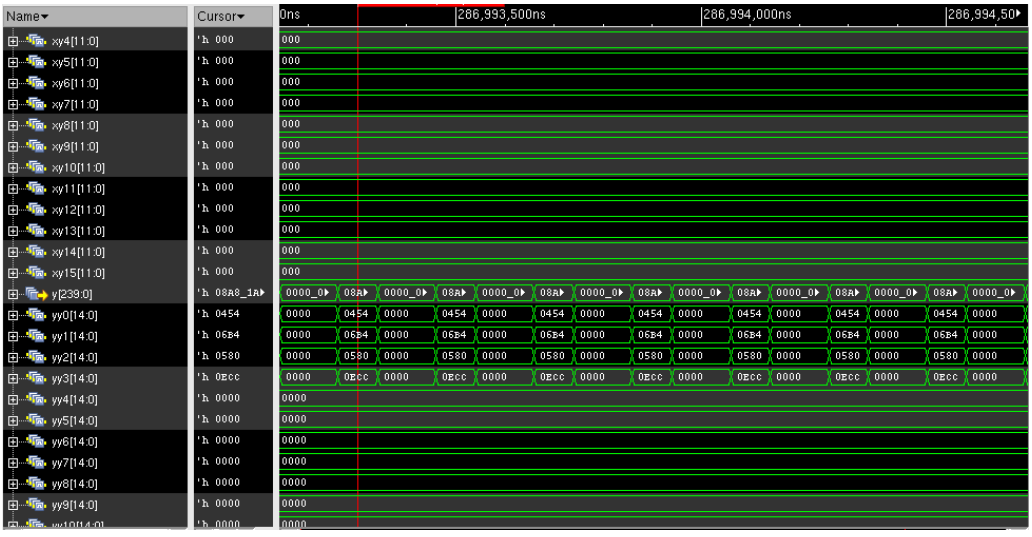

Figure 8: Simulation result of first 1D transform units and second 1D transform units.

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The above figure 8 represents the output of first of the two one dimensional ICT. This 4x4 matrix is transposed before it passes through the second of the two 1-dimension transform blocks. This transform is carried out by using wire logic, eliminating the use of any sequential circuits resulting in higher throughput and reduced power consumption.

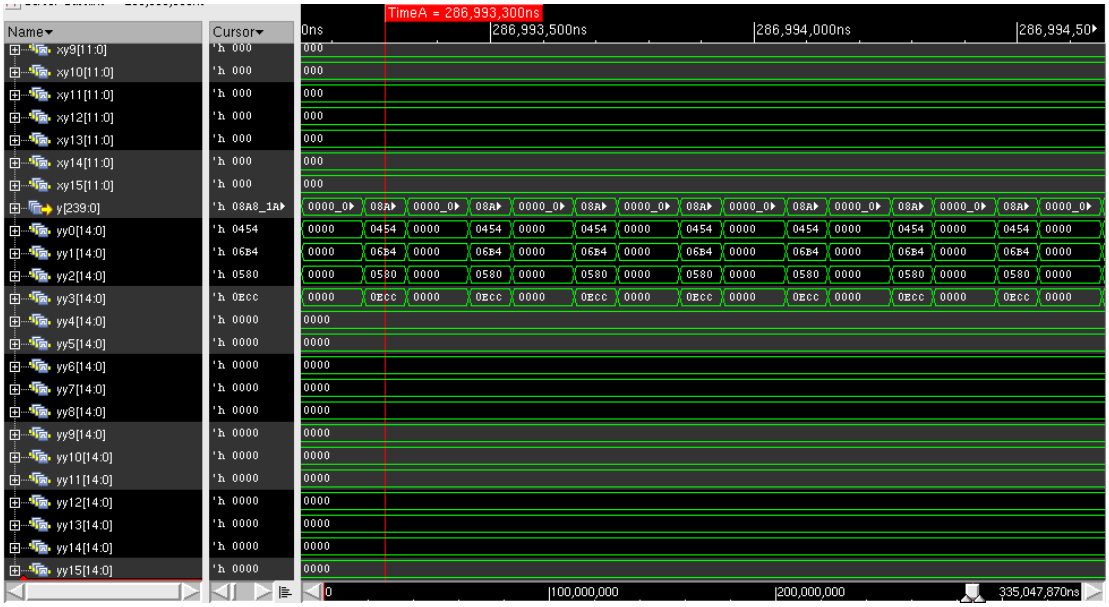

Figure 9: Simulation result final output of the 2D ICT module.

Final 2D ICT is obtained by subjecting the transposed 1D transform outputs through the second set of transform blocks.

b. Synthesis Results and comparison of Results

The proposed architecture was synthesised using 6 layer, 180 nano meter technology libraries and the obtained results are as follows.

Table 1. Synthesis results

Parameter	Value
Frequency	250M Hz
Total power	38.5 mw
Area	97816
Cell count	4048

Table 1 shows the synthesis results for 180 nm technology library. The synthesis was done at a frequency of 250M Hz. The total power consumed at this frequency was found to be 38.5 mW. A total of 4048 library cells were used to implement the system which occupied an area of 97816 $um^{2.}$

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Table 2. Comparison of obtained synthesis results with various other architectures.

	Proposed	[5]	[4]	[6]	[7]
Frequency(M Hz)	**250**	250	100	50	125
Power(mw)	**38.5**	54	24.2	39	--
Processing rate(Pixels/sec)	**16**	4	8	8	16/2
Gate count	**4.048K**	17.7K	6.5K	39.8K	18.5K
Throughput(Pixels/sec)	**4000M**	1000M	800M	400M	1000M

Table. 2 provides a comparison of the obtained synthesis results of the proposed architecture with results of standard architecture. A power of 38.5 mW was obtained against 54 mW as according to architecture proposed in [5] for the same frequency of 250M Hz. Hence a percentage of power saving is 33.5% . Finally it is observed that it is low power consumption. A through put of 4000M pixels/sec was obtained as compared to that of [7] which is 1000M pixels/sec. Hence proposed architecture four times as many pixels as [7] does in a given interval of time. . Total gate count of the proposed design is 4048 which is lesser than 6500 as according to [4] with a percentage difference of 46.49%.

V. CONCLUSION

In this proposed paper a low power high speed architecture for 2D Integer cosine transform was designed. The computation speed was increased by eliminating the row column transpose buffer, The power reduction was obtained by employing shifters and eliminating the need for transpose memory. For a frequency of 250M Hz, 38.5 mW of power was consumed with a percentage difference of 33.5% compared to [5]. The through put is 4000 M pixels/sec which is 300% more than that of [5]. In conclusion the proposed design is suitable for low power high speed applications.

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