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Design a Radix 8-Booth Multiplier with Pre-Encoded Mechanism

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ABSTRACT: The radix-8 Booth algorithm is widely used to improve the performance of multiplier because it can reduce the number of partial products by half. However, numerous additional encoders and decoders would cause the power consumption of the Booth multiplier to be considerable. In this paper, a new radix-8 Booth pre-encoded mechanism is proposed to reduce the power consumption of the Booth multiplier. The proposed design can effectively reduce the power of the Booth multiplier dissipated in the redundant activities by disabling the Booth encoders and decoders from unnecessary working. Particularly, since the control signals are generated early at the pipeline input register before the multiplier, the performance of our design is better than the traditional Booth multiplier. Based on the TSMC 40 nm technology, the simulation results show that the proposed pre-encoded mechanism can reduce the dynamic and static power by 45% and 65%, respectively, compared to the traditional 16-bit radix-4 Booth multiplier. Compared to the previous designs, the proposed design keeps the feature of race-free and has lower power consumption. Even compared to the approximate design, the proposed design has better power efficiency and can provide the exact products.

KEYWORDS: Booth algorithm; Manets; FPGA ;ALU; Multification; TSMC

I. INTRODUCTION

Digital multipliers are major source power dissipation in Digital Signal Processors. High power dissipation in these structures is mainly due to the switching of a large number of gates during multiplication. In addition, much power is also dissipated due to a large number of spurious transitions on internal nodes. Timing analysis of a Full Adder, which is a basic building block in multipliers, has resulted in a different array connection pattern that reduces power dissipation due to the spurious transition activity. Furthermore, this connection pattern also improves the multiplier throughput. A variety of measures can be used to evaluate the efficiency of the processors. So both the area occupied by the circuit and the time required for the performance of computation must be taken into consideration. Therefore depending on the speed and area requirements, the digital multipliers used can be either of bit-serial or a bit-parallel based architecture. The bit-serial approach processes the data serially where at every clock cycle a single data bit is fed to the processor to be processed. In contrast, the parallel approach processes the data bits in a parallel fashion in just one clock cycle. The initial architectures were implemented using bit-serial based structures due to their design simplicity and low hardware requirements, which lead to cheap system costs. But for systems that require high speeds, bit-parallel approach is used. But this approach requires large silicon area, communication overhead, and pin out. So a trade off must be made between these two approaches depending on the application.

The multiplication process may be viewed to consist of the following two steps:

1) Evaluation of partial products

2) Accumulation of the shifted partial products.

The product of two n-digit numbers can be accommodated in '2n' digits. In the binary system, an AND gate can be used to generate partial product Xi Yj.

II. RELATED WORK

A primary objective of this project was to develop a synthesizable model for the booth algorithm. Synthesis is the process of converting the register transfer level (RTL) representation of a design into an optimized gate-level netlist. This is a major step in ASIC design flow that takes an RTL model closer to a low-level hardware implementation.

Synthesis consists of three main steps. The first step is the "Translation", which involves converting the RTL description of a design into a non-optimized intermediate representation that is used by the synthesis tool. The second step is the "logic optimization", which optimizes the internal representation by removing redundant logic and performing Boolean logic optimizations. The third step is called "technology mapping & optimization" which maps

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the internal representation to an optimized gate level representation using the technology library cells based on design constraints

III. PROPOSED ALGORITHM

The first step in the synthesis process is to read all the components in the design hierarchy. There are three components in the 3-level design hierarchy that needs to be synthesized. Since the RTL model utilizes a Verilog "Package", then the synthesis tool needs to enable the semantics of a package. In addition, the synthesis tool needs to know if there are multiple instances of calling an automatic function in the design, to preserve separate values for each instance.

After reading the design files, they are "Analyzed" and "Elaborated" through which the RTL code is converted into the Synopsys Design Compiler(SDC) internal format. [6] The intermediate results are stored in the defined "working library".

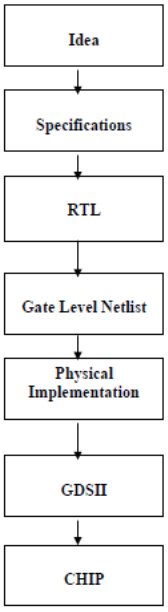
After this step, a 40MHz clock signal is applied to the clock port of the root module, and the synthesis tool is programmed not to modify the clock tree during the optimization phase. In addition, an arbitrary input delay of 5ns with respect to the clock port is applied to all input and output ports (except the clock port itself) to set a safe margin by considering any unintended source of delay such as the delay associated with driving module/modules.

Then, the design is constrained with hypothetical maximum area equal to zero to force the tool to make the gate level netlist as compact as possible.

In the next steps, the tool is programmed to consider a unique design for each cell instance by removing the multiply-instantiated hierarchy in the current design. Then, the synthesis script removes the boundaries from all the components in the design hierarchy and removes all levels of hierarchy.

Finally, the tool compiles the design with high effort and reports any warning related the mapping and final optimization step. At the end, the tool generates reports for the optimized gate level netlist area, the worst combinational path timing, and any violated design constraint.

IV. ALGORITHM CHART



V. SIMULATION RESULTS

The synthesis area report shows the total number of cells and nets in the netlist. It also uses the area parameter associated with each cell in the LSI_10K library file, to calculate the total combinational and sequential area of the netlist. The total area of the gate level netlist is unknown since it depends on total area of the interconnects, which

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itself is a function of the wiring load model used in physical design. The total cell area in the netlist is reported as 22978 units, which is the sum of combinational and sequential areas.

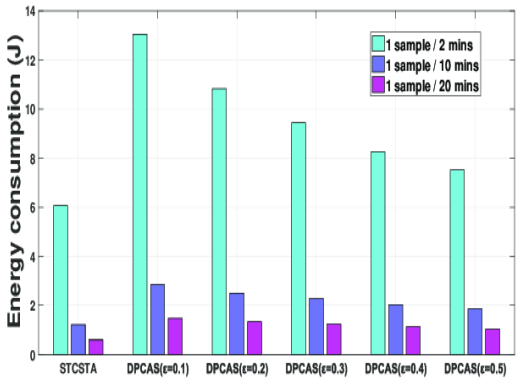

Fig.1.Energy consumption by each node

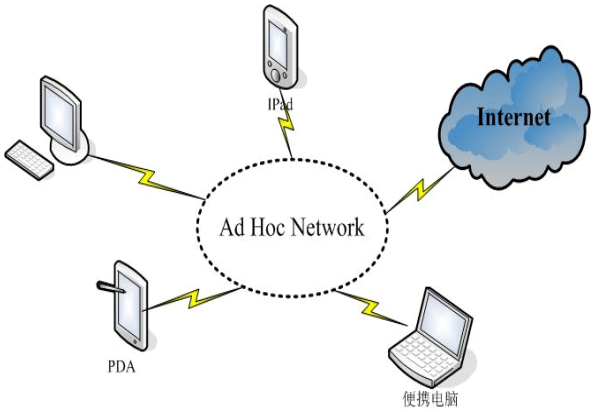

Fig 2. Ad Hoc Network of 5 Nodes

VI. CONCLUSION AND FUTURE WORK

The simulation results showed that the proposed algorithm performs better with the total transmission energy metric than the maximum number of hops metric. The proposed algorithm provides energy efficient path for data transmission and maximizes the lifetime of entire network.As the performance of the proposed algorithm is analyzed between two metrics in future with some modifications in design considerations the performance of the proposed algorithm can be compared with other energy efficient algorithm. We have used very small network of 5 nodes, as number of nodes increases the complexity will increase. We can increase the number of nodes and analyze the performance.

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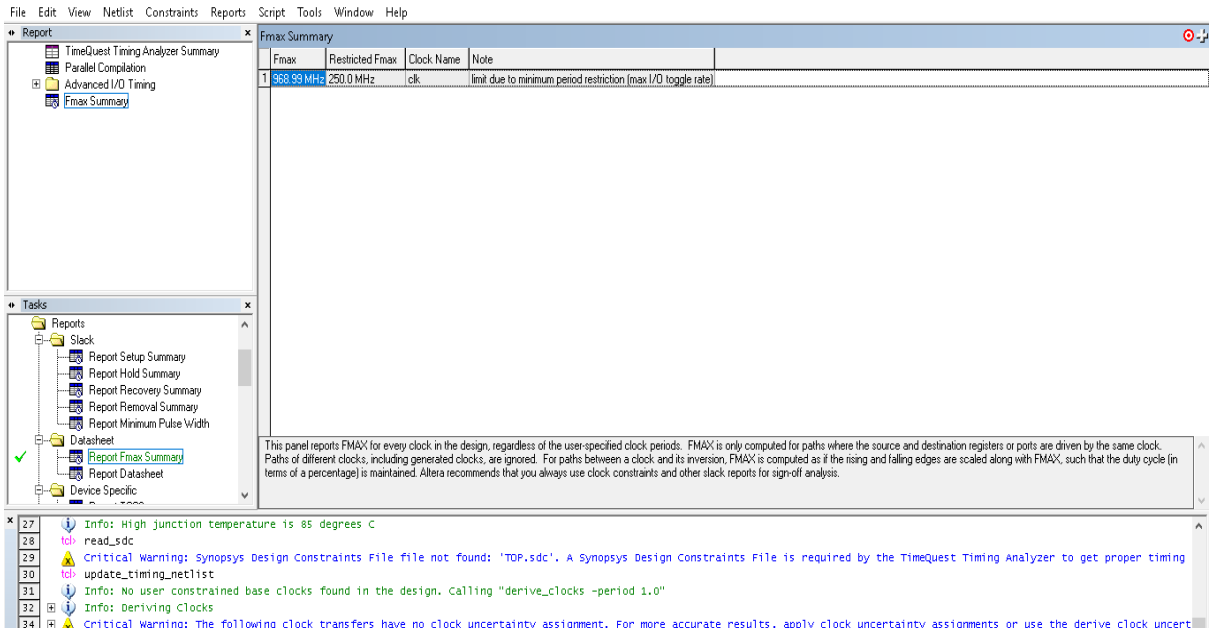
Flow Summary

Flow Status	Successful - Tue Mar 05 05:16:56 2019
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	TOP
Top-level Entity Name	booth_radix8_algorithm
Family	Cyclone III
Device	EP3C16F484C6
Timing Models	Final
Met timing requirements	N/A
Total logic elements	208 / 15,408 (1 %)
Total combinational functions	208 / 15,408 (1 %)
Dedicated logic registers	32 / 15,408 (< 1 %)
Total registers	32
Total pins	35 / 347 (10 %)
Total virtual pins	0
Total memory bits	0 / 516,096 (0 %)
Embedded Multiplier 9-bit elements	0 / 112 (0 %)
Total PLLs	0 / 4 (0 %)



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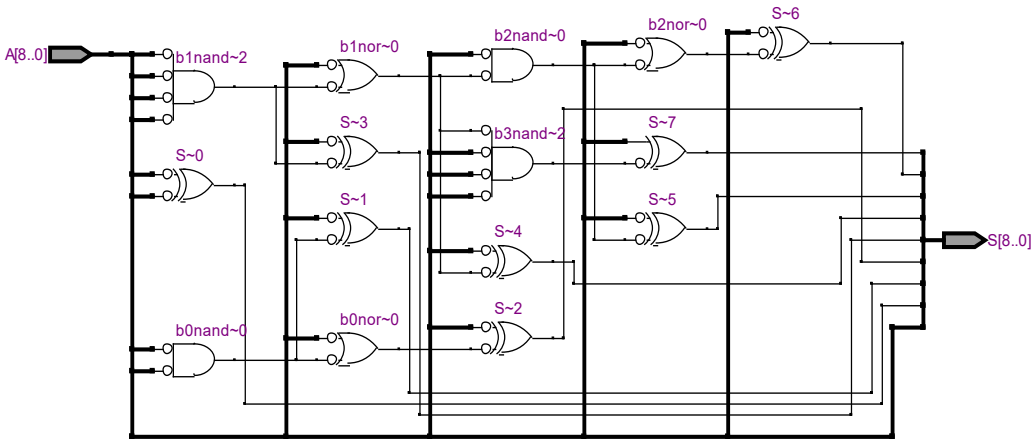

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REFERENCES

1. Jiang, H., Han, J., Qiao, F., et al.: 'Approximate radix-8 booth multipliers for low-power and high-performance operation', Trans. Comput., 2018, 65, (8), pp. 2638–2644, doi: 10.1109/ TC.2015.2493547
2. Xue, H., and Ren, S.: 'Low power-delay-product dynamic CMOS circuit design techniques', Electron. Lett., 2017, 53, (5), pp. 302–304, doi: 10.1049/el.2016.4173
3. Chattopadhyay, T., and Gayen, D.: 'All-optical 2's complement number conversion scheme without binary addition', Optoelectronics, 2017, 11, (1), pp. 1–7, doi: 10.1049/iet-opt.2015.0087
4. Qian, L., Wang, C., Liu, W., et al.: 'Design and evaluation of an approximate wallace-booth multiplier'. IEEE Int. Symp. Circuits and Systems (ISCAS), Montreal, QC, Canada, May 2019, pp. 1974–1977
5. Chuang, P., Sachdev, M., and Gaudet, V.: 'A 167-ps 2.34-mW singlecycle 64-bit binary tree comparator with constant-delay logic in 65-nm CMOS', Trans. Circuits Syst., 2019, 61, (1), pp. 160–171, doi: 10.1109/TCSI.2013.2268591
6. B. Bross, W.-J. Han, J.-R. Ohm, G. J. Sullivan, Y.-K. Wang, and T. Wiegand, High Efficiency Video Coding (HEVC) Text Specification Draft 10, document Rec. JCTVC-L1003, 2013.
7. L.-M. Po and W.-C. Ma, "A novel four-step search algorithm for fast block motion estimation," IEEE Trans. Circuits Syst. Video Technol., vol. 6, no. 3, pp. 313–317, Jun. 2017.
8. JVT of ISO/IEC MPEG, ITU-T VCEG, MVC Software Reference Manual-JMVC 8.2, document Rec. JVT-B118r2, May 2010.
9. J.-C. Tuan, T.-S. Chang, and C.-W. Jen, "On the data reuse and memory bandwidth analysis for full-search block-matching VLSI architecture," IEEE Trans. Circuits Syst. Video Technol., vol. 12, no. 1, pp. 61–72, Jan. 2002. T. Y. Lee, "A new frame-recompression algorithm and its hardware design for MPEG-2 video decoders," IEEE Trans. Circuits Syst. Video Technol., vol. 13, no. 6, pp. 529–534, Jun. 2003.
10. R. Dugad and N. Ahuja, "A fast scheme for image size change in the compressed domain," IEEE Trans. Circuits Syst. Video Technol., vol. 11, no. 4, pp. 461–474, Apr. 2001.
11. Y. Lee, C.-E. Rhee, and H.-J. Lee, "A new frame recompression algorithm integrated with H.264 video compression," in Proc. IEEE Int. Symp. Circuits Syst., ISCAS, May 2007, pp. 1621–1624.
12. X. Bao, D. Zhou, and S. Goto, "A lossless frame recompression scheme for reducing DRAM power in video encoding," in Proc. IEEE Int. Symp. Circuits Syst., ISCAS, May/Jun. 2010, pp. 677–680.
13. Subramanian P, A Sagar Chaitanya Reddy "VLSI Implementation of Fully Pipelined Multiplierless 2D DCT/IDCT Architecture for JPEG"
14. G. A. RUIZ, J. A. MICHELL AND A. BURO´ N "High Throughput Parallel- Pipeline 2-D DCT/IDCT Processor Chip" Journal of VLSI Signal Processing 45, 161–175, 2006
15. JarmoTakala, JariNikara, David Akopian, Jaakko Astola', and Jukka Saarinen' "PIPELINE ARCHITECTURE FOR 8 x 8 DISCRETE COSINE TRANSFORM" 0-7803-6293-4/00/$10.00 *0* 2000IEEE.
16. J. A. Michell, G. A. Ruiz, A. M. Burón " PARALLEL-PIPELINED
17. ARCHITECTURE FOR 2-D ICT VLSI IMPLEMENTATION" 0-7803-7750- 8/03/$17.00 ©2003 IEEE.

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