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Design of Quantum Dot Cellular Automata (QCA) Based T Flip-Flop using QCA Designer

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ABSTRACT: Downscaling of current CMOS devices after a certain limit is not feasible. It introduces an abnormal quantum behaviour in nanoscale range. Several emerging technologies such as single-electron transistors, quantum-dot cellular automata,silicon nanowires,carbon nanotubes emerge as a possible replacement of current CMOS. Quantum-dot cellular automata (QCA) is one of them, and it promises high circuit density, faster speed, low power consumption over the CMOS technology. The 3-input majority voter is the primarypart of QCA circuits. The 3-input majority voter is functionally imperfect without an inverter logic to synthesize all types of Boolean functions. In this work, we propose the design of T Flip-Flop circuit using QCA technology with majority voter as a base.

KEYWORDS: CMOS Technology, QCA Technology, 3-Input Majority voter, Edge Triggered Clock,T-Flip-Flop

I. INTRODUCTION

Quantum-dot cellular automata (QCA) is one of the new nanoelectronics that has emerged in the last decade. QCA technology wasintroduced by Lent et al. in 1993 [1]. QCA is being used as a new technique for computation. QCA is a good choice for replacement of CMOS technology due to many advantages such as itshigh speed, small size, and low power consumption. It hangs on electron configurations instead of voltage levels as in CMOS. The main issue in QCA is complexity reduction. Many papers have been introduced designing digital circuits using QCA technology. Most of these papers were searching for an optimal circuit form. Researchers have been paying attention to the design of the memory cell as one of the important circuits in QCA technology [2–7], and a well-optimized flip-flop structure [8–10], in addition to counters [9–11]. This paper introduced an optimal Edge Triggered T flip-flop structure with a smaller number ofcells count and used it to design N-bit counter circuits. The presented flip-flop was used to implement many counter circuits.

The rest of this work is as follows: Section II focuses on the QCA fundamentals, Section III on Basic QCA Designs, Section IV on the proposed design, Section V provides the simulation results,and finally, the conclusion of this paper is presented in Section VI.

II. QCA BASICS

A quantum cell is a brick unit in QCA. Each squareshaped cell consists of four dots arranged regularly inside the cell. Each cell contains two electrons that can tunnel between the dots but electrons cannot escape out of the cell. Due to electron repulsion forces, the electrons to occupy the dots diagonally. Theelectrons inside the cell can represent the digital binary numbers: where the cell polarization (P) equals +1, it is represented as binary logic 1; while when polarization (P) equals −1, it is represented as binary logic 0. Fig. 1 shows the state of the cell at different polarizations.

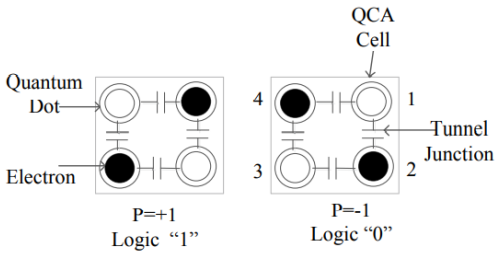

Fig. 1.Two states of polarization in a basic QCA cell, binary zero and one.

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The main building blocks in QCA are the 3-input majority gate (Maj-3), as illustrated in Fig. 2, and the inverter shown in Fig. 3. Any Boolean function can be implemented or represented by using these gates. The AND gate can be formed using the majority gate by connecting one of its inputs to fixed polarization -1 or logic 0. If any inputs of the majority gate connect to fixed polarization +1 or logic 1, the OR gate will be obtained. The logical function of the majority gate is illustrated in Equation 1.

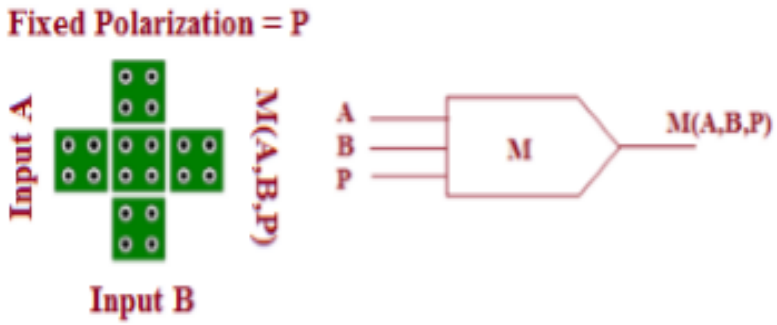

Fig. 2. Majority gate.

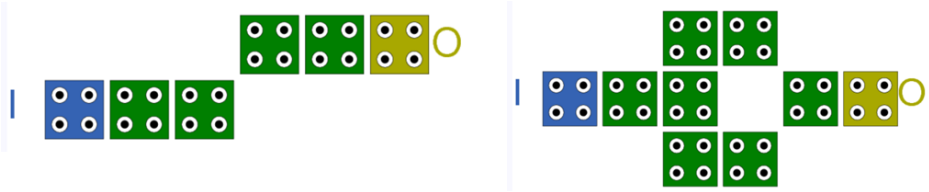

Fig. 3.Quantumdot cellular automata (QCA) inverter forms.

$$M(P, A, B) = PA + PB + AB \quad \ldots \quad (1)$$

The multi-input majority was considered by researchers [12–16], and its reliability was studied in [17].

The clock is a vital issue in QCA for the following reasons: The clock signal gives the circuit the power to make the synchronizationand it controls thedata flowdirection. Clocking is the major source of power to stimulate the QCA circuit. QCA circuits use four clocking signals to achieve the inherent pipelining, with each signal having four phases, as illustrated in Fig. 4. The clock phases provide adiabatic switching instead of abrupt switching for the cells, thereby making the circuit closer to the ground state [18,19].

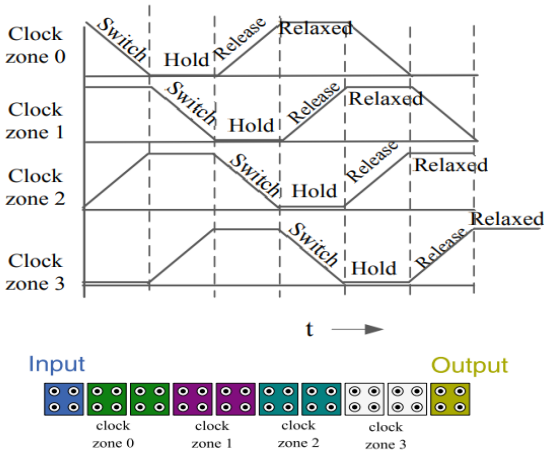

Fig. 4.QCA clock signals.

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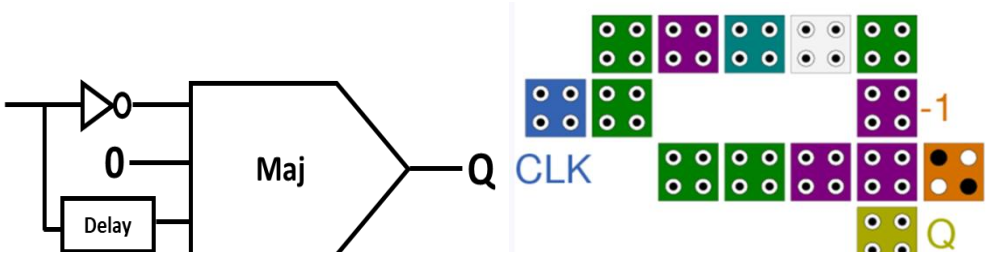
III. BASIC QCA DESIGNS

Edge triggered clock Design

In electronics, a signal edge is a transition of a digital signal from low to high or from high to low.
A **rising edge** or **positive edge** is the lowtohigh transition.
A **falling edge** or **negative edge**is the hightolow transition.

Falling Edge triggered clock Design

In this, clock is Active when the input signal is transitioning from a high state (logic '1') to a low state (logic '0').
In QCA Designer the Falling Edge triggered clock is design using AND gate (Majority gate with one input is fixed polarization '-1'). The fig. 6(a) shows schematic diagram of Falling Edge triggered clock and fig. 6(b) shows QCA layout of Falling Edge triggered clock. One input to the AND gate is clock with delay and other input is inversion of clock without delay. The output of the AND gate (Q) is Falling Edge triggered clock.

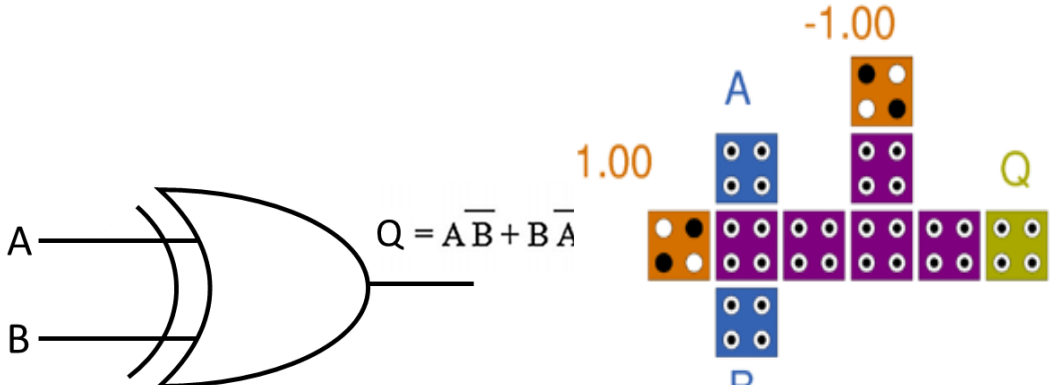


(a) (b)

Fig. 6. Falling Edge triggered clock: (a) Schematic diagram, (b) QCA layout

XOR Gate Design

XOR gate is important logic in the digital circuits. This is widely used in the comparators,adders,multipliers, multiplexer circuit, etc. The XOR digital logic symbol is shown in fig. 7(a) and the QCA layout is presented in fig. 7(b). It does not follow any Boolean function, but take advantage of the inherent characteristics of QCA cells to form XOR gate.The XOR design shown in fig. 7(b) is area efficient and optimized in comparison with the earlier XOR in QCA.This XOR structure needs only 1 clock zone. The structure of the XOR gate in the fig. 7(b) was introduced by [20].



(a) (b)

Fig. 7. XOR gate: (a) Symbol, (b) QCA layout

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IV. T FLIP-FLOP DESIGN

T flip-flop Design

In electronics, a flip-flop is a circuit that has two stable states and can be used to store state information. Flip-flops are used as data save elements. A flip-flop is a device which stores a single bitof data: one of its two states represents a "zero" and the other represents a "one".

T flip-flop is widely used in frequency divider circuits, binary addition, and digital counters.

A characteristic table of a flip-flop explains the logical properties, by expressing its operation in tabular form. The characteristic table of T flip-flop is presented in Table 1. They define the next stateas a function of the inputs and the present state. Q(n) refers to the present state.Q(n+1) is the next state one clock period later.Q(n) denotes the state of the flip-flop immediately before the clock edge, and Q(n+1) denotes the state that results from the clock transition.

The characteristic table of the T flip-flop has only two conditions: When T = 0, the clock edge does not change the present state; when T = 1, the clock edge inverts(complements) the presentstate of flip-flop.

Table 1: T flip-flop Characteristic table

CLK	T	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

The logical properties of a flip-flop, as described in the excitation table, can be expressed algebraically with a characteristic equation. For the T flip-flop the characteristic equation is shown in Equation 2

$$Qn+1 = CLK'.Qn + T'.Qn + CLK.T.Q'n$$
Or
$$Qn+1 = (Qn) \text{ XOR } (CLK.T)$$

The schematic diagram of T flip-flop is illustrated in Figure 3.6, while the QCA layout is shown in Figure 3.7. It is clear from the presented diagram that the T flip-flop was accomplished by using the Falling Edge triggered clock and XOR gate with the AND gate. The data storage was accomplished using a loop-based mechanism.

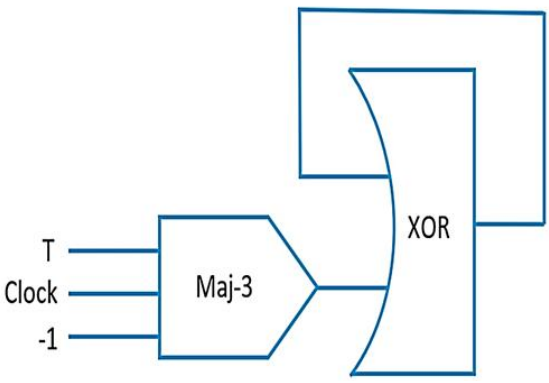

Fig. 8. Schematic diagram of T flip-flop

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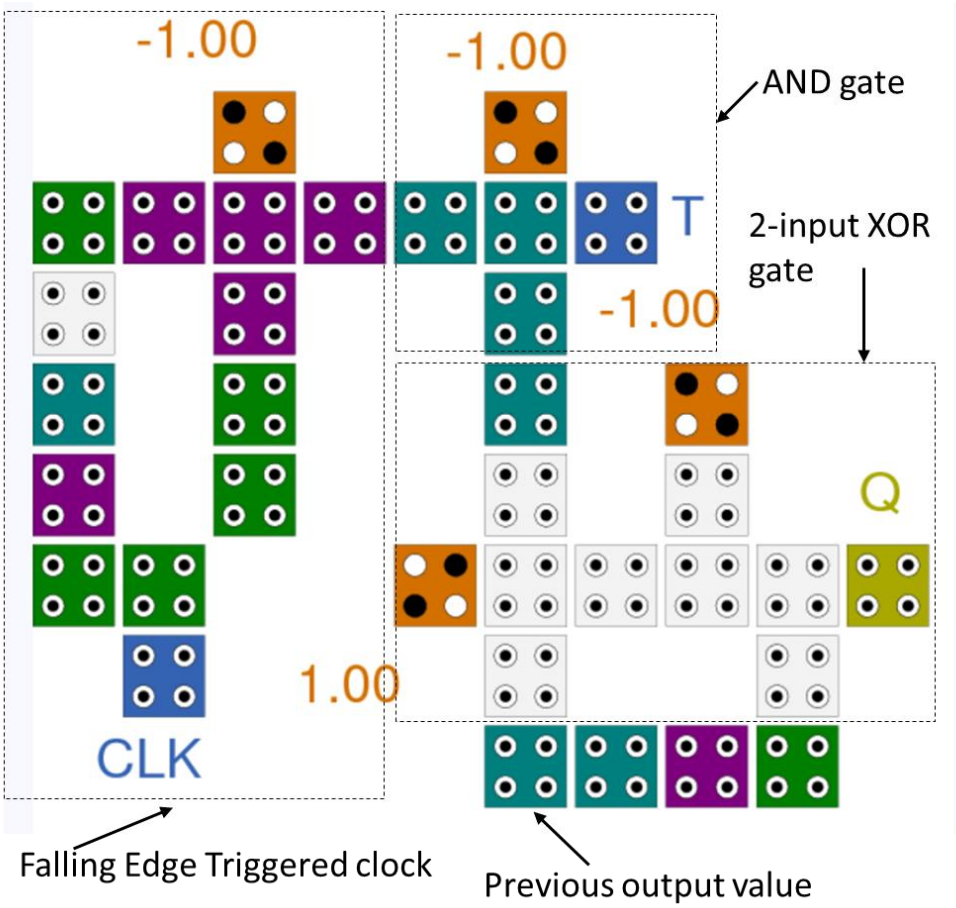

Fig. 9. Falling Edge triggered T flip-flop QCA layout

V. SIMULATION RESULTS

The Simulation Results of Falling Edge triggered T flip-flop is shown in fig. 10. We know T flip-flop has only two conditions: When T = 0, the clock edge does not change the presentstate; when T = 1, the clock edge complements the presentstate of the flip-flop.

Form fig. 10 we can observe

- If previous output = "1" and clock = 1, T = 0 then the new output will be same previous output.
- If previous output = "1" and clock = 1, T = 1 then the new output will be invert to "0".
- If previous output = "0" and clock = 1, T = 1 then the new output will be invert to "1".

In QCA there is delay between clock zones. Due to this delay the output of T flip-flop is not in synchronous with the input, there some delay between input and output.

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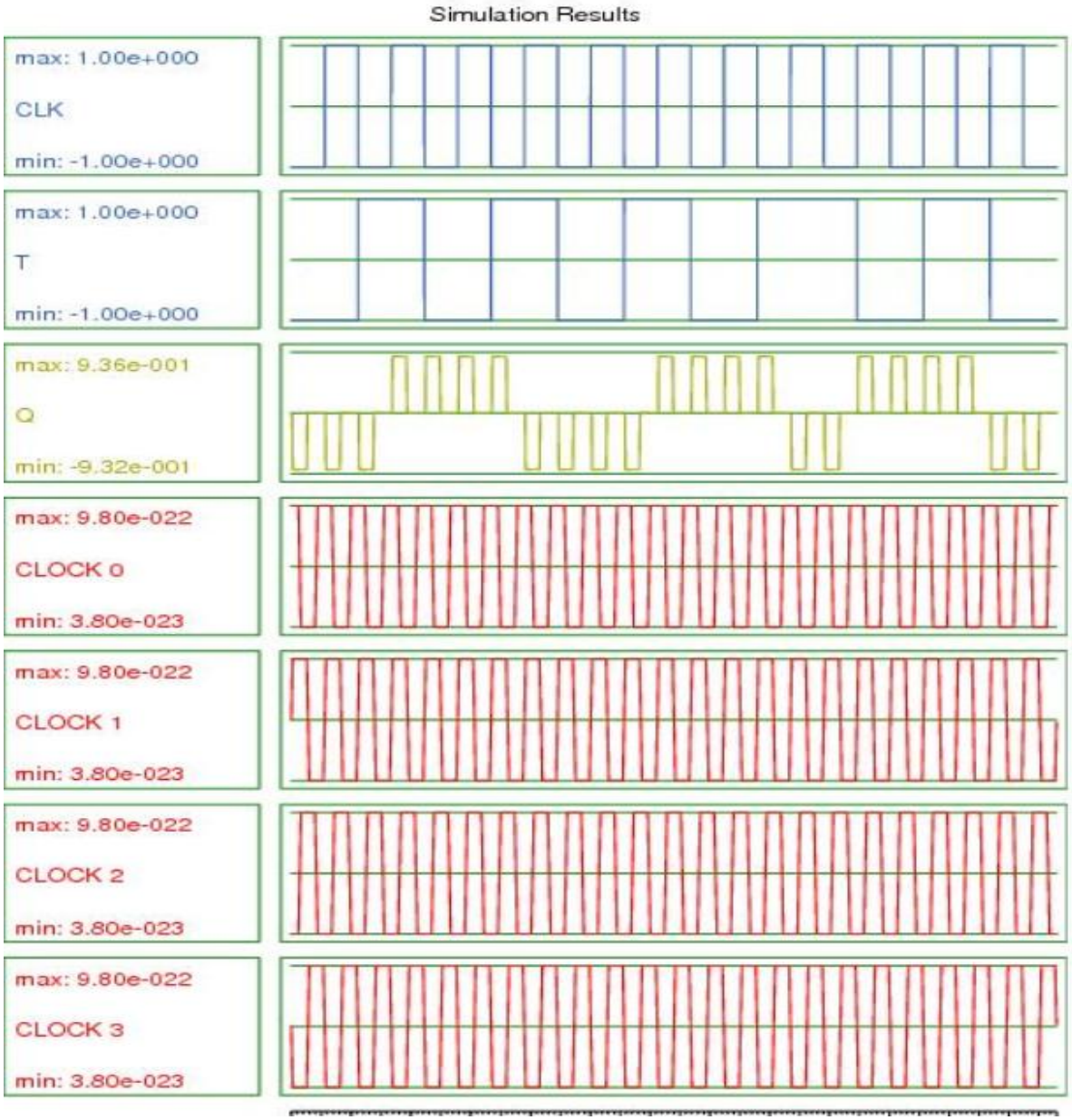

Fig. 10. Simulation Results of Falling Edge triggered T flip-flop

VI. CONCLUSION AND FUTURE WORK

This paper introduced an optimal form of the T flip-flop. The presented flip-flop was Falling Edge triggered and was implemented with a noticeable area of 0.03 μm2 and at minimum complexity with only 35 cells. The verification of the proposed circuits was performed using the QCA Designer software. The unique proposed design of the flip-flop can utilize to implement synchronous counters with different sizes, binary addition, and frequency divider circuits.

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