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# High Speed and Area Efficient Scalable N-Bit Digital Comparator

**Logadevi.G, Pallavi.G, Maheswari.I, Nikhilkumar.N, Nagapravallika.P, Kumaraswamy.G**

Professor, Department of Electronics & Communication Engineering, Siddharth Institute of Engineering & Technology, Puttur, India

Department of Electronics & Communication Engineering, Siddharth Institute of Engineering & Technology, Puttur, India

**ABSTRACT**: An area-efficient *N*-bit digital comparator with high operating speed and low-power dissipation is presented in this work. The proposed comparator structure consists of two separate modules. The first module is the comparison evaluation module (CEM) and the second module is the final module (FM). Independent from the input operand bitwidths, stages present in CEM involve the regular structure of repeated logic cells used for implementing parallel prefix tree structure. The FM validates the final comparison based on results obtained from the CEM. The presence of regular very large-scale integration topology in the proposed structure allows the analytical derivation of the area in terms of total number of transistors present in the design and total delay encountered in input–output flow as the function of input operand bitwidth. Spectre simulation results have been presented using 0.18 µm complementary metal–oxide–semiconductor (CMOS) technology at 1 GHz. The main advantages of the proposed comparator are minimum input–output delay of 0.57 ns, minimum fan-out-of-4 delay of 9.5 ns and low-power dissipation of 1.03 mw as compared with existing comparators designed using 180 nm CMOS technology for 64 bit comparison.

KEYWORDS: Digital comparator; Area-efficient; Comparision operation; Bitwidths; EXOR-EXNOR logic gates; Low power consumption

## I. INTRODUCTION

Digital comparator is the fundamental design element used for the applications, in which the final results are based on the output obtained from the computation involving comparison as an activity. There are wide range of applications, which involve scientific computations (digital image processing, pattern recognition/ matching, arithmetic sorting, data compression and digital neural network) and test circuit applications (built-in self-test circuits, signature analysers and jitter measurement consisting of comparator as the basic design element. The optimized design of comparator is used as the key component in the general-purpose computer architecture for developing the memory addressing logic, queue buffers, test circuits etc. Extensive use of comparator logic in various computation-based designs necessitates optimization in terms of area, power and speed. Some of the comparator designs use dynamic logic to achieve low-power consumption but limitations of low-speed and poor-noise margin make the dynamic design rather challenging. Digital comparator is the fundamental design element used for the applications, in which the final results are based on the output obtained from the computation involving comparison as an activity. There are wide range of applications, which involve scientific computations (digital image processing, pattern recognition/ matching, arithmetic sorting, data compression and digital neural network [1–3]) and test circuit applications (built-in self-test circuits, signature analysers and jitter measurement [4–5]) consisting of comparator as the basic design element.

The optimised design of comparator is used as the key component in the general-purpose computer architecture for developing the memory addressing logic, queue buffers, test circuits etc. [6–8]. Extensive use of comparator logic in various computation-based designs necessitates optimisation in terms of area, power and speed. Some of the comparator designs use dynamic logic to achieve low-power consumption but limitations of low-speed and poor-noise margin make the dynamic design rather challenging. The other designs use subtractors in the form of flat adder components along with custom logic circuits [9–13] to implement comparison process for wider bit operands but these designs give slower response and area intensive arrangement [14– 16]. The improvement in the scalability and reduction in the comparison delay has been achieved in hierarchical prefix tree structure-based comparator that composed of 2bit comparators at each level [17]. However, for the wide input operands, these structures maybe prohibitive due to prolonged delay and power consumption arising from $\log_2 N$ comparison levels. Improvement in some of the limiting factors of the parallel prefix tree structure such as area and power consumption can be achieved by

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using two input multiplexers at each level and generate–propagate logic at the first level [18]. However, the comparator structure has very high- power consumption since every cell remains in active state irrespective of the applied operand values.

## II. RELATED WORK

However, heavy- loaded clock signal further imposes limitations on the clock speed and jitter margin, which makes the design unsuitable for wide- range comparison. The comparator for large operand bitwidths is reported in [24], which comprises of two comparator stages. The first stage performs the 8bit comparisons, then subsequently results from the first stage transferred to the priority encoder and 8- to-1 multiplexer present in the second stage for the selection of the appropriate result obtained from the first stage. The two-phase domino clocking [25, 26] is utilised in the comparator so that two- stage operations could be performed in the single clock cycle for facilitating the operations to be synchronised with the rising and falling edges of the clock signal. This further limits jitter margin and operating speed, and therefore, the comparator becomes sensitive to the race conditions [27]. Another comparator structure proposed in [28] for enhancing operating speed using a combination of two-phase domino clocking structure and tree structure. In the structure, the carry-out signal is used as the indicator for 'greater-than' or 'less-than' outputs. However, the heavy loading of the clock signal present in the circuit remains the bottleneck of the design, and therefore, large drivers are required for the clock signal. Some of the comparator structures improved power efficiency through the removal of dynamically redundant computations using ripple-based structures [29–31].Similarly, most of the structures include compute-on-demand comparators that focus on the reduction of switching activities for achieving energy-efficient design [32–34]. However, these structures experience a prolonged delay in the worst-case scenario when the wide operands are considered for the comparison. To reduce the delay and power consumption due to the addition of ripple-based computations in the design, a comparison scheme based on bitwise competition logic has been proposed [35]. The pre-encoder structure in this approach limits the operating frequency and increases power consumption.

A parallel binary comparator reported in [36] uses regular digital hardware structure independent of input bitwidths but its area and power dissipation are high. To eliminate the limitations of the previous comparator structures, some designs are proposed, which leverage the two-level approach for comparison [37].

## III. PROPOSED ALGORITHM

The working principle of conventional comparison is , where the operands $A$ and $B$ have unequal most significant bit (MSB) bits. Since the first unequal bits of operands $A$ and $B$ encountered is well-sufficient to decide the outcome of the comparison between the two operands, remaining bit positions are ignored for comparison.

The comparison process used for comparing $N$-bit operands starts comparison from ($N$–1)th bit (or MSB bit) and proceeds toward the comparison of ($N$–2)th bit (or least significant bit (LSB)) if and only if the MSB bits of the two operands are equal.

The comparison process continues to compare the bit pairs obtained from the operands until it gets an unequal pair of bits on its way toward the LSB bit position. The unequal bit pair ($X$) and equal bit pair ($E$) are realised as

$$X = A \oplus B \quad (1)$$

$$E = A \odot B \quad (2)$$

The two $N$-bit input operands A and B are selected for the comparison and are checked if the operands are equal or not equal by performing the bitwise comparison. If the result of comparison comes out as 'equal', then the proposed comparator drives the output logic AEB to logic 1. If the comparison result of the operands comes out as 'unequal', then the pre-encoder output bits are checked from MSB to LSB. The output logic AGB or ALB goes to logic 1 based on the results of pre- encoder. The proposed algorithm reduces the superfluous switching activities occurred during comparison operation, which further limits the dynamic power consumption of the proposed comparator. The proposed $N$-bit digital comparator is shown in Fig. 4. For performing a comparison between two $N$-bit binary operands, the proposed structure is divided into the comparison evaluation module (CEM) and final module (FM). These modules serve as a high-level and low-level architectures. The CEM incorporates parallel prefix tree structure that is intended for performing a bitwise comparison of two $N$-bit operands A and B depicted by $A_{N-1}A_{N-2}$, …, $A_0$ and $B_{N-1}B_{N-2}$, …, $B_0$. To explore the regularity of the proposed comparator for arbitrary bitwidths, two operands $A$ and $B$ are applied into 4bit partitions as $A_{N-1}A_{N-2}A_{N-3}A_{N-4}$, …, $A_3A_2A_1A_0$ and $B_{N-1}B_{N-2}B_{N-3}B_{N-4}$, …, $B_3B_2B_1B_0$.

The complete process of comparison is divided into five sets, in which CEM contains sets 1–4 and FM contains only set 5. All the sets in the design are placed in four hierarchal prefix orders according to their functionality;

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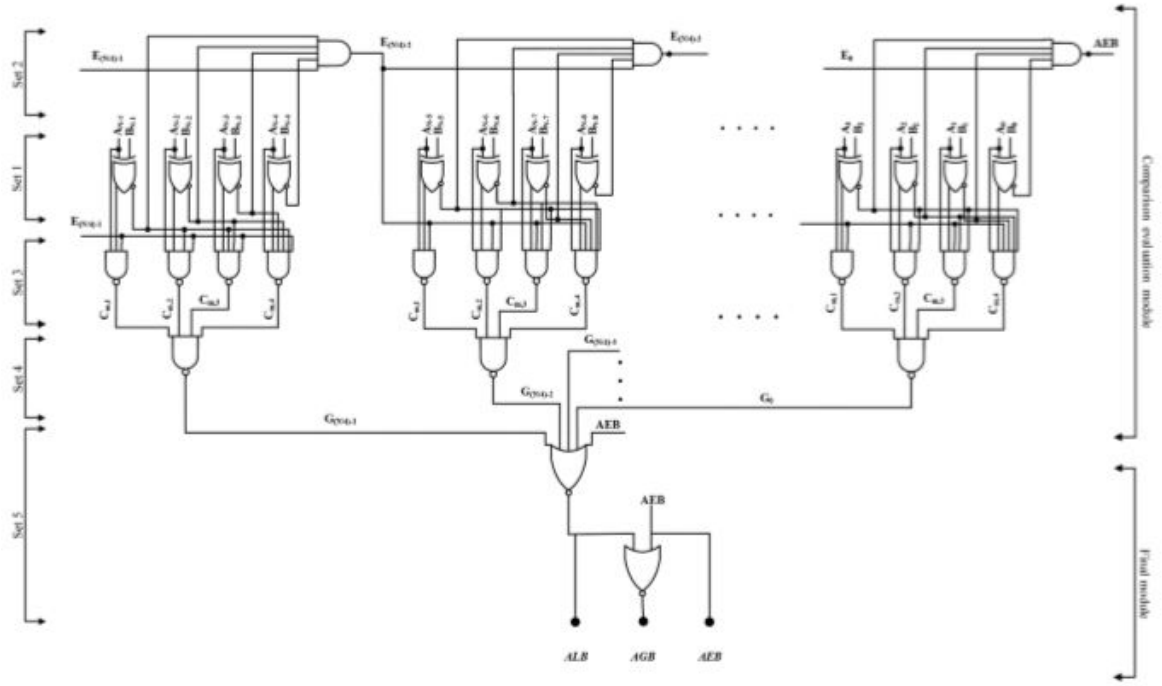
therefore, the output of each set in this approach serves as the input of another set with an exclusion of set 1, whose outputs act as the inputs of sets 2 and 3.In set 1, bitwise comparison of two *N*-bit binary operands is carried out by the novel EX–OR–NOR cell. The proposed structure of EX–OR–NOR cell is based on the pass transistor logic and CMOS logic. It uses seven transistors for EX– OR and EX–NOR operations as compared with the conventional eight transistors model [37]. The transistor M5 is used to obtain full output voltage swing of EX–NOR operation as shown in Fig. 6. The six transistors model has also been reported in [40] but it gives limited output voltage swing when applied input operands are (0, 0) or (1, 1). Optimum aspect ratios of the seven transistors (M1−M7) consisting of four P-channel MOS (PMOS) and three N- channel MOS transistors of the proposed EX–OR–NOR cell are carried out to avoid the universal drive constraint faced by the pass transistor logic. The novel structure uses a PMOS transistor in the feedback to maintain the logic level on the EX–NOR output terminal and the CMOS logic to boost up the output for achieving the full voltage swing on the EX–OR output terminal.The outputs of novel EX–OR–NOR cells provide the termination and comparison bits intended for sets 2 and 3 structures.




The proposed N-bit digital comparator is shown in Fig

## IV. COMMANDS

16bit comparator:
.include "Z:\Tanner EDA\Nanometer Technology Files\TSMC018.md"

V1 vdd GND 5
V2 a0 Gnd BIT ({100} )

V3 b0 Gnd BIT ({001 } )

V5 a1 Gnd BIT ({000} )
V6 b1 Gnd BIT ({001} )
V7 a2 Gnd BIT ({000} )
V8 b2 Gnd BIT ({001} )
V9 a3 Gnd BIT ({000} )
V10 b3 Gnd BIT ({001})
V11 a4 Gnd BIT ({000})
V12 b4 Gnd BIT ({001})

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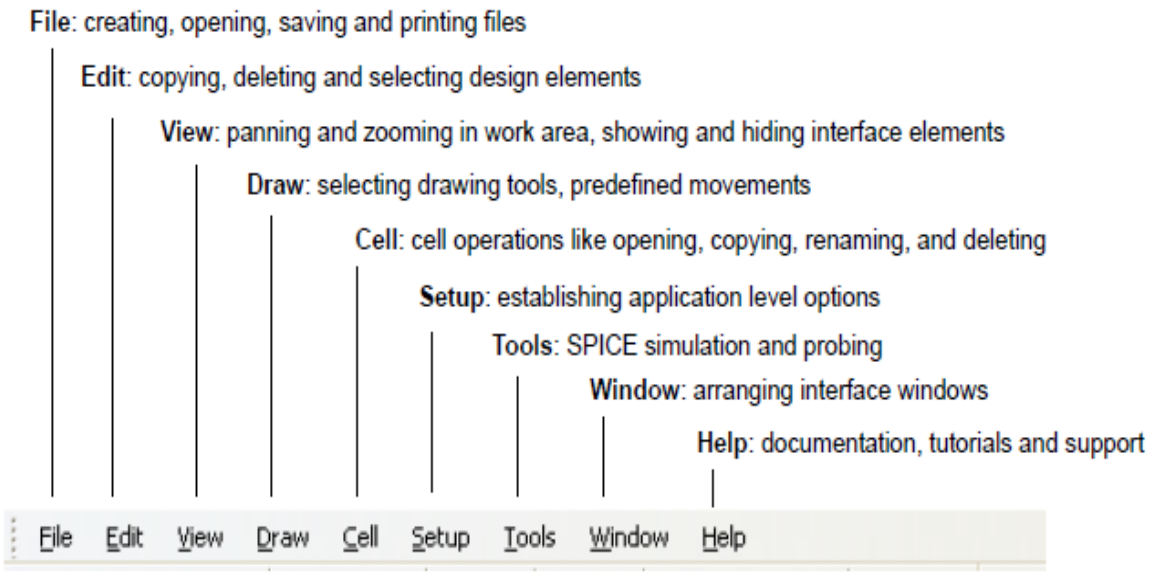
```
V13 a5 Gnd BIT ({000})
V14 b5 Gnd BIT ({001})
V15 a6 Gnd BIT ({000})
V16 b6 Gnd BIT ({001})
V17 a7 Gnd BIT ({000})
V18 b7 Gnd BIT ({001})
V19 a8 Gnd BIT ({000})
V20 b8 Gnd BIT ({0011})
V21 a9 Gnd BIT ({000})
V22 b9 Gnd BIT ({0011})
V23 a10 Gnd BIT ({000})
V24 b10 Gnd BIT ({001})
V25 a11 Gnd BIT ({000})
V26 b11 Gnd BIT ({001})
V27 a12 Gnd BIT ({000})
V28 b12 Gnd BIT ({001})
V29 a13 Gnd BIT ({000})
V30 b13 Gnd BIT ({001})
V31 a14 Gnd BIT ({000})
V32 b14 Gnd BIT ({001})
V33 a15 Gnd BIT ({100})
V34 b15 Gnd BIT ({001})
.print tran v(a0) v(AGB) v(ALB) v(AEB)

.measure tran DELAY trig V(a0) val=0.1 cross=1 targ v(AGB) val=0.1 cross=1

.tran 10n 100n

.end


.end
```

## V. SIMULATION RESULTS




The design cycle for the development of electronic circuits includes an important pre-fabrication verification phase. Because of the expense and time pressures associated with the fabrication step, accurate verification is crucial to

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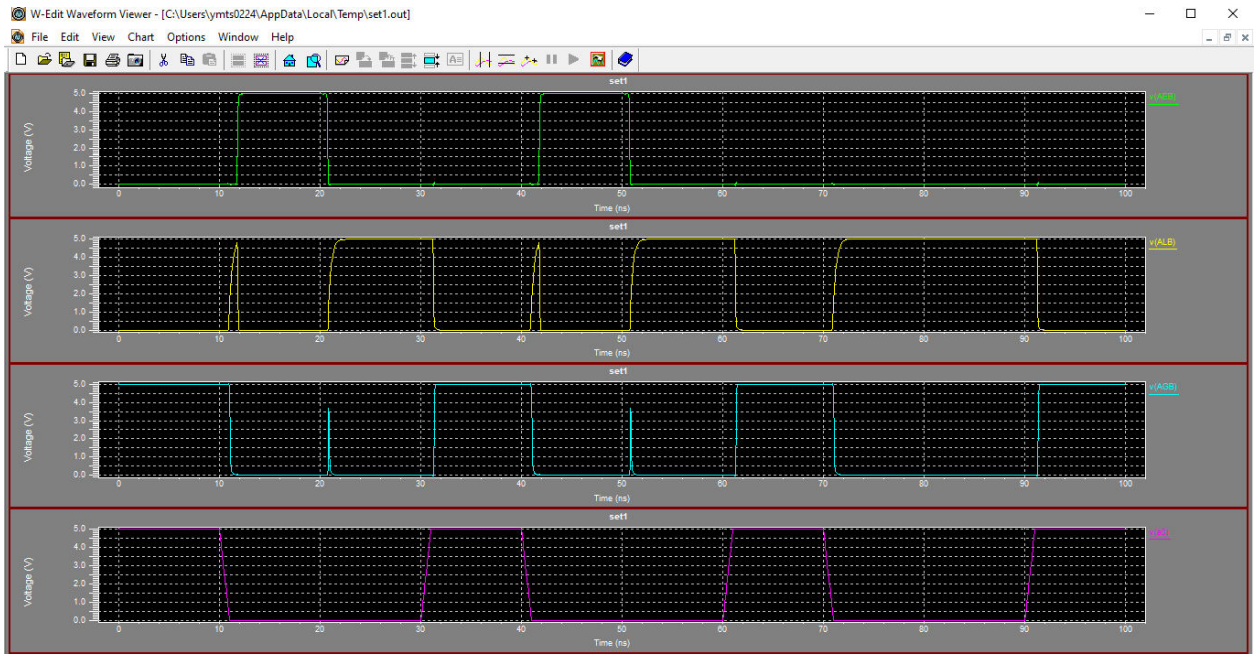
efficient design. The role of EDA tool is to help design and verify a circuit's operation by numerically solving the differential equations describing the circuit. These simulation results allow circuit designers to verify and fine-tune designs before submitting them for fabrication. Tanner EDA tool is a complete circuit design and analysis system that includes:

- Schematic Editor (S-Edit): Schematic editor is a powerful design capture and analysis package that can generate netlist directly usable in T-Spice simulations.
- T-Spice Circuit Simulator: T-Spice performs fast and accurate simulation ofanalog and mixed analog/digital circuits. The simulator includes the latest and best device models available, as well as coupled line models and support for userdefined device models via tables or C functions. T-Spice uses an extended version of the SPICE input language that is compatible with all industry standard SPICE simulation programs. All of SPICE's device models are incorporated, as well as resistors, capacitors, inductors, mutual inductors, single and coupled transmission lines, current sources, voltage sources, controlled sources, and a full complement of the latest advanced semiconductor device models from Berkeley and Philips Labs.
- Waveform Editor (W-Edit): W-Edit displays T-Spice simulation output waveforms as they are being generated during simulation. Visualizing the complex numerical data resulting from VLSI circuit simulation is critical to testing, understanding, and improving those circuits. W-Edit is a waveform viewer that provides ease of use, power, and speed in a flexible environment designed for graphical data presentation.




**Waveform of Proposed 16bit Comparator**

## V. CONCLUSION AND FUTURE WORK

In this paper, a novel scalable comparator using CEM and FM structures is proposed. The CEM comprises of the regular structure of repeated logic cells used for implementing parallel prefix tree structure. This regular structure can be used to predict the characteristics of the proposed comparator for arbitrary bitwidths. The proposed comparator has a maximum operating frequency, low-power dissipation and minimum FO4 delay as compared with existing comparators designed using 0.18µm CMOS technology. These advantages of the proposed comparator make it suitable for various applications such as scientific computations, test circuits, memory addressing logic etc.

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