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Implementation of Modified Baugh Wooley Signed Multiplier

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ABSTRACT: Adders and multipliers are fundamental building blocks in many computational units. The project is implemented on Wallace signed multiplier circuit in ASIC through modified Baugh-Wooley approach using standard conventional logic gates/cells, based on complementary pass transistor logic and have been validated with simulations, a layout vs. schematic check, and a design rule check. It is proved that the proposed multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, constant inputs, garbage outputs, hardware complexity, and number of transistors required. The Baugh-Wooley multipliers exhibit comparable delay, less power dissipation and smaller area.

KEYWORDS: Wallace signed multiplier, Baugh-Wooley approach, and standard conventional logic cells.

I. INTRODUCTION

Multiplication involves two basic operation generation of partial products and their accumulation. There are two possible ways to speed up the multiplication reduce the number of partial product or accelerate there accumulation. The project implemented on Wallace signed multiplier circuit in ASIC through modified Baugh-Wooley approach. Implemented by using the standard conventional logic gates/cells, based on complementary pass transistor logic and have been validated with simulations, a layout vs. schematic check, and a design rule check. Comparing to its existing counterparts with respect to the number of gates, constant inputs, garbage outputs, hardware complexity, and number of transistors required with Baugh-Wooley multipliers.

Multiplication is an important fundamental function in arithmetic logic operation. Computational performance of a DSP system is limited by its multiplication performance and since, multiplication dominates the execution time of most DSP algorithms therefore high-speed multiplier is much desired. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip. With an ever-increasing quest for greater computing power on battery-operated mobile devices, design emphasis has shifted from optimizing conventional delay time area size to minimizing power dissipation while still maintaining the high performance. Low power consumption is also important issue in multiplier design. To reduce significant power consumption it is good to reduce the number of operation thereby reducing dynamic power which is a major part of total power consumption so the need of high speed and low power multiplier has increased. Designer mainly concentrate on high speed and low power efficient circuit design. The objective of a good multiplier is to provide a physically packed together, high speed and low power consumption unit.

II. LITERATURE REVIEW

Charles R. Baugh and Bruce A. Wooley, member of IEEE presents “A Two’s complement parallel Array Multiplication Algorithm” in 1973. In this two’s complement, m-bit by n-bit parallel array multiplication is described. As multiplication is an essential function in digital system due to its necessity in operation of digital filters and Fourier transform processor. This paper presents an algorithm for parallel two’s complement multiplication. The advantage of

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the algorithm is the sign of all the partial products bits are positive, which allow the product to be formed using array addition technique. The drawback of the proposed algorithm is the need for the complements of each multiplier and multiplicand bit. [4] AswathySudhakar et al in 2010 proposed "High Speed Power-Efficient Modified Baugh-Wooley Multipliers", in this in this they proved modified Baugh-Wooley multiplier. Here comparison of various multiplier architecture for VLSI application. The baugh-wooley multiplier found to be best suited for the multiplication functionality according to resolution and efficiency. [10] K'Andrea et al presents, "Analysis of column compression multipliers" in 2001. This paper tests the proficiency of the area, delay and power characteristic of Dadda and Wallace multiplier. As operand word length increases, column compression multiplier increases roughly. Simulation indicate that, Wallace multipliers have 4% to 7% more area than equivalent Dadda multiplier, and approximately the same delay for operand sizes from 8 to 64 bits. [11] Andrew D. Booth present "A signed binary multiplication technique". In this a technique is described by which binary numbers of either sign may be multiplied together by a uniform process which is independent. In the design of automatic computing machines it is necessary to have two numbers whose signs are not necessarily positive. [12]

III. METHODOLOGY

- *Baugh Wooley Multiplier*

Baugh wooley technique was developed to design direct multipliers for complement numbers [1].When multiplying complement number directly each of the partial products to be added is a signed number. Thus each partial product has to be sign extended to the width of final product in order to form the correct by carry save adder tree. According to Baugh wooley approach, an efficient method of adding extra entries to bit matrix is suggested to avoid having to deal with negatively weighted bits in partial product matrix.Baugh Wooley method increases the height of longest column by two, which may lead to greater delay through the carry save Adder tree.

Modified form of Baugh wooley method is more preferable since it does not increase the column in the matrix. However this is type of multiplier is suitable for application where operand with less than 32 bit are processed like digital filter where small operand like 6,8,12 bits are used. Baugh wooley scheme become slowly and area consuming when operand greater than and equal to 32 bit.

IV. PROPOSED ALGORITHM

To compute product of two signed numbers we have used modified Baugh-Wooley approach [4]. Conventional multiplier design is divided into two parts: partial product generation circuit and then multi-operand addition circuit.

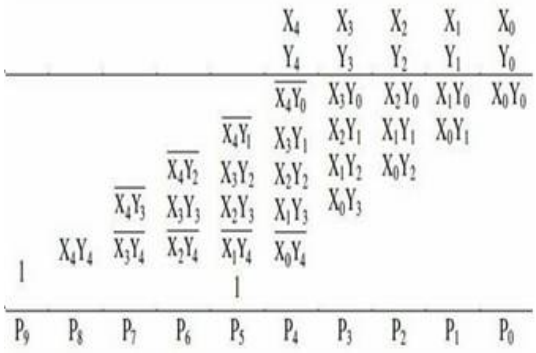

Fig.1. Modified Baugh-Wooley 5 x 5 Signed Multiplier

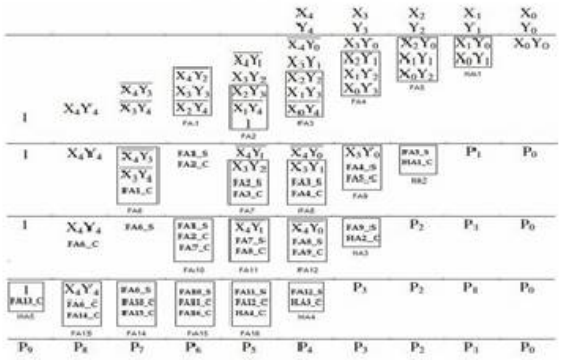

Fig.2. Multiplication by Wallace approach in the proposed Circuit

A. *DESIGN OF CONVENTIONAL MULTIPLIER*

First to compute partial product, 17 ANDs and 8 NANDs are used to employ the procedure given in Fig. 1. Aftergenerating partial products, next step is a multi-operandaddition. The bits of each column should be added given

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in Fig.1. To add these bits, FA and HA are used. The bits should added in such a way that our circuit will give the best results. Figure 2 shows the way of adding these bits in our proposedcircuit. The Wallace approach has been used to construct acircuit with less delay. To minimize delay in our proposedcircuit, P9 is computed by inverting carry output fromearlier (FA13). The resulting circuit for multi-operand additionneeds one 1-NOT gate, 4-HA and 16-FA as shown in fig.2. [2].

B. *PROPOSED ALGORITHM*

- To implement conventional multiplier using technology CMOS 600micrometer, structural Verilog code is written for the circuit.
- Then by using digital design flow from Cadence which uses :
  I. Cadence Encounter RTL Compiler.
  II. Encounter RTL-to-GDSII System.
- Then by using analog design flow from Cadence which uses :
  I. Virtuoso Schematic.
  II. Layout Editor Tools.
- Conventional multiplier is implemented with schematic and Layout.

V. SIMULATION RESULTS

Semi-custom ASIC design is carried out using Cadence tool [3]. To implement conventional multiplier, structural Verilog code is written for the circuit shown in Fig. 2. Then by using digital design flow from Cadence which uses Cadence Encounter RTL Compiler, Encounter RTL-to-GDSII System, Virtuoso Schematic and Layout Editor tools, we implemented conventional multiplier, schematic and Layout is shown in Fig. 3 and Fig. 4.

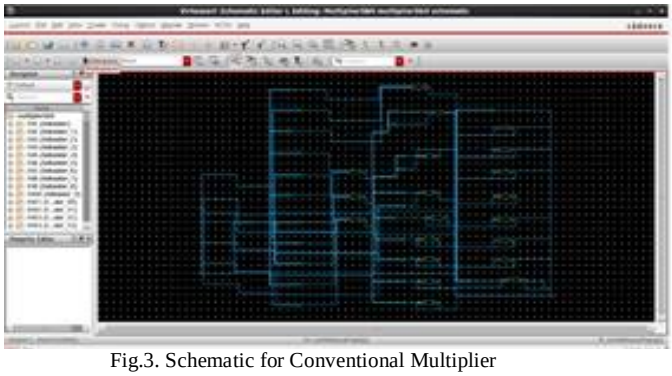

Fig.3. Schematic for Conventional Multiplier

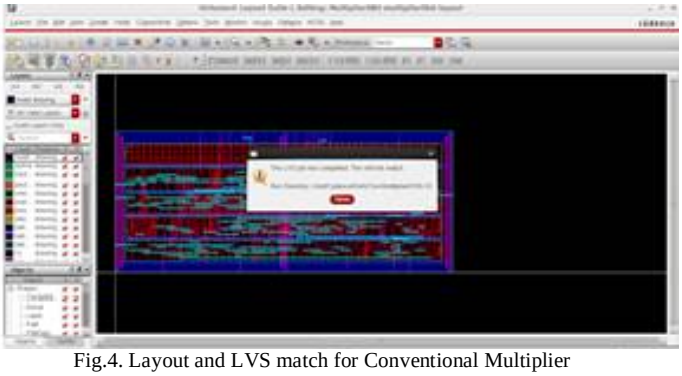

Fig.4. Layout and LVS match for Conventional Multiplier

For conventional multiplier, Schematic were validated by electrical simulations using Spectre, Layout has been successfully validated by the DRC and LVS check has successfully validated the functionality with respect to the schematic. For simulation of schematic and analog extracted view we written Digital Vector file which generates stimuli and performs vector check according to digital vectors using Virtuoso UltraSim Simulator, which is used in Virtuoso Spectre Mode. Finally the post extraction simulation is carried out for the circuits and calculated power dissipation values as shown in Fig. 5 and Fig. 6 for conventional multiplier.

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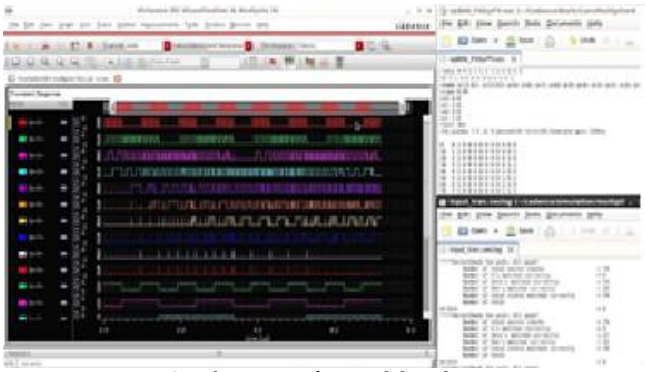

Fig. 5.Post Extraction Simulation waveform and digital vector file for conventional multiplier

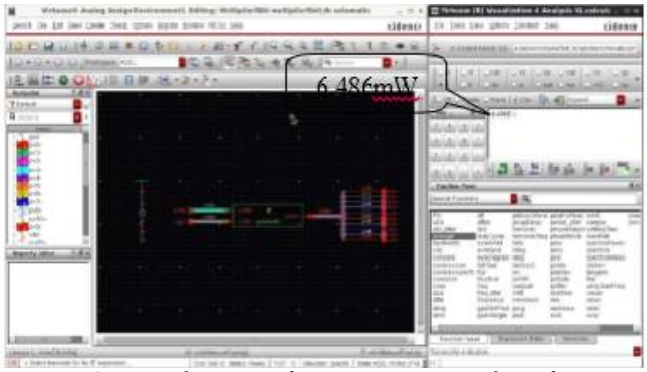

Fig 6. Power dissipation after post extraction simulation for Conventional Multiplier

VI. RESULTS

The table 1 shows the result of conventional multiplier where circuit is implemented by semi-custom ASIC design. It shows result in terms of power dissipation, numbers of transistors required and total area required for actual implementation of conventional multiplier circuit.

MULTIPLIER DESIGN	PROCESS TECHNOLOGY	POWER DISSIPATION	TRANSISTOR REQUIRED	PLACE ROUTE	TOTAL AREA
Conventional circuit	AMI06(C5N 0.6u)CMOS Process Technology	6.486mw	810	By Tool	389umX156um, With Power ring

Table 1. Results for proposed conventional signed multiplier circuit

VII. CONCLUSION AND FUTURE WORK

In this way, the Baugh Wooley signed Multiplier is implemented. It is proving that not only the proposed multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, constant inputs,garbage outputs, hardware complexity, and number of transistors required, but also results in low power dissipation in conventional logic design. Also, the standard cells were implemented in 0.6m CMOS using complementary pass transistor logic. These cells are prototype cells and knowledge for future improvements.

The proposed conventional multiplier placement and routing can be carried out by tool like Cadence Encounter. Optimization can be done by reducing the number of gates, or the circuit delays, but in this case it would also allow us to improve the placement and routing of cells. Number of required transistor can further be decreased in the implementation of multi-operand addition.

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