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Design and Analysis of Low Power Two Stage CMOS Op- Amp with 50nm Technology

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ABSTRACT: The main challenging issues in VLSI is reducing supply voltage and transistor channel length, so designing of high performance analog integrated circuits such as operational amplifier in CMOS technology becomes more critical. Scaling down of CMOS feature sizes enable yet faster speeds. In this project the two stage CMOS Operational amplifier (op-amp) has been designed using miller compensation technique. Miller compensation technique has been employed with two approaches first is using single capacitor miller compensation. Whereas second approach uses single miller compensation capacitor in series with nulling resistor. To achieve increased phase margin which indicate stability of a system, new design has been proposed with the help of second approach. The simulation was performed using micro wind tool.

Tool required: Micro wind software.

KEYWORDS: CMOS, op-amp, stability, low power dissipation, differential amplifier.

I. INTRODUCTION

Op-amp is among the most used electronic devices today, used in a wide range of consumer devices, industrial and scientific. High performance can be achieved by scaled down the MOS transistors which helps incorporation of more number of transistors on chip. Operational amplifiers are used as a basic building block in many analog and mixed signal systems. During designing of op-amp various electrical characteristics such as gain, offset, phase margin, unity gain bandwidth etc. all have taken into consideration. To meet the desired specification better compensation strategy and topology has to be selected. Among various introduced topologies, here we have chosen up two stage op-amp topology for high input impedance and low output impedance. In various op-amp applications, gain with single stage is not sufficient. To achieve higher gain more stages have to be introduced which provides additional phase shift to the system. For Closed loop circuit stability and well maintained magnitude and time response frequency compensation is needed. The important feature of compensation technique is that they can increase the phase margin. Operational amplifier can be used efficiently for practical consequences for example switched capacitor designing, analog to digital converters, and digital to analog converters, oscillator, waveform generators etc. The objective of this paper is to perform a comparative analysis between two stage CMOS Op-amp using miller compensation capacitor and two stage CMOS op-amp using compensation capacitor along with nulling resistor effect. Design has been carried out in micro wind software along with simulation results for different sizes of transistor.

Block Diagram of Two Stage CMOS Op-amp:

Op-amp is the backbone for many analog circuit designs. Designing amplification block to achieve high gain is not only the concern area for modern op-amp, it also includes proper biasing circuitry along with the effective compensation technique for stable operation.

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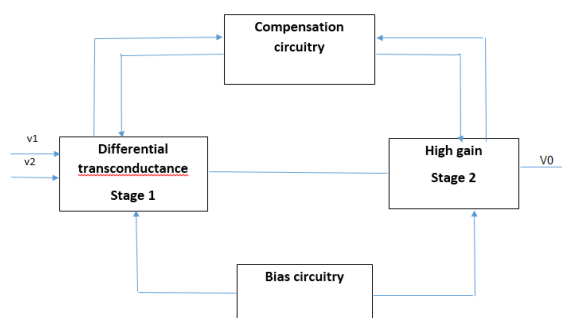


Figure 1. General structure of Two Stage CMOS op-amp

The block diagram consists of four functional blocks. The first block indicates Tran's conductance stage forms the input of the op-amp followed by the second stage simple differential pair amplifier. A common source amplifier generally meets the specification of the second stage. The second stage is mainly used to provide the large output swing with high DC gain for a given supply voltage. Again higher gain leads to lower bandwidth, so designer has to decide between these tradeoffs based on the specifications and the product requirements. Bias circuit is provided to establish the operating point for each transistor in its quiescent stage. The purpose of a compensation circuit is to provide stability to the closed loop performance. Since op-amps are designed to operate with negative feedback connection so frequency compensation is necessary for stability.

II. TWO STAGE CMOS OP-AMP WITH SCMC

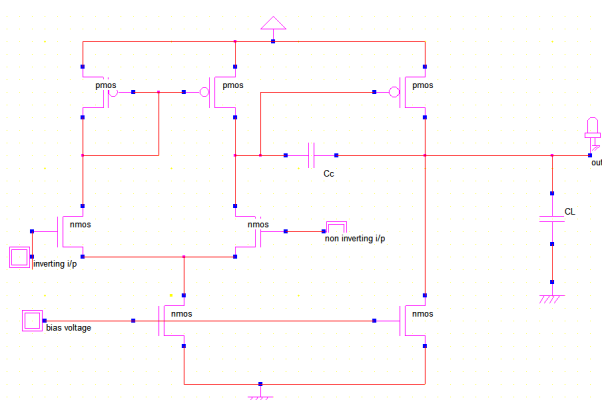


Figure 1: Two Stage CMOS op-amp with SCMC

The circuit designed to meet the required specifications the circuits consists of 7 transistors out of those 3 are PMOS and 4 are NMOS. Transistors M1, M2, M3, and M4 form the first stage of the op amp the differential amplifier with differential to single ended transformation. Transistors M1 and M2 are standard N channel MOSFET (NMOS) transistors which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The current mirror configuration comparison of M3&M4 used as an active load for input differential stage. Second stage uses current sink load inverter where M6&M7 as load. The output from drain of M2 will be amplified using current source configuration (M6). The mirror active load (M3&M4) use of active load

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devices creates a large output resistor in a relatively small amount of die area. Conversion from differential to single ended is achieved by CM (M3, M4). The current from M1 is mirrored by M3&M4 and subtracted from the current from M2. The differential current from M1&M2 multiplied by the output resistor of 1st stage gives single-ended output voltage, which constitutes the input of second gain stage. For current bias string (M5&M7) voltage is supplied between gain and source. However the compensation capacitance (Cc) connected between the outputs of the first and second gain stages, leads to a right-half plane (RHP) zero. In this method, stability is less and hence power dissipation is more.

III. PROPOSED METHOD

Two Stage CMOS Op-amp using SCMC with nulling resistor:

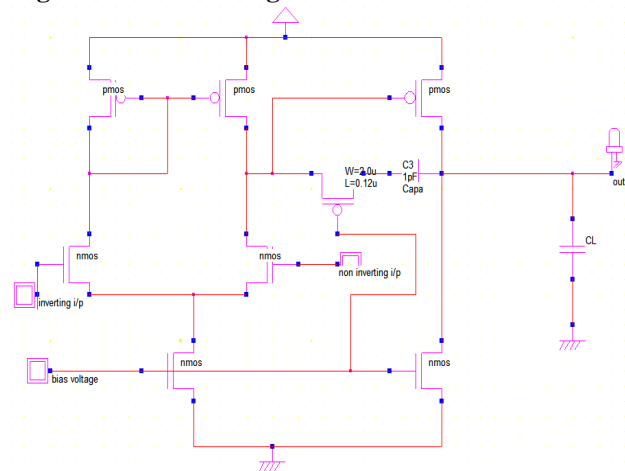


Figure 2. Two Stage CMOS op-amp Using SCMC with Nulling Resistor.

In this method, FET placed in series with Cc and FET acts as nulling resistor in triode region and FET occupies less space when compare with resistor. This FET does not allow the feed forward current from the output of first stage to input of second stage, so poles are shift to LHP results in stability and power dissipation decreases.

IV. SIMULATION RESULTS

Two Stage CMOS Op-amp with SCMC:

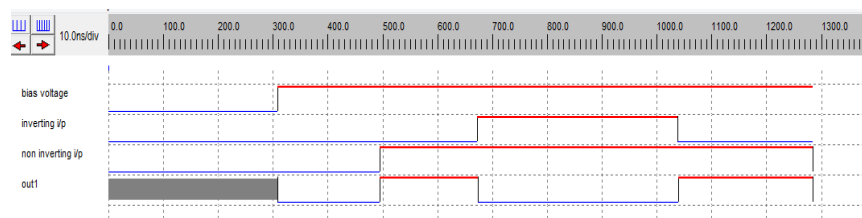


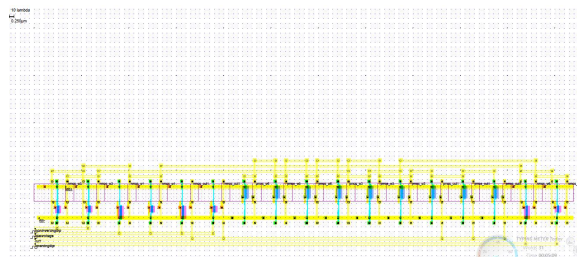
Figure 3. Timing waveform of SCMC.

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Layout of SCMC:



The operation starts when the bias voltage is applied for the circuit. If the inverting input is high then the output is high, other than this condition the output is low.

Two Stage CMOS Op-amp using SCMC with nulling resistor:

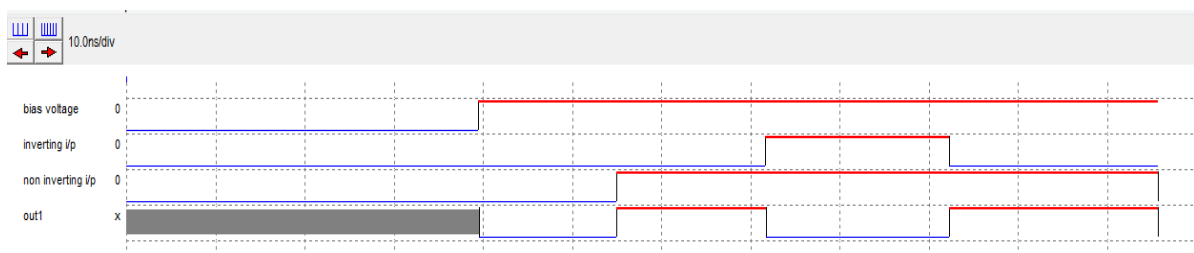
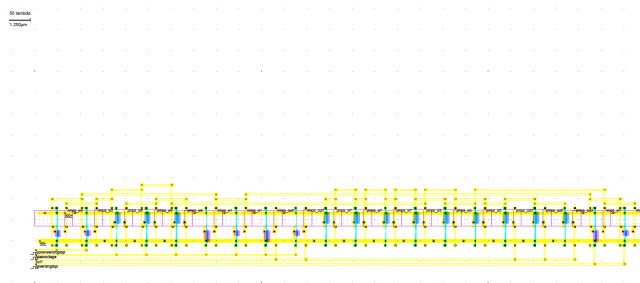


Figure 4. Timing waveform of SCMC with nulling resistor.

Layout of SCMC with nulling resistor:



The simulation is same as SCMC.



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Comparison of power dissipation of different size of transistors:

Size of transistor	Power dissipation for SCMC	Power dissipation for SCMC with NR
90nm	0.213mw	0.420mw
70nm	0.137mw	0.12mw
50nm	32.7 μ w	0.044 μ w

V. CONCLUSION

While designing several factors are taken into consideration such as area, power, supply voltage and current. Thus, to achieve optimized performance devices are scaled down accordingly. Along with negative feedback configuration addition of each stage in multistage op-amps introduces another pole in the system which creates stability problem. For this reason, a miller compensation technique has been employed in system. In this paper two stage CMOS op-amp with miller compensation technique has been designed and simulated at 180nm technology. Two Stage CMOS op-amp with SCMC approach provides max gain and min phase margin. In second approach, two Stage CMOS op-amp Using SCMC with nulling Resistor increase the phase margin, which indirectly makes system more stable, miller compensation capacitor is used in series with nulling resistor, which provides gain of low dB and phase margin of high degree. Apparently there is not a single point of scaling while designing, designers have to perform scaling depending upon the requirements or the specifications laid for a particular product.

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