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Fault Detection in Combinational Circuit (Full Adder) Using Prolog

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ABSTRACT: The complexness of integrated circuits is increasing whereas dependability of the elements is decreasing because of tiny gates and junction transistor. one amongst the impacts of technology scaling is a lot of sensitivity to transient and permanent faults. So, fault tolerant system plays vital role in vital application wherever immediate act isn't doable. For reliable and economical operation of a system, the detection of the transient fault is important. it's terribly troublesome to observe these faults offline. The fault tolerant circuits will observe the faults and tolerate the detected faults. So, AN economical fault observation style is projected for full adder during this paper which may detect the faults with their actual location and additionally tolerate the faults. The projected styles will observe the faults in single and multi-internet. Inductive Logic Programming (ILP) is programing language we have a tendency to area unit attending to employed in programing language software system to style our system. Inductive Logic Programming (ILP) could be a new discipline that investigates the inductive construction of first-order expression theories from examples and background. First, varied downside specifications of ILP area unit formalized in linguistics settings for ILP, yielding a "model-theory" for ILP Second, a generic ILP algorithmic program is bestowed. Third, the logical thinking rules and corresponding operators employed in ILP area unit bestowed, leading to a "proof-theory" for ILP Fourth, since inductive logical thinking doesn't manufacture statements that area unit assured to follow from what's given, inductive inferences need another sort of justification. this could take the shape of either probabilistic support or logical constraints on the hypothesis language.

I. INTRODUCTION

As transistors become progressively smaller and quicker and noise margins become tighter, circuits and chip particularly microprocessors tend to become additional susceptible to permanent and transient hardware faults. Most micro chip designers specialize in protective memory components among different components of microprocessors against hardware faults through adding redundant error-correcting bits like parity bits. However, the speed of soppy errors in combinatory components of microprocessors is contemplating edas necessary as in serial components like memory components these days. the explanation is that advances in scaling technology have light-emitting diode to reduced electrical masking. This paper proposes and evaluates a logic level fault-tolerant methodology supported parity for coming up with combinatory circuits. Experimental results on a full adder circuit show that the projected methodology makes the circuit fault- tolerant with less overhead compared with ancient ways. it'll even be incontestable that our projected methodology allows the standard TMR methodology to find multiple faults additionally to single fault masking. Inductive Logic Programming (ILP) may be a analysis space fashioned at the intersection of Machine Learning and Logic Programming. ILP systems develop predicate descriptions from examples and background. The examples, background and final descriptions area unit all represented as logic programs. A unifying theory of Inductive Logic Programming is being engineered up around lattice-based ideas like refinement, least general generalization, inverse resolution and most specific corrections. additionally to a well-established tradition of learning-in-the-limit results, some results among Valiant's PAC-learning framework are incontestible for ILP systems. U-learnabilty, a replacement model of learnability, has conjointly been developed. Presently successful applications areas for ILP systems embody the educational of structure-activity rules for drug style, finite-element mesh analysis style rules, primary-secondary prediction of supermolecule structure and fault identification rules for satellites.

Inductive Logic Programming (ILP) may be a new discipline that investigates the inductive construction of first-order expression theories from examples and background. we tend to survey the foremost necessary theories and ways of this

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new field. First, numerous drawback specifications of ILP area unit formalized in linguistics settings for ILP, yielding a "model-theory" for ILP. Second, a generic ILP algorithmic rule is bestowed. Third, the abstract thought rules and corresponding operators employed in ILP area unit bestowed, leading to a "proof-theory" for ILP. Fourth, since inductive abstract thought doesn't turn out statements that area unit assured to follow from what's given, inductive inferences need another style of justification. this could take the shape of either probabilistic support or logical constraints on the hypothesis language. data compression techniques used among ILP area unit bestowed among a unifying theorem approach to confirmation and certification of hypotheses. Also, other ways to constrain the hypothesis language or specify the declarative bias area unit bestowed. Fifth, some advanced topics in ILP area unit self-addressed. These embody aspects of procedure learning theory as applied to ILP, and therefore the issue of predicate invention. Finally, we tend to survey some applications and implementations of ILP. ILP applications make up 2 totally different categories: initial, scientific discovery and information acquisition, and second, programming assistants.

II. LITERATURE SURVEY

The basic methodology of classification of any system is started with pure mathematics. almost like pure mathematics we've rough pure mathematics. As a mathematical data discovery tool for large knowledge [6], rough pure mathematics has been wide employed in the sector of higher cognitive process and intelligent management. In bio-information field, it's wont to analyze organic phenomenon knowledge - to find the potential causative relationship between human body and sure illness like cancer. And such effort has initial rewards. we have a tendency to believe that police investigation anomaly sequence in human-being is comparable with anomaly detection in cluster nodes in several aspects. First, human illness and cluster node anomaly area unit all caused by the mal-function of sure half. Second, such mal-function should have some relationship with expression knowledge of human sequence or node options. By applying rough pure mathematics in cluster node faulty detection, we are able to realize the hidden relationship between sure options and anomalies.

Pancreatic malignant growth may be a staggering sickness and foreseeing the standing of the patients turns into a major and pressing issue. The creators investigate the materialness of inductive principle programming (ILP) strategy within the malady and demonstrate that the collected clinical center data may be used to foresee sickness qualities, and this can raise the selection of remedial modalities of exocrine gland malignant growth. The accessibility of heaps of clinical research facility data offers items of knowledge to assist within the learning speech act of ailments. In foreseeing the separation of growth and also the standing of humor hub metastasis in exocrine gland malignancy, utilizing the ILP model, 3 tips area unit engineered up that area unit steady with portrayals within the writing. the rules that area unit recognized area unit valuable to differentiate the separation of growth and also the standing of humor hub metastasis in exocrine gland malignant growth and during this manner contributed altogether to the selection of remedial systems. What is more, the projected strategy is contrasted and also the alternative commonplace characterization procedures and also the outcomes any affirm the prevalence and worth of the projected technique.

As AN implementation platform is on FPGA we have a tendency to fill have several advantage .The susceptibleness of digital systems to faults needs the implementation of Fault Tolerant architectures to make sure high-reliability and convenience. Field Programmable Gate Arrays area unit particularly sensitive to Single-Event Upsets and Single-Event Transients, since the configuration memory of the chip may be affected, leading to permanent error; therefore, special care should be taken once implementing Fault Tolerant architectures for FPGAs. This paper describes the design of a Fault Tolerant soft-core processor mistreatment triplication of all units still as employing a parity protection theme for on-chip caches, presenting the impact on space, clock frequency and I/O needs of each implementations, targeting FPGAs[8]. Experiments show a high fault tolerance and demonstrate the link of cache hit rates with fault propagation.

This paper bestowed OntoILPER, AN ILP-based methodology for extraction relations instances from matter knowledge. OntoIL-PER has the advantage of exploiting a site metaphysics in its extraction method that opens new opportunities in RE. OntoILPER integrates each a hypothesis house that allows the finding out candidate hypothesis

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house, ANd an ILP-based learning part that induces Horn-like extraction rules from annotated examples. we have a tendency to revised the literature and located that a lot of similar ILP-based RE systems don't integrate linguistics resources or ontologies in their i.e. method. Contrastingly, OntoILPER permits for integration helpful background in many ways, notably by exploiting a site metaphysics given as input. OntoILPER was assessed on 2 normal datasets for RE. The yielded results incontestible the OntoILPER effectiveness; however there's still area for improvement.

A large portion of this learning ways for NER and RE depend upon regulated AI systems with additional precise outcomes for NER than RE. This paper presents OntoILPER a framework for separating part and affiliation occasions from unstructured writings utilizing philosophy and Inductive Logic Programming, AN emblematic AI methodology. OntoILPER utilizes the world cosmology and exploits a better communicatory social speculation house for chatting with models whose structure is vital to i.e.. It prompts extraction decides that subsume instances of components and affiliation occurrences from a selected chart based mostly model of sentence portrayal. Moreover, OntoILPER empowers the abuse of the world cosmology and any foundation data as social highlights. To assess OntoILPER, some tests over the TREC corpus for each NER and RE undertakings were LED and also the yielded outcomes show its adequacy within the 2 errands. This paper likewise offers a close to analysis among OntoILPER and alternative NER and RE frameworks, demonstrating that OntoILPER is aggressive on NER and outflanks the selected frameworks on RE.

III. PREVIOUS FAULT TOLERANT DESIGN APPROACHES

Various existing approaches square measure is accessible for achieving fault tolerance. Redundancy is common altogether. There are two sorts of redundancy: time redundancy, hardware redundancy that is needed within the self-checking system is described concisely during this section. every one of them has some advantages and disadvantages square measure delineated below.

A. Time redundancy: In Time redundancy approach repetition of the computation or transmission of the info 2 or a lot of times and that we compared the result with the result obtained at the various interval of time (or antecedently keep data). The distinction within the time interval is given by the delayed clock. By the delayed clock time interval distinction is made between 2 perennial computations. Just in case of the transient fault, if we tend to continuance the computation twice, as shown in fig.1 and once the recomputed result not the same as antecedently keep lead to that condition fault is detected. If each the results square measure the same then it's a fault-free condition. By victimization this method we will observe all transient and intermittent faults at totally different intervals of your time however not the both along [9]. Permanent fault can't be known by victimization the antecedently used theme as shown in fig.1 however we will additionally detect and proper permanent fault if we tend to combine some encoding theme with time redundancy. There is some limitation during this approach one in all them is that for computation repetition we want some information that's a gift in the system. because of the transient fault system going towards failure, which produces the computation tough or impracticable to repeat. Propagation of the result's done when 1st computation and if there's a fault gift in 1st computation it's propagated to the opposite module before police investigation the fault due to that alternative module results become faulty. The positive aspect of your time redundancy is that it will differentiate transient and permanent fault. we will say it's transient if the fault is vanishing when recomputation [10]. Time redundancy has lower hardware and software package overhead as compared to other redundancy techniques.

B. Hardware redundancy: In the hardware redundancy approach we tend to use some further hardware (everyone is identical) to perform the parallel computation to identified fault or fault-free condition and mask out the fault or further hardware replaced the faulty component. Hardware redundancy has few disadvantages like it takes more time to style, fabricate and check, weight and size increased because of the employment of additional hardware and its additionally increased the value and power consumption. In hardware redundancy, there square measure 2 most usually used approaches, i.e. triple standard redundancy and double standard redundancy.

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IV. METHODOLOGY

Inductive Logic Programming (ILP) is a subfield of machine learning that learns computer programs from data, where the programs and data are logic programs. It may also be explained as a form of supervised machine learning which uses logic programming (primarily Prolog) as a uniform representation for background knowledge, examples, and induced theories. ILP is preferred over other machine learning approaches because of its easy comprehensibility, intelligibility, and ability to include additional information in the learning problem.

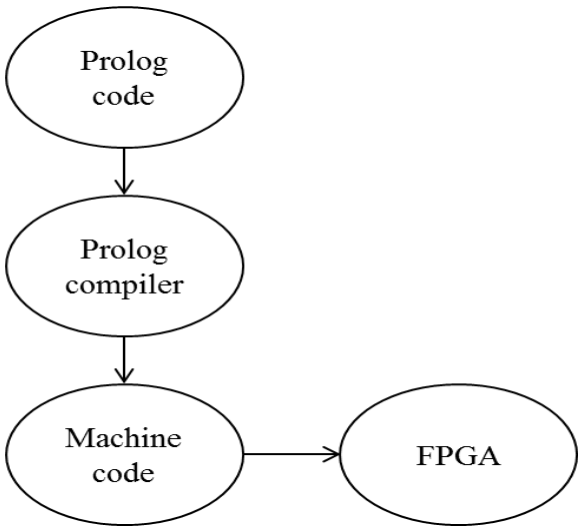

Fig 1 block diagram of proposed system

Inductive language programming method is used to detect fault in hardware models because its coding is easy and it checks every alternative option to detect fault. Prolog compiler compiles program and convert file into metlist file as shown in figure 1. This metlist file is then converted to hex file as machine code. This code is then fed to FPGA.

Packaging is classed mutually of back-end processes within the integrated circuits (ICs) producing, xtremely capital-intensive and involves advanced processes. in contrast to the front-end method that fabricates wafers, the back-end method isn't uniform. Because of the complexness of the method and increasing sort of merchandise, the packaging manufacturing plant sometimes encounters complaints that may be classified into categories looking on the loss. we tend to apply rough pure mathematics to find vital attributes resulting in complaints and induce call rules supported the information of a Taiwanese IC packaging manufacturing plant that ranks one in every of the biggest within the world. The data contain 454 records and every record includes eleven condition attributes still mutually call attribute characterizing the category. We first obtain vital set of attributes that ensures prime quality of classification, so we tend to generate rules for every category of complaints [9].

High-speed, accuracy, meticulosity and fast response area unit notion of the important necessities for contemporary digital world. An efficient electronic circuit unswervingly affects the makeover of the total system. Different tools area unit needed to unravel differing types of engineering tribulations. up the efficiency, accuracy and low power consumption in associate electronic circuit is often been a bottle neck downside. Therefore, the want of circuit miniaturization is often there. It saves a lot of your time and power that's wasted in change of gates , the wiring-crises is reduced, cross- sectional space of chip is reduced, the amount of transistors which will enforced in chip is multiplied several folds. thus to trounce with this downside we've planned associate Artificial intelligence (AI) based mostly approach that make use of Rough pure mathematics for its implementation. Theory of rough set has been proposed by

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Z Pawlak within the year 1982. Rough set theory may be a new mathematical tool that deals with uncertainty and unclearness [10].

In complicated and bad natural environment, the performance of electronic system may be easily affected by the environment, go wrong and result in abnormal operation. In the complicated environment like deep space and deep sea, if the electronic equipment after break down cannot be repaired in time, it will cause serious loss. However, the fault self-repairing technique proposed based on hardware evolution can realize self-repairing of fault. The paper firstly expounds the basic theory of hardware evolution and introduces foreign and domestic situation of fault self-repairing based on hardware evolution in details. Then, it explains important procedures in fault self-repairing and points out the existing problems and improvement direction. Fault self-repairing based on hardware evolution has very broad prospect and great engineering application value[11].

Full Adder in Digital Logic

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.

A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to the another.

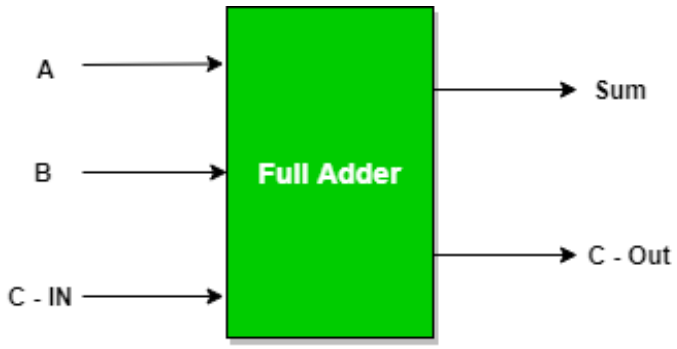

Fig. 2 Full Adder

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table -1 Full Adder Truth

Logical Expression for SUM:

= A’ B’ C-IN + A’ B C-IN’ + A B’ C-IN’ + A B C-IN

= C-IN (A’ B’ + A B) + C-IN’ (A’ B + A B’)

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= C-IN XOR (A XOR B)
= (1,2,4,7)

Logical Expression for C-OUT:
= A' B C-IN + A B' C-IN + A B C-IN' + A B C-IN
= A B + B C-IN + A C-IN
= (3,5,6,7)

Another form in which C-OUT can be implemented:
= A B + A C-IN + B C-IN (A + A')
= A B C-IN + A B + A C-IN + A' B C-IN
= A B (1 +C-IN) + A C-IN + A' B C-IN
= A B + A C-IN + A' B C-IN
= A B + A C-IN (B + B') + A' B C-IN
= A B C-IN + A B + A B' C-IN + A' B C-IN
= A B (C-IN + 1) + A B' C-IN + A' B C-IN
= A B + A B' C-IN + A' B C-IN
= AB + C-IN (A' B + A B')
Therefore COUT = AB + C-IN (A EX – OR B)

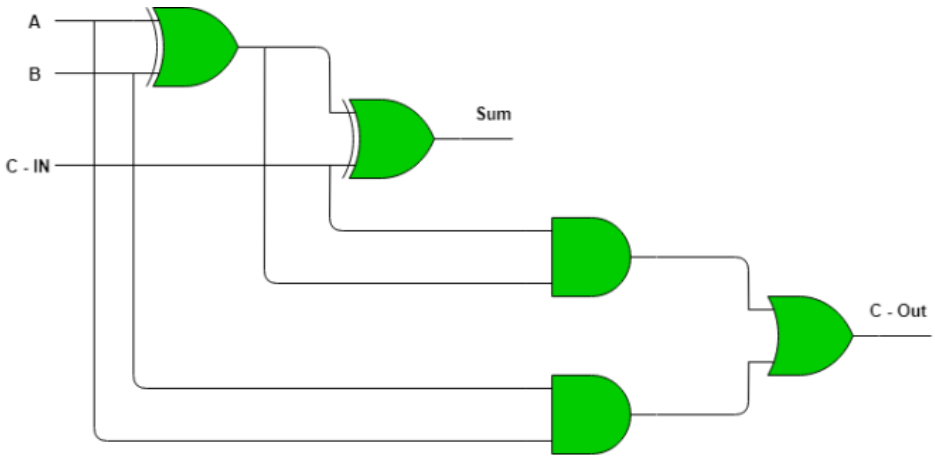

Fig.3 Implementation of Full Adder using Half Adders

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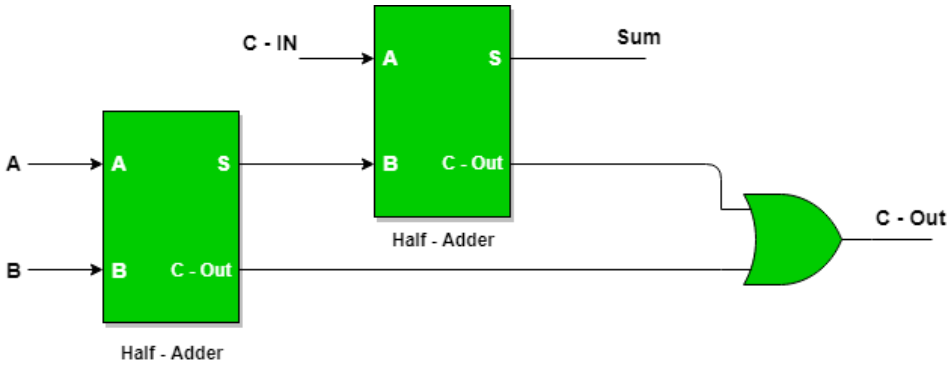

Fig.4 Half Adders and a OR gate is required to implement a Full Adder.

With this logic circuit, two bits can be added together, taking a carry from the next lower order of magnitude, and sending a carry to the next higher order of magnitude.

V. RESULTS

Fig 5 half adder

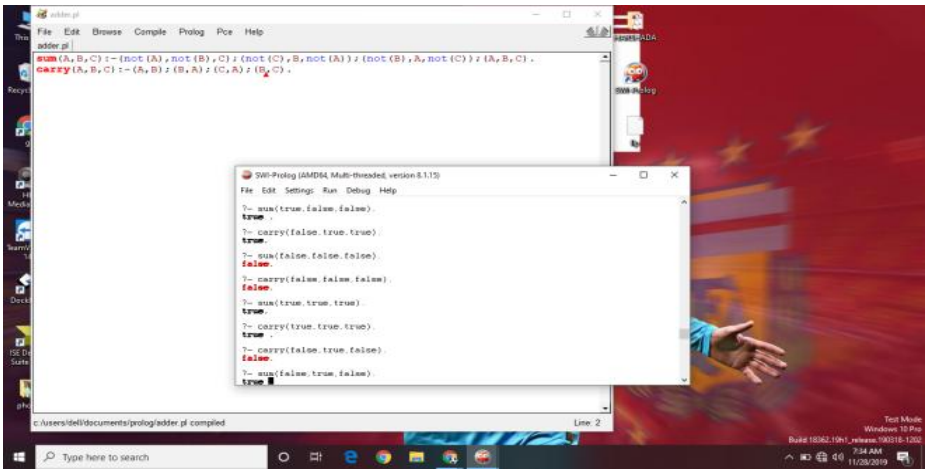

Fig 6 full adder result

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VI. CONCLUSION

The integration level in today's word is continuously increasing in VLSI chips. So that complexity of testing is a major challenge. That is because the internal chip modules have become increasingly midcult to access. There is a significant amount of the testing cost as compared to the total manufacturing cost. Hence there is a necessity to reduce the testing cost. The main factor is the time required to test the circuitry that has the biggest impact on testing cost of a chip. Inductive Logic Programming (ILP) is used to detect fault in Full Adder circuit.

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