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Comparison Between Power Dissipation, Delay And Area Adders

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ABSTRACT: Due to continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of integrated circuits. Low power consumption and smaller area are some of the most important criteria for the fabrication of DSP systems and high performance systems. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip.
Therefore comparison has been carried out by assuming the circuits with minimum size transistors, to minimize the power consumption. Power consumption is a function of load capacitance, frequency of operation, and supply voltage.

I. INTRODUCTION

Rapid growth in semiconductor technology has led to shrinking of feature sizes of transistors using deep submicron (DSM) process. Modern portable battery operated devices such as cell phones, laptops; PDAs are particularly affected by this as high power dissipation reduces battery service life. The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Therefore, in realizing modern Very Large Scale Integration (VLSI) circuits, low-power and high-speed are the two predominant factors which need to be considered. Like any other circuits' design, the design of high-performance and low-power adders can be addressed at different levels, such as architecture, logic style, layout, and the process technology. As the result, there always exists a trade-off between the design parameters such as speed, power consumption, and area. Recently, the requirement of probability and the moderate improvement in battery performance indicate power dissipation is one of the most critical design parameters day by day the demand of probability and mobility is increasing.
Also the area of chip design is taken into consideration while talking about probability. Hence three most widely accepted parameters to measure the quality of a circuit or to compare various circuit styles are area, delay and power dissipation. There are three major sources of power consumption in digital CMOS circuits, which are summarized in the following equation

$$P_{Total} = P_{Switching} + P_{Short+Circuit} + P_{Leakage}$$

BASIC TYPES OF ADDER

Adders are commonly used in the critical path of many building blocks of microprocessors and digital signal processing chips. Adders are critical component not only for addition, but also for subtraction, multiplication, and division. Addition is one of the fundamental arithmetic operations. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. The most important parameter for measuring the quality of adder designs is propagation delay, and area.
Adder or summer is a digital circuit that performs addition of numbers. In modern computers adders reside in the arithmetic logic unit (ALU) where other operations are performed. Although adders can be constructed for many numerical representations, such as Binary-coded decimal or excess-3, the most common adders operate on binary numbers.

1.1 Application of Adders

- Used in CPU side
- Used in networking side
- Used in DSP oriented system
- In application-specific processors
- In biomedical applications
- In image processing and video processing.

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Types of Adder

For single bit adders, there are two general types of adders which are given below

1. Half Adder
2. Full Adder

1.2 GDI ADDER

The fig 1 shows the CMOS transistor level implementation of Modified conventional CMOS full adder design using 20 Transistor model which is the heart of the arithmetic unit. This type of CMOS full adder configuration has been widely used in numerous applications. It often exhibits a critical delay that actually limits the system performance. Two or more full adders are cascaded together to perform multiple bit addition .

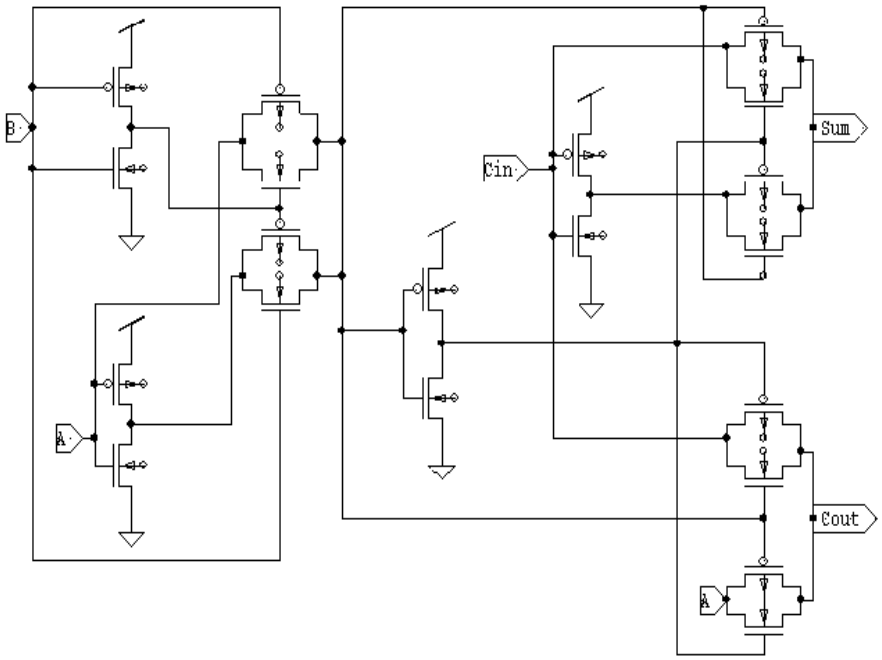

Fig :1. Circuit Diagram of GDI Adder

1.2 GDI ADDER

A new low power design technique that solves most of the problems is known as Gate-Diffusion-Input (GDI) method. This technique reduces power consumption, propagation delay, and area of digital circuits. GDI method is based on the use of a simple cell as shown in below figure. At the first look the design seems to be like an inverter, but the main differences are

1. GDI consist of three inputs- G (gate input to NMOS/PMOS), P (input to source of PMOS) and N (input to source of NMOS).
2. Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biasedat contrast with CMOS inverter.

By using this method a wide variety of logic functions can be implemented using only two transistors. Schematic diagram of GDI based adder is shown in fig2

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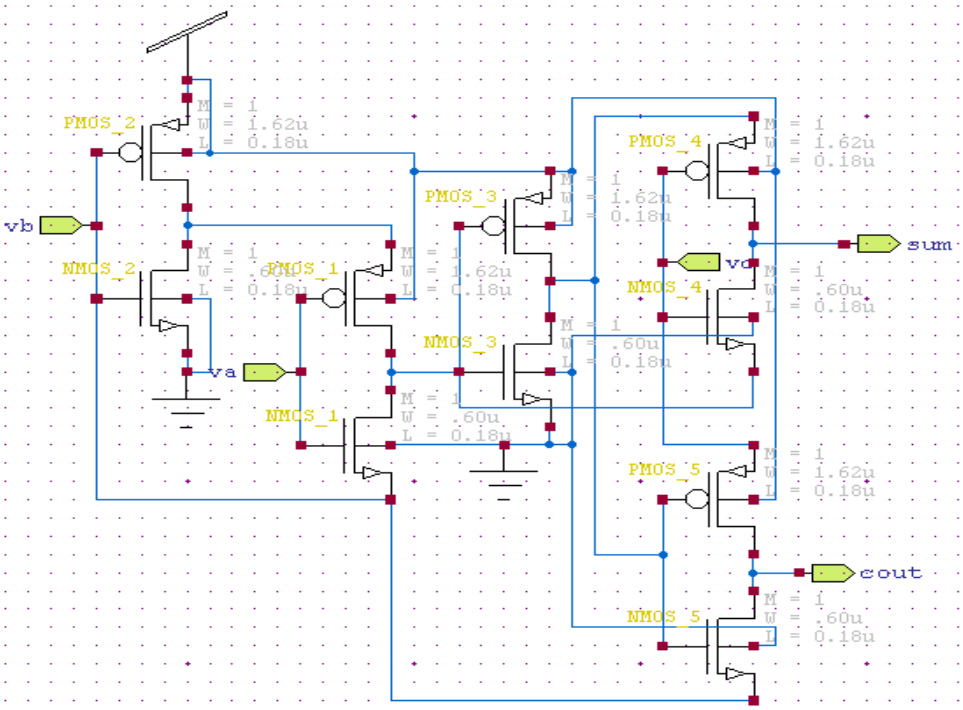

Fig 2: Schematic Diagram of GDI Adder

This method is also suitable for designing fast, low-power circuits, using a less number of transistors, while improving logic level swing and static power characteristics and allowing simple top down design by using small cell library

II. SIMULATION RESULT

GDI ADDER

Simulated waveform of GDI based full adder is shown in fig 5.9. Sumbit is obtained from

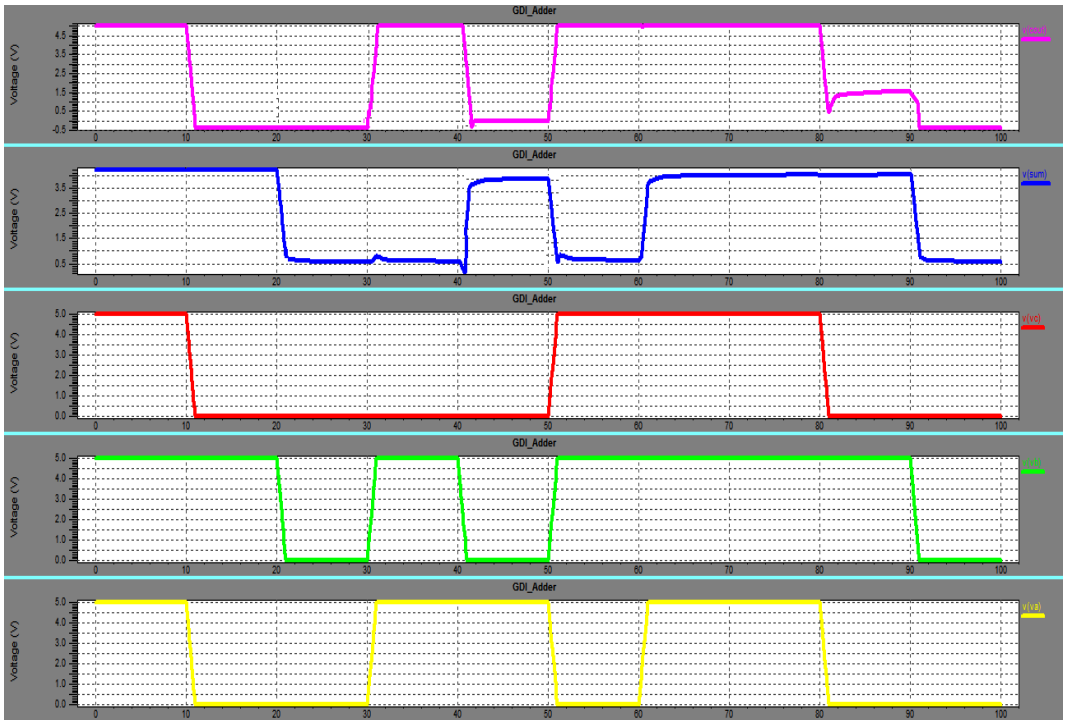

Fig 3: Simulated waveform of GDI based Adder

the output of the second stage of XOR circuit while Carry bit (C out) is calculated by multiplexing B and C in controlled by (A XNOR B). When both inputs (va and vb) and carry in (vc) is logic '1' then both outputs sum and carry out (C out). When even number of inputs to the adder are logic '1', then sum is '0' and C out is logic '1' & for odd numbers of input sum output is logic '1' and C out is '0' as shown in fig 3.

Advantage: These features give the GDI cell two extra input pins to use which makes it flexible than usual CMOS design. It is also a genius design which is very power efficient without using large amount of transistor count.

Disadvantage: Major problem of GDI method is that twin-tub CMOS or silicon on insulator (SOI) process is used to fabricate. Thus, it will be more expensive to realize a GDI chip. Moreover if only standard p-well CMOS process is used, the GDI scheme will face the problem of lacking driving capability which makes it more expensive and difficult to realize as a feasible chip**.**

III. CONCLUSION

In this dissertation adder has been designed and simulated using 180 nm CMOS technology of tanner tool at a various supply voltage from 1.0V to 1.8 V& compare their results with respect to various parameter. The comparison has been carried out both assuming circuits with minimum transistors size, to minimize the power consumption. Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heat sinks. This provides the consumer with a product that costs less. In this paper we conclude that

- The power consumption of GDI based adder is 50% less from RBSD adder but 26% less speed as compared to conventional RBSD adder.

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