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Low Power Energy Efficient Level Shifter in Multi supply Voltage Design

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ABSTRACT: Multi supply voltage design (MSVD) emerging as an effective technique to trade off between speed and energy. Level shifter are used for interface different voltage domains. In this brief, a low power energy efficient level shifter is presented which is able to convert low level input voltage to high level voltage domain. To obtain low static power consumption, the proposed level shifter is based on the single stage differential cascade voltage switch scheme. Moreover, it exploit self-adapting pull-up network to increase switch speed and to reduce dynamic energy consumption, and a split input inverting buffer is used at the output stage to improve energy efficiency. When implement in a 180 nm CMOS process, the proposed level shifter can up-convert from 100 mV input signal into 1.8 V output signal. For target voltage conversion from 0.4 V to 1.8 V, our level shifter exhibits an average propagation delay of 12.56 ns, an static power dissipation 360 pW and an energy per transition of 51.2 fJ.

KEYWORDS: Level Shifter (LS), Multi Supply Voltage Design (MSVD), Low Power, Low Voltage.

I. INTRODUCTION

Energy efficiency is one of the most important issue address in today's system on chip design. To reduce power consumption, among various techniques known in the literature are based on power supply voltage reduction, are considered very effective even though they can severely penalize speed performance [1].
An alternative approach, known as multi supply voltage domain technique [2] is gaining broad popularity for the design of advance system on chips (SoCs). It is used to reduce both dynamic leakage power. This approach consist of partitioning the design into separate voltage islands (or "voltage domains") each operating at a proper power supply voltage level depending on its timing requirement. Time critical domain work on higher supply voltage (VDDH) to maximize the performance, while non-critical section work at low supply voltage (VDDL). In this way dynamic and static power can be reduced without impacting on the overall circuit performance. For extremely low power applications, the presence of the section of system operating in sub-threshold regime is a valuable option.[3]
A key challenge in design of efficient multi supply circuits is minimizing the cost of voltage level conversion between different voltage domains. While maintain the overall of the design level shifter circuits have to be used for these type of purpose [3].
This paper deals with a low power energy efficient LS design to convert near or sub threshold voltages to above threshold voltage level. When implemented with cadence virtuoso 180 nm CMOS technology process, the new design converts input voltage as low as 100 mV into 1.8V nominal output voltage, with delay of 12.56 ns and static power consumption 360 pW for VDDL = 0.4 V.

II. RELATED WORK

Several level shifter (LS) circuits were recently proposed [4-9] to allow voltage conversion from the deep sub threshold regime up to the nominal supply voltage level. The traditional LS topology is the differential cascade voltage switch (DCVS) circuit, as show in Fig. 1 it includes a full-latch formed by four PMOS transistor (MP4 & MP5 and MP10 & MP11) and a pair of inverter controlled by the differential low voltage input signal A and AN.[4]
The DCVS-LS behaves as a rationed circuit As a consequence, pull-up network (PUN) and pull-down network (PDN) strengths has to be properly balanced to ensure correct functionality of the circuit. This is difficult to achieve in practice when input signals have sub-threshold voltage levels [2]. One obvious way to deal with this problem is to increase the

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strength of PDNs relative to PUNs. Some work demonstrated that PDN transistor need to be upsized by several order of magnitude in order to correctly overcome the strength of PUNs for converting from sub threshold to above threshold voltage level, which is often impractical.

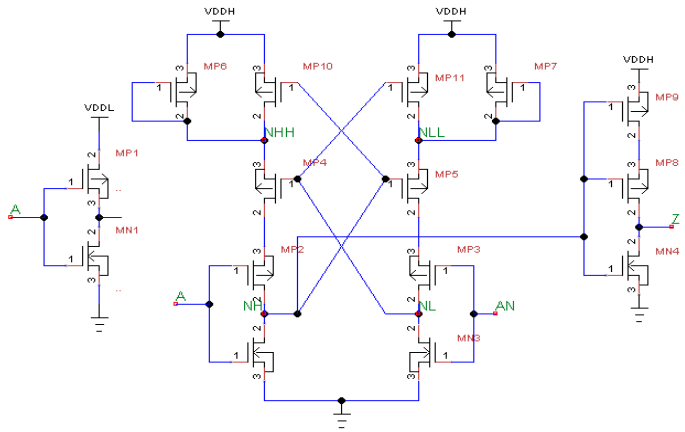

Fig. 1. Conventional DCVS level shifter

To solve this problem,Lütkemeier estimated that a NMOS-to-PMOS ratio of ~2400 is needed to design a fully functional DCVS-LS circuit which converts .2 V input signal into 1-V output signals, with 90-nm CMOS process technology [5].
In [7] , a low-power negative level shifter for low voltage applications is presented. Which is used to reduce the switching delay and leakage current. Furthermore, a pull-down driver is proposed to increase driving capability under various operation modes. The circuit was designed in 130nm CMOS technology with power supply of 1.5V. Simulation results show that the switching delay and power consumption is reduced by 62% and 65%, respectively.
Macro Lanuzza, in 2012, presented a level shifter which can up-convert from 180 mV to 1 V, this level shifter exhibits delay of 21.7ns and energy per transaction of 74 fJ, with an average power consumption 6.4 nW

III. PROPOSED WORK

The Proposed novel level shifter circuit design consists of an input inverter to provide differential low-voltage signals to the conversion stage, a modified DCVS-based conversion stage, which is responsible of the voltage shifting operation and an inverting buffer designed to assure adequate output driving strength. The key improvements in proposed level shifter with respect to the conventional DCVS-based structure are highlighted in Fig.2. Two p-MOS diode connected [4] (i.e. MP1 and MP2), are used to mitigate the current contention at the beginning of NH or NL discharging transition, acting as current limiters. The output buffer is driven in a split way [9] by NHH and NH nodes, whose voltage values differ from the voltage drop (VD) on MP1. This ensures that one of the devices (either the pull-up or the pull-down transistor) in the output inverter is completely turned OFF when the other turns ON. In this way, the short circuit current in the output buffer is significantly reduced with respect to the option used in, while the output switching speed is also improved. To further improve the charge and the discharge operations of the critical internal node, self-adapting PUNs able to dynamically adjust their strengths depending on the occurring output transition, were considered for the two branches of the conversion stage. For this purpose two pull-up boost circuits were introduced in parallel to the pull-up devices (i.e. MP3 and MP4) of the conventional DCVS structure. Although the multi-threshold CMOS technique can be exploited to emphasize the operating characteristics of the proposed LS, in our design, we used only regular threshold (RVT) devices to better evaluate advantages offered by the circuit topology without any interference from the Vth of the devices.

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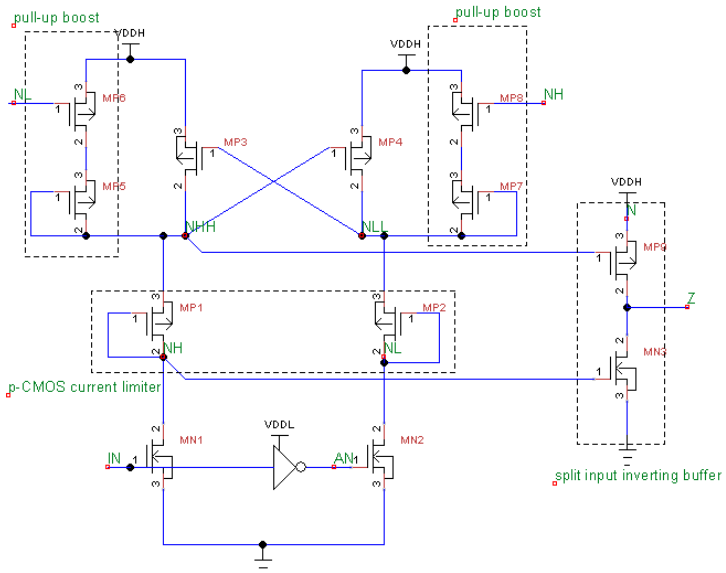

Fig. 2. Proposed level shifters

The schematic of proposed level shifter is designed on Cadence virtuoso UMC 180 nm technology process.

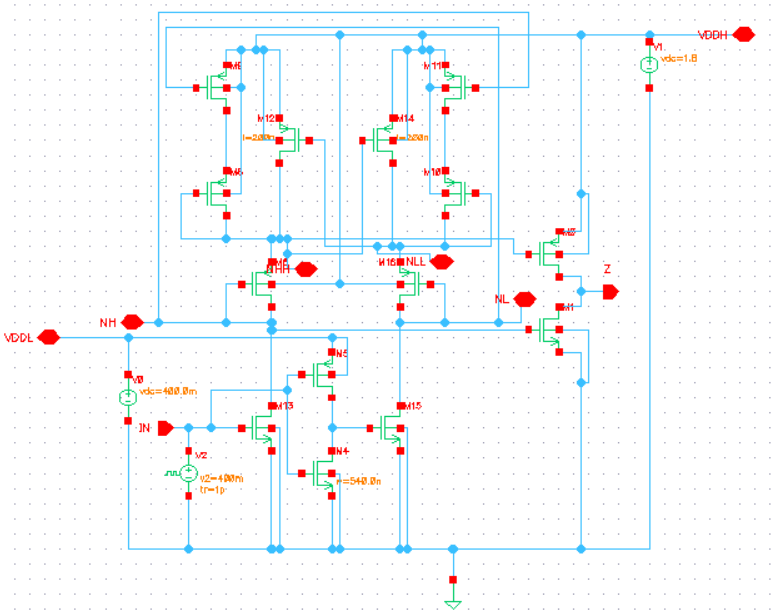

Fig. 3. Schematic circuit of proposed level shifter draws in Cadence

IV. SIMULATION RESULTS AND DISCUSSIONS

Fig. 4 shows the behavior of proposed Level shifter, When the input signal IN is low, the voltage on node NH is high (VDDH-VD,MP1) and the voltage on node NL is low (0V). A low-to-high (high-to-low) input signal A transition causes MN1 to be switched ON and, consequently the NH node starts to be discharged. This operation is in a first

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phase greatly favored by the current-limiting action of MP1 and by the presence of MP2 which forms a voltage divider to keep the node NLL at a voltage higher than GND. In this way, |VGS| of MP3 is reduced and the pull-up of the left branch is weakened to allow faster discharging of node NH. As NH discharges through MN1, e pull-up boost of right branch turns ON (i.e. the pull-up of the right branch is strengthened),

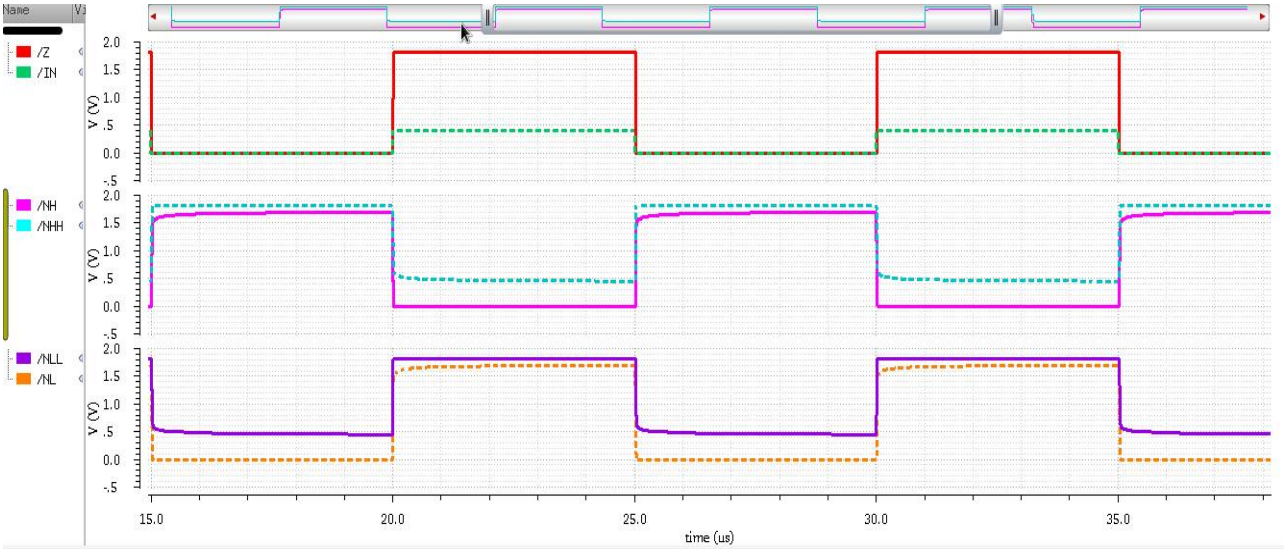

Fig. 4. Simulated transient behavior of the proposed level shifter

thus leading the NLL node to be fast charged towards the VDDH-VD,MP7 voltage. As a consequence, a positive feedback is triggered causing MP3 to be completely turned OFF and NH to be fully discharged. At the same time the pull-up boost of the right branch turns OFF (i.e. the MP7 diode becomes OFF) and NLL is raised to VDDH through MP4. In this way, the voltage levels of the internal nodes are established to assure fast switching and reduced energy consumption in the subsequent input transition (i.e. the pull-up of the right branch is now weakened due to the reduced |V GS| of MP4). The proposed LS was designed for the 180 nm UMC CMOS technology.

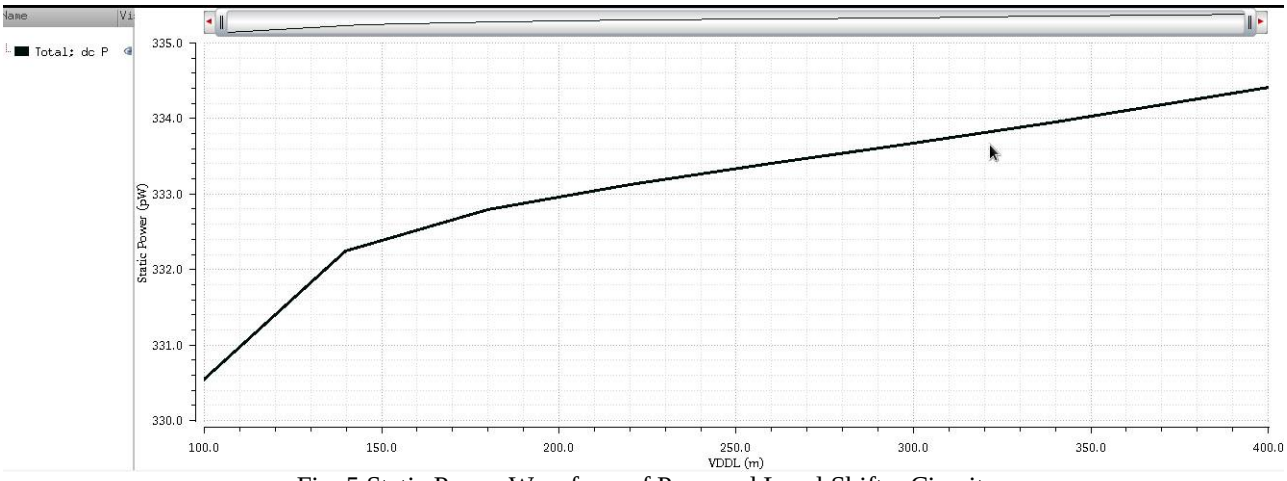

Fig. 5 Static Power Waveform of Proposed Level Shifter Circuit

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TABLE
COMPARATIVE RESULTS

Design	Tech.	Conversion rang	Delay (ns)	E_{tr} (fJ)	P_s (pW)
[10]	180 nm	.2V-1.8V	30(0.3V-1.8V)	350@100Khz	1920
[9]	180 nm	.19V-1.8V	21.6(.4V-1.8V)	390@100Khz	160
[8]	180 nm	.32V-1.8V	31(0.4V-1.8V)	680@1Mhz	1160
Conv. [4]	90nm	.1V-1V	16.6(.2V-1V)	77@1Mhz	870
This Work….	.18um	.1V-1.8V	12.5(.4V-1.8V)	51.2@10Khz	360

V. CONCLUSION

In this paper a low power energy efficiency level shifter is presented for multi supply voltage design. New circuit exploits proper design strategies to limit energy and static power consumption. The proposed design was design in the 180 nm UMC CMOS process technology. The results obtained show that the proposed level shifter can convert an input signal as low as 100 mV to 1.8 V, it exhibits average propagation delay of 12.5ns and energy per transition 51.2 fJ. This is obtained while the consuming a static power less than 360 pW.

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