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Implementation of 4-Tap Sequential and Parallel Micro-programmed Based Digital FIR Filter Architecture using VHDL

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ABSTRACT: The digital Finite Impulse Response (FIR) is widely used in many Digital Signal Processing (DSP) Systems, ranging from wireless communication to image and video processing. Basically, the digital FIR filter is consist of multiplier, adder delay element. In the realization of FIR filter, multiplier is an essential and complex building block. Several techniques have been reported in the open literature to implement digital FIR filter using Field Programmable Gate Array (FPGA).In this paper, the implementation of 4-tap sequential and parallel micro-programmed based digital FIR filter using VHDL is presented using 16 bit Wallace tree multiplier and Vedic multiplier. Performance evaluation is done based on the implementation results obtained through FPGA synthesis tools. Results clearly indicate that sequential filter achieves better performance in terms of speed and resource utilization as compared to parallel filter. Also Vedic multiplier is faster than Wallace multiplier. The coding is done in VHDL (Very High Speed Integrated Circuit Hardware Descriptive Language) and synthesized using Xilinx ISE version 13.4i.

KEYWORDS: Wallace Tree Multiplier, Vedic Multiplier, VHDL, FIR, FPGA.

I. INTRODUCTION

Digital signal processing (DSP) is one of the core technology used in communication system such as wireless sensor network (WSN) and Internet of Thing (IoT), requires fast processing of large amount of digital information. The digital filter is one of the most widely used building block of many digital signal processing (DSP) system. They are most commonly used in signal, image and video processing application. Digital filters are an important class of linear time invariant (LTI) system designed for filtering out undesirable parts from the signal, spectral shaping, motion estimation, noise reduction and channel equalization among many other applications. Digital filters are divided into two types, Finite Impulse Response (FIR) filter and Infinite Impulse Response (IIR) filter. The FIR filters are preferred over IIR filter for the operation in DSP includes filtering, convolution and inner product due to its linear phase response and inherent stability.

Adders, multipliers and delay elements are the key block used in the implementation of digital FIR filter. These blocks are arranged and interconnected in different ways based on the architecture of FIR filter. Basically, FIR filter performs a linear convolution on a window of N data samples which can be mathematically expressed as follows:

$$y(k) = \sum_{n=0}^{N-1} w(n).x(k-n)$$

The direct form implementation of an FIR filter can be readily developed from the convolution sum as shown in fig. 1.

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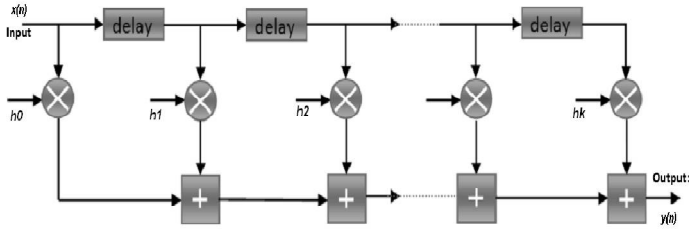

Fig. 1: Direct form FIR filter architecture

Direct form FIR filter are also known as tapped delay line or traversal filters. N-tap FIR filter consist of N delay elements, N multipliers, N-1 adders or accumulators. The impulse response of FIR filter can be directly inferred from the tap coefficient h_k. This paper presents the implementation of micro-programmed digital FIR filter using Wallace tree multiplier and Vedic multiplier. The performance of micro-programmed digital FIR filter is evaluated and compared using both Wallace tree and Vedic multiplier.

This paper is organized as follows; Section II describes proposed micro-programmed FIR filter. Section III describes Wallace tree multiplier. Section IV describes Vedic multiplier. Section V describes the implementation results and finally section VI describes the conclusion.

II. RELATED WORK

In [1], the author designs 64-tap linear phase filter operating at 1.4 MHz with 60dB attenuation at 0.28fs, 12dB attenuation at 0.25fs based on explicit multiplier and concluded that pipelined multiplier provides best trade-off between speed and resource requirement. In [2], the author implements digital-serial 5-tap FIR filter on a Xilinx XC4010 FPGA and concluded that digital-serial design with digit-size of 2 bit have about 17% smaller area-time product than those of bit-serial implementations. In [3], the author, introduces the design and simulation of FIR filter which is mainly based on FPGA, Quartus II ,Matlab and concluded that the use of these software significantly shortens the R& D period and it is able to greatly improve the speed of the filter by use of the pipelining structure. In [4], the author proposes a new hardware efficient reconfigurable FIR filter architecture based on binary signed sub-coefficient method and concluded that the FPGA synthesis results of the designed two filters based on 3-bit and 4-bit partitioning have been shown 33% and 27% reduction in the resource usage with respect to two state of art architecture. In [5], the author presents implementation of low power and low area digital Finite Impulse Response (FIR) filter The proposed FIR filter have been synthesized and implemented using Xilinx ISE V7.1 and Virtex IV FPGA. The author concluded that the minimum power achieved is 56mw in fir filter based on shift/add multiplier in 100MHz with 8-bit input and 8-bit coefficient.

III. MICRO-PROGRAMMED FIR FILTER

The micro-programmed FIR filter consists of data-path and micro-program control unit. The most important part of micro-program control unit is its flexibility to modify the micro-program in ROM based control memory. The micro-program controller consists of two main parts.

1. Addressing microinstruction kept in control memory.
2. Hold and generate microinstruction for data-path.

In this paper, two different architecture of digital FIR filter using micro-programmed controller is presented:

A. Sequential Architecture of Micro-programmed FIR Filter

The sequential architecture of 4-tap FIR filter is shown in Fig. 2. It is basically consist of the micro-programmed control unit and data path unit. The micro-program control unit consists of a micro-program counter and micro-program memory. The data path unit consist of two 4 x 16 bit FIFOs having inputs as data x[n] and coefficient h[n], a

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multiplier and an adder, a two input multiplexer to control the flow of data from multiplier or accumulator, one 32 bit accumulator and 32 bit register to latch the output data.

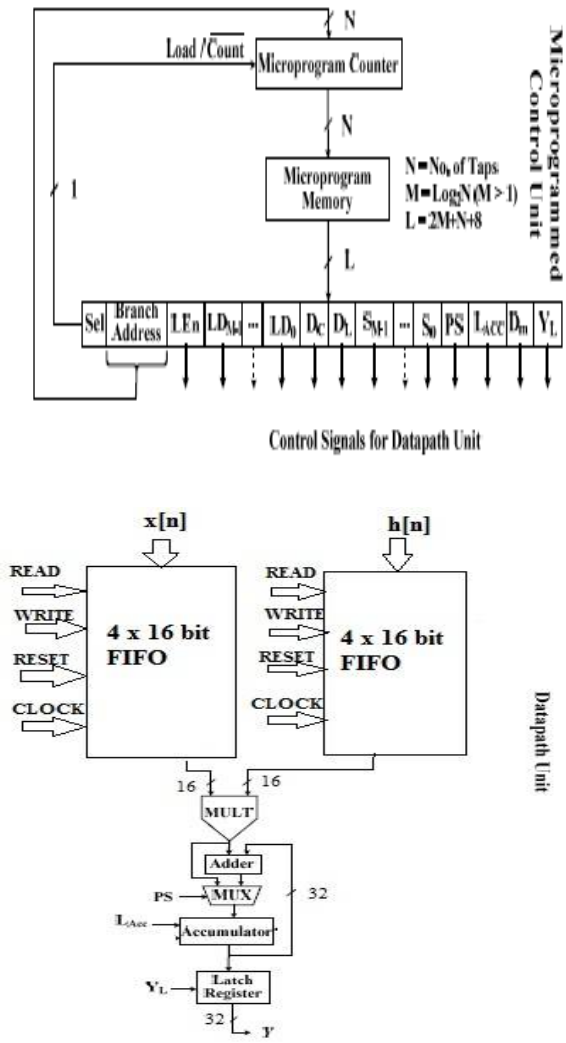

Fig. 2: Architecture of 4-tap sequential micro-programmed FIR filter

B. Parallel Architecture of Micro-programmed FIR Filter

The parallel architecture utilizes multiple adders and multipliers based on the size of it. In this paper, the 4-tap FIR filter is designed is consists of the following sub-modules:

- Four 16-bit data register
- One 2-to-4 decoder
- Four 16-bit coefficient register
- Four 16-bit multipliers
- Three 32-bit adders
- One 32-bit register for latching output

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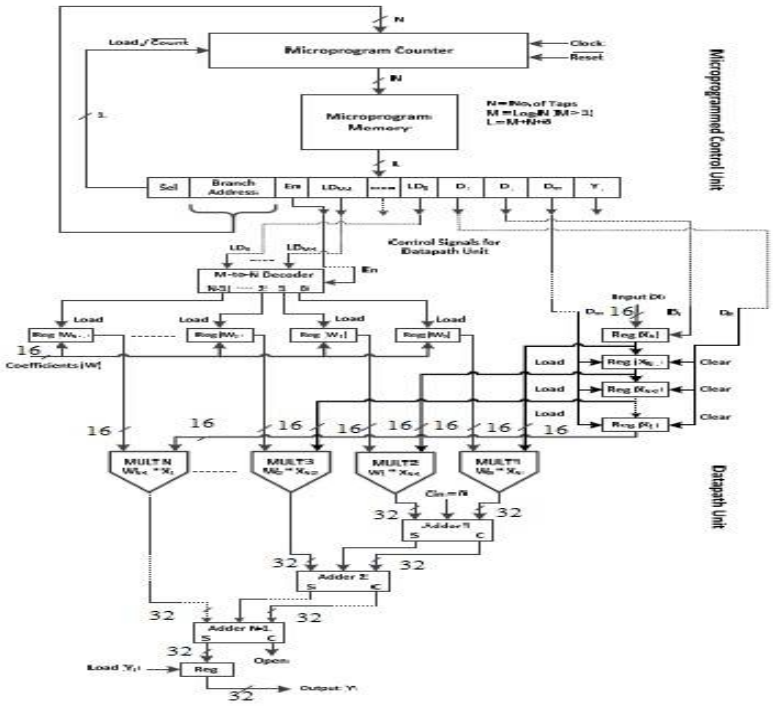

Fig. 3: Architecture of 4-tap parallel micro-programmed FIR filter

IV. WALLACE TREE MULTIPLIER

A Wallace tree multiplier is an efficient methodology, easily hardware implementable that multiplies two integers, proposed by an Australian Computer Scientist Chris Wallace. Using this method, a three step process is used to multiply two integer numbers. The first step is to multiply each bit of one of the arguments, by each bit of other, yielding n^2 result. The second step is to reduce the number of partial products to two by the layers of full adders and half adders. The third step is to group the wires in two numbers and add them with conventional adder. In this paper, two different architecture of Wallace tree multiplier are presented. First is designed using half adder and full adder, while second one uses the carry look ahead adder.

A. Wallace Tree Multiplier using Half adder and Full Adder

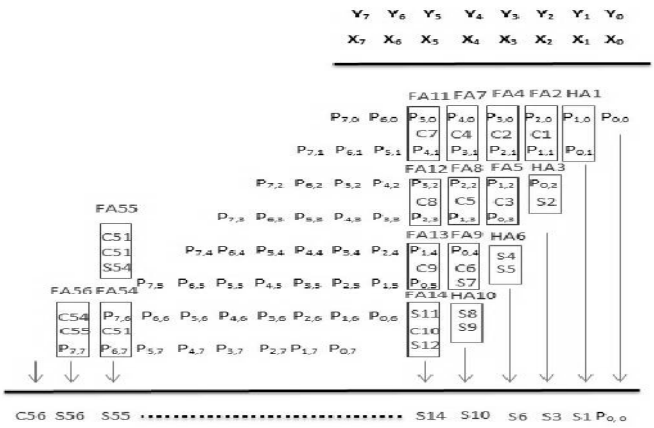

Fig. 4: Wallace Tree partial product addition using half and full adders.

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Wallace tree method is used to reduce the number of adder by minimizing the number of half adder in any multiplier. As shown in fig. above the first partial product is the least significant bit (LSB) in the output of multiplier result. Then moving towards the next column of partial product if there are any adders from the previous product, the full adder is used otherwise half adder is used. Fig. 4 shows how algorithm is implemented.

A. Wallace Tree Multiplier using Carry Look Ahead Adder (CLA)

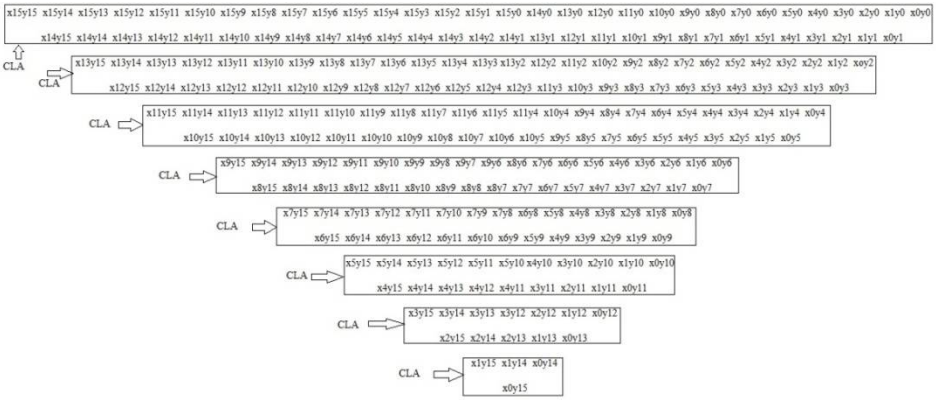

Fig. 5: 16 Bit Wallace Tree Multiplier using Carry Look Ahead (CLA) Adder

The Fig. 5 shows the implementation of 16 Bit Wallace tree multiplier using carry look ahead adder. The two 16-bit inputs are x15x14.....x2x1x0 and y15y14.....y2y1y0. Firstly, multiply each one input to all other 16 inputs and we get the AND operation results. Then arrange these results as shown in Fig. 5(in triangular form). Now, addition of these AND operation results is performed using CLA. The output of this adder is the final output of multiplier which is denoted as P31P30.....P2P1P0.

V. VEDIC MULTIPLIER

Vedic mathematics is an ancient form of mathematics which was developed in India by Sri Bharti Krishna Tirthaji between 1911 and 1918. Vedic mathematics is based on 16 sutras or algorithm. The Urdhava Tiryakbhagyam Sutra (Vertically and Crosswise Algorithm) is one of them used for multiplication. The Urdhava Tiryakbhagyam Sutra is used for efficient digital multiplication. The multiplier based on this algorithm has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multiplier. The proposed Vedic multiplier is designed using Urdhava Tiryakbhagyam Sutra (Vertically and Crosswise Algorithm).In this algorithm, the partial product and their sum are calculated in parallel and because of this the multiplier is independent of clock frequency of the processor. The proposed 16 bit Vedic multiplier design is shown in fig. 6 as given below:

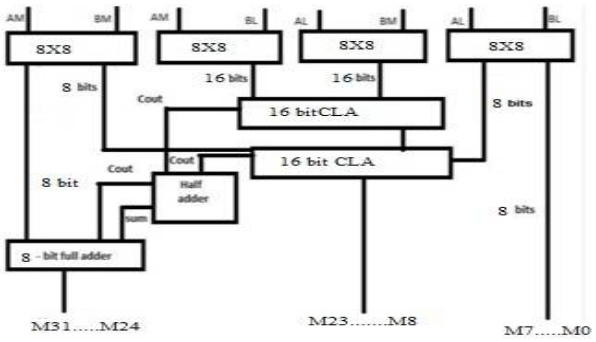

Fig. 6: Block Diagram of 16x16 Vedic Multiplier

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The Fig.6 consist of four 8 bit Vedic multiplier, two 16 bit carry look ahead adder (CLA), one 8 bit carry look ahead adder (CLA) and one half adder for designing of 16-bit Vedic multiplier.

VI. RESULT

The proposed 4-tap micro-programmed sequential and parallel FIR filter is implemented using VHDL. The synthesis is done using Xilinx Synthesis Tool (XST) available with Xilinx ISE 13.4i simulator. Table I and Table II given below indicates the total path delay occur while designing these micro-programmed FIR filters.

Table I: Comparison of Synthesis Result of Proposed 4-tap micro-programmed sequential FIR filter using 16 bit Wallace Tree and Vedic Multiplier

	4-tap micro-programmed sequential FIR filter (Using 16 bit Wallace tree multiplier)	**4-tap micro-programmed sequential FIR filter (Using 16 bit Vedic multiplier)**
Delay (ns)	15.56	10.56
No. of Slices	758 out of 28800(2%)	892 out of 28800(3%)

Table II: Comparison of Synthesis Result of Proposed 4-tap micro-programmed parallel FIR filter using 16 bit Wallace Tree and Vedic Multiplier

	4-tap micro-programmed parallel FIR filter (Using 16 bit Wallace tree multiplier)	**4-tap micro-programmed parallel FIR filter (Using 16 bit Vedic multiplier)**
Delay (ns)	19.51	14.28
No. of Slices	2687 out of 28800(9%)	3309 out of 28800(11%)

The Table I and II shows that the utilization of 4-tap micro-programmed sequential FIR filter is less (which are 2% and 3%) than the utilization of 4-tap micro-programmed parallel FIR filter (which are 9% and 11%). The path delay of 4-tap micro-programmed sequential FIR filter using 16- bit Wallace tree multiplier and 16- bit Vedic multiplier is 15.56ns and 10.56ns. The path delay of 4-tap micro-programmed parallel FIR filter using 16- bit Wallace tree multiplier and 16- bit Vedic multiplier is 19.51ns and 14.28ns.

Fig. 7, Fig. 8, Fig. 9, Fig. 10 indicates the simulation results of 4-tap micro-programmed sequential and parallel FIR filter using 16- bit Wallace tree multiplier and 16- bit Vedic multiplier.

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Fig. 7: Simulation Result of 4-tap micro-programmed sequential FIR filter using 16- bit Wallace tree multiplier

Fig. 8: Simulation Result of 4-tap micro-programmed sequential FIR filter using 16- bit Vedic multiplier

Fig. 9: Simulation Result of 4-tap micro-programmed parallel FIR filter using 16- bit Wallace tree multiplier

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Fig. 10: Simulation Result of 4-tap micro-programmed parallel FIR filter using 16- bit Vedic multiplier

VII. CONCLUSION

In this paper, the 4-tap micro-programmed sequential and parallel FIR filter using 16- bit Wallace tree multiplier and 16- bit Vedic multiplier is implemented. The comparison of synthesis result shows that the path delay of the 4-tap micro-programmed sequential and parallel FIR filter using 16- bit Vedic multiplier is less than that of the path delay of the 4-tap micro-programmed sequential and parallel FIR filter using 16- bit Wallace tree multiplier. Results clearly indicate that sequential filter achieves better performance in terms of speed and resource utilization as compared to parallel filter.

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BIOGRAPHY

Miss. Tamli D. Sawarkar is presently pursuing final semester M. Tech in Electronics at Rajiv Gandhi College of Engineering and Research, Nagpur. She received degree B.E. in Electronics and Telecommunication from SRMCEW, Nagpur. Her areas of interest are VLSI and VHDL.