ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 10, October 2016

Review Paper on 8-bit Discrete Cosine Transform using Common Boolean Logic Adder

Manendra Zarbade, Anshuj Jain

M. Tech Scholar, SCOPE College of Engineering, Bhopal, India

Assistant Professor, SCOPE College of Engineering, Bhopal, India

ABSTRACT: Low-power design is one of the most important challenges to maximize battery life in portable devices and to save the energy during system operation. Discrete Cosine Transform (DCT) is widely used in image and video compression standards. In this paper, we review on a low-power DCT (Discrete Cosine Transform) architecture using various techniques. Discrete Cosine Transform (DCT) is one of the most popular lossy techniques used today in video compression schemes. Several algorithms have been proposed to implement the DCT. Loeffler (1989) has given a new class of 1D-DCT using just 11 multiplications and 29 additions. To implement such an algorithm, one or more multipliers have to be integrated. This requires a high silicon occupation area. Arithmetic distribution is widely used for such algorithms. The coding for reconfigurable 8 point DCT has been done using VHDL under Xilinx platform.

KEYWORDS: Discrete Cosine Transform (DCT), Inverse discrete Cosine Transform (IDCT), VHDL

I. INTRODUCTION

With the advent of high resolution images and high definition videos, they are very popular and can be easily found in daily use by several people. Relying on quality data for processing led to the development of the multimedia products such as Mobile phone video capture, Wireless camera, Sensor Networks etc. The increase in crime and elevated Terrorist threats has also been a reason for the increase in video surveillance system. More often than not, these applications and/or devices require storing and/or transmitting of the recorded media. Compression becomes important in such cases, where the video is need to be of minimal space possible but not degrading the visual quality too much. Due to the scarcity of storage space and computational capabilities in the handheld and monitoring devices, we need an algorithm with good compression rate. For some applications/devices it is imperative that they consume low power at both the ends of the codec, as in mobile phone camera. Modern digital video coding schemes are governed by the ITU-T (International Telecommunication Unit-Telecommunication) and ISO/IEC MPEG (Moving Picture Experts Group) (2) standards, which relies on combination of transformations, block-based, and interface prediction to exploit spatial and temporal correlations within encoded video. This results in high complexity encoders because of the motion estimation (ME) process run at the encoder side. On the other hand, the resulting decoders are simple and around 5 to 10 times less complex than the corresponding encoders. However these types of architecture are more suited for the applications where the media is once encoded and might be decoded multiple times. Few such areas include on-demand-video, broadcasting etc. It presents a challenge for the traditional video coding paradigms to fulfill the requirements posed by these applications. So, there is a need for the low cost and power encoding device possibly at the expense of slightly complex decoder. Additional challenge arises while trying to achieve the efficiency as of those achieved by the traditional coding techniques, like those of MPEG-x or H.26x when the complexity shifts from encoder to decoder.

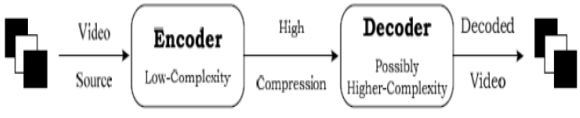

Figure 1: Ideal coding architecture for upcoming video applications

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2016

Distributed source coding (DSC) mainly depends on the principle of independent encoding and joint decoding. 'Distributed' in DSC points to the distributed nature of encoding operation, not the location as in distributed computing. DSC regards the compression of correlated information resources that do not communicate with each other (1). DSC models the correlation between multiple sources together with channel code and hence able to shift complexity from encoder to decoder. Hence DSC, DVC in current context, can be used to develop the devices having complexity-constrained encoder.

II. LITERATURE REVIEW

Mamatha I et al. [1], discrete Fourier Transform is generally utilized as a part of sign preparing for unearthly investigation, sifting, picture upgrade, OFDM and so forth. Cyclic convolution based methodology is one of the strategies utilized for registering DFT. Utilizing this approach a N point DFT can be registered utilizing four sets of [(M-1)/2]-point cyclic convolution where M is an odd number and N=4M. This work proposes a design for convolution based DFT and its FPGA usage. Proposed design includes a pre-preparing component, systolic exhibit and a post handling stage. Handling component of systolic cluster utilizes a label bit to choose the kind of operation (expansion/subtraction) on the info signals. Proposed engineering is reproduced for 28 point DFT utilizing ModelSim 6.5 and blended utilizing Xilinx ISE10.1 utilizing Vertex 5 xc5vfx100t-3ff1738 FPGA as the objective gadget and can work at a greatest recurrence of 224.9MHz. The execution examination is done regarding equipment use and calculation time and contrasted and existing comparable models. Further, as the convolution based DCT has two systolic clusters like that of DFT , a bound together engineering is proposed for 1D DFT/1D DCT.

Mansi Mane et al. [2], CORDIC or CO-ordinate Rotation Digital Computer is a quick, straightforward, intelligible and capable calculation which is utilized for enhanced Digital Signal Processing applications. In compatibility of velocity and exactness prerequisites of today's applications, we set forward variable emphasess CORDIC calculation. In this calculation, to support speed we can diminish number of emphasess in CORDIC calculation for particular exactness. This upgrades proficiency of customary CORDIC calculation which we have used to figure Discrete Cosine Transform for picture preparing. One Dimensional Discrete Cosine Transform is executed by utilizing just 6 CORDIC squares which needs just 6 multipliers. Due to the straightforwardness in equipment rate of picture handling on FPGA is raised. Further increment in velocity can be accomplished by simultaneously preparing number of large scale pieces of a picture on FPGA.

Hyeonuk Jeong et al. [3], Low-control design is a champion amongst the most basic challenges to help battery life in adaptable contraptions and to save the essentialness in the midst of system operation. In this paper, we propose a low-control DCT (Discrete Cosine Transform) auxiliary arranging using a balanced multiplier-less CORDIC (Coordinate Rotation Digital Computer) number juggling.

The trading power use is decreased in the midst of DCT: the proposed fabricating plan does not perform math operations of pointless bits in the midst of the CORDIC figurings. The test outcomes exhibit that we can diminish up to 26.1% power spread without deal of the last DCT results. Furthermore, the pace of the proposed basic arranging is extended around 10%. The proposed low-control DCT auxiliary designing can be associated with client contraptions and flexible sight and sound structures requiring high throughput and low-control.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2016

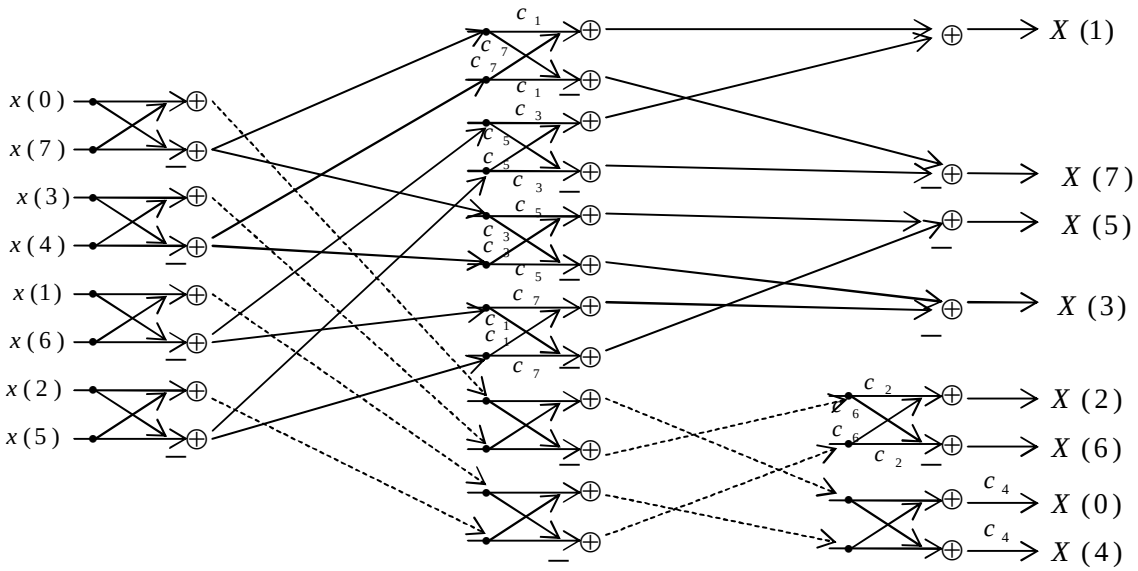

Figure 2: 8-point Discrete Cosine Transform

Esakkirajan G et al. [4], CORDIC or CO-ordinate Rotation Digital Computer is a quick, basic, proficient and intense calculation utilized as a part of Digital Signal Processing applications. In this paper, we develop the approach for planning a low-control territory productive DCT for picture pressure utilizing just move registers, and adders! Sub tractors and exceptional interconnections. Through equipment combination we demonstrated that movement and include based DCT calculation is productive one over routine multiplier based methodology lastly exactness was measured by contrasting PSNR estimation of reproduced picture and unique picture utilizing MATLAB.
E. Jebamalar Leavline et al. [5], Discrete Cosine Transform (DCT) is widely used in image and video compression standards. This paper presents low-power co-ordinate rotation digital computer (CORDIC) based reconfigurable architecture for discrete cosine transform (DCT).

III. DISCRETE COSINE TRANSFORM

A discrete cosine transform (DCT) expresses a finite sequence of data points in terms of a sum of cosine functions oscillating at different frequencies. DCTs are important to numerous applications in science and engineering, from lossy compression of audio (e.g. MP3) and images (e.g. JPEG) (where small high-frequency components can be discarded) , to spectral methods for the numerical solution of partial differential equations. The use of cosine rather than sine function is critical for compression, since it turns out (as described below) that fewer cosine functions are needed to approximate a typical signal, whereas for differential equations the cosines express a particular choice of boundary conditions.

DCT output

$$F(0) = 0.5(f(0) + f(1) + f(2) + f(3) + f(4) + f(5) + f(6) + f(7))\cos\frac{\pi}{4}$$

$$F(1) = 0.5[\{(f(0) - f(7)\}\cos\frac{\pi}{16} + \{f(1) - f(6)\}\cos\frac{3\pi}{16} + \{f(2) -$$

$$f(5)\}\cos\frac{5\pi}{16} + \{f(3) + f(4)\}\cos\frac{7\pi}{16}]$$

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2016

$$F(2) = 0.5[\{(f(0) - f(3) - f(4) + f(7)\}\cos\frac{2\pi}{16} + \{f(1) - f(2) - f(5) + f(6)\}\cos\frac{6\pi}{16}]$$

$$F(3) = 0.5[\{(f(0) - f(7)\}\cos\frac{3\pi}{16} + \{f(6) - f(1)\}\cos\frac{7\pi}{16} + \{f(5) - f(2)\}\cos\frac{\pi}{16} + \{f(4) + f(3)\}\cos\frac{5\pi}{16}]$$

$$F(4) = 0.5[(f(0) + f(3) + f(4) + f(7) - f(1) - f(2) - f(5) - f(6))\cos\frac{\pi}{4}]$$

$$F(5) = 0.5[\{(f(0) - f(7)\}\cos\frac{5\pi}{16} + \{f(6) - f(1)\}\cos\frac{\pi}{16} + \{f(2) - f(5)\}\cos\frac{7\pi}{16} + \{f(3) + f(4)\}\cos\frac{3\pi}{16}]$$

$$F(6) = 0.5[\{(f(0) - f(3) - f(4) + f(7)\}\cos\frac{6\pi}{16} - \{f(1) - f(2) - f(5) + f(6)\}\cos\frac{2\pi}{16}]$$

$$F(7) = 0.5[\{(f(0) - f(7)\}\cos\frac{7\pi}{16} + \{f(6) - f(1)\}\cos\frac{5\pi}{16} + \{f(2) - f(5)\}\cos\frac{3\pi}{16} + \{f(4) + f(3)\}\cos\frac{\pi}{16}]$$

IV. COMMON BOOLEAN LOGIC

Zone and power proficient fast information rationale way are the most critical zones of exploration. With the assistance of straightforward alteration in entryway level we can accomplish the change in the outcomes. Pace of the snake relies on upon the time required to engender the help through the viper. These snake works in arrangement organize, that is the entirety of the rudimentary position bit is figured when the past bits are summed and the convey is spread to that next stage.

Convey select viper (CSLA) is one of the propelled adders utilized as a part of information preparing processors to perform quick number juggling capacity. It concentrates on the issue of convey engendering delay by creating the convey freely at every stage and the select the effective one with the assistance of multiplexer to play out the total. The ordinary CLSA is RCA (Ripple convey snake) which create the fractional whole and convey by utilizing the information convey condition Cin=0 and Cin=1, select one out of every pair to frame last total and last convey yield.

RCA is not zone proficient as huge number of doors hardware is utilized to frame the halfway items and afterward the last whole and convey is chosen.

Another type of CLSA viper utilizes paired to overabundance 1 convertor supplanting swell convey snake with Cin=1. This viper is known as CLSA alongside BEC. The quantity of entryways utilized has been decreased when we need to outline huge piece viper. This adders is more traditional as contrast with RCA when manage silicon territory utilized yet this is having possibly higher deferral time.

The proposed Common Boolean Logic (CBL) snake is region power-delay productive. It chip away at the rationale to expel the repetitive adders and use Common Boolean Logic as contrast with traditional convey select viper.

The CBL square is contained two sections entirety era piece and convey era square. In whole era obstruct the yield total is accomplished utilizing the multiplex. This multiplex is utilized to choose the yield esteem depeding on the estimation of Cin(past piece).If Cin=0, then output is xor of the two input bits. If Cin=1, then output get inverted. In carry

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2016

generation block, multiplexer is used to select the carry of next stage depending upon the previous carry input. If Cin=0, cout is OR of two input and if Cin=1 the output carry is AND of the input bit.

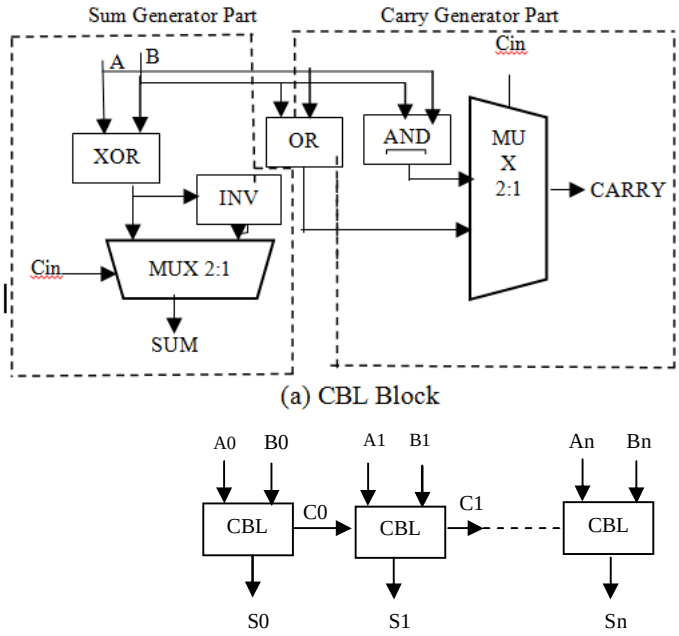

Figure 3: Block Diagram of n-bit CBL

$$If\ C_{in} = 0$$
$$Sum = A\ XOR\ B$$
$$Carry\ A OR\ B$$
$$else$$
$$Sum = NOT\ (A\ XOR\ B)$$
$$Carry = A\ AND\ B$$

This same process is used for the n number of bits and thus we get the final sum and carry as output.

V. CONCLUSION

In literature survey we found that CBL adder based DCT algorithm is the best algorithm in the existing algorithm. So we are implementation to CBL based DCT algorithm in this paper. The performance evaluation of the various sub modules are carried out using Xilinx 14.1 ISE Simulator and it was found that the circuits designed using DCT logic showed a reduced delay and power. As a future work more arithmetic and logical function can be used.

REFERENCES

[1] Mamatha I, Nikhita Raj J, Shikha Tripathi, Sudarshan TSB, "Systolic Architecture Implementation of 1D DFT and 1D DCT", 978-1-4799-1823-2/15/$31.00 ©2015 IEEE.
[2] J. E. Volder, "The CORDIC trigonometric computing technique," IRE Trans. Electron. Comput. Vol. EC-8, no.3, pp.335-339, Sept. 1959.
[3] Liyi Xiao Member, IEEE and Hai Huang, "Novel CORDIC Based Unified Architecture for DCT and IDCT", 2012 International Conference on Optoelectronics and Microelectronics (ICOM) 978-1-4673-2639-1/12/$31.00 ©2012 IEEE.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 7, July 2016

[4] Shymna Nizar N.S,Abhila and R Krishna, "An Efficient Folded Pipelined Architecture For Fast Fourier Transform Using Cordie Algorithm", 2014 IEEE International Conference on Advanced Communication Control and Computing Technologies (lCACCCT) IEEE.
[5] E. Jebamalar Leavline, S.Megala2 and D.Asir Antony Gnana Singh, "CORDIC Iterations Based Architecture for Low Power and High Quality DCT", 2014 International Conference on Recent Trends in Information Technology 978-1-4799-4989-2/14/$31.00 © 2014 IEEE.
[6] Hyeonuk Jeong *et al*, "Low-Power Multiplierless" DCT Architecture Using Image Data Correlation;" IEEE Transactions on Consumer Electronics, Vol. 50, No. 1, FEBRUARY 2004.
[7] Syed Ali khayam, "The Discrete cosine transform(DCT) Theory and Application" Department of Electrical and Computer Engineering Michigan state University, March10th 2003.
[8] Satyasen Panda, "Performance Analysis and Design of a Discreet Cosine Transform processor Using CORDIC algorithm", 2008-2010.
[9] Befrooz parhami, "Computer Airthmatic Algorithms and Hardware design", published by Oxford university press lnc. 198, Madison Avenue, New Yark , 2000.
[10] Keshab K. Parhi, "VLSI Digital Signal Processing Systems, design and implementation", Wiley.
[11] J.SriKrishna, "DESIGN OF 2D DISCRETE COSINE TRANSFORM USING CORDIC ARCHITECTURES IN VHDL" Department of Electronics and Communication Engineering National Institute of Technology, Rourkela May, 2007.
[12] Deepika Ghai, "COMPAATIVE ANALYSIS OF VARIOUS CORDIC TECHNIQUES", June, 2011.
[13] Yuan-Ho Chen *et al*, "A High Performance Video Transform Engine by Using Space- Time Scheduling Strategy", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 4, APRIL 2012.