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## An Efficient Implementation of Area Reduced S-MB Fused Add-Multiply Operator

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**ABSTRACT:** Electronic circuits comprises of complex arithmetic units, one such field is DSP applications. Multiplier is the base of any arithmetic circuits. A system performance is generally determined by the performance of the multiplier. Recent research activities in the field of arithmetic optimization combining operation which share data lead to significant performance improvement. The proposed optimized design of Add Multiply operator is based on the fusion of the adder and MB encoding unit into a single datapath block. For the design of Fused Add Multiply (FAM) unit different recoding techniques are introduced(SMB1,SMB2,SMB3) for the odd and even bit width of input. These techniques are used to implement direct recoding of sum of two numbers in the Modified Booth Form. Modified Booth Form are mainly used in multiplier, it reduce the number of partial products into half. By comparing the proposed recoding techniques with existing one , the proposed system yields considerable reduction in terms of area . The proposed FAM unit is coded in Verilog, simulated and synthesized using Xilinx tool.

**KEYWORDS:** Modified Booth Recoding ,Adder, Multiplier.

### I.INTRODUCTION

Multiplier are the basic elements of an arithmetic unit. One such field is digital signal processing application such as fast fourier transform, filtering , convolution etc. Thus multiplier optimization in terms of area and speed is a major concern for digital designs. A system performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in all system and also it is occupying more area consuming. Recent research activities in the field of arithmetic optimization shown that the design of arithmetic components combining operation which share data lead to significant performance improvement [1],[2],[3]. Based on the observation Multiply- Accumulator (MAC) [4-6] and Multiply- Add (MAD) units were introduced. Except the MAC/MAD operations, many DSP applications are based on Add- Multiply (AM) operations. The straight forward architecture of AM unit by first allocating an adder then driving its output to the input of a multiplier. An optimized design of the AM operator is based on the fusion of the adder and the Modified Booth encoding unit into a single data path block. The FAM component contain only one adder. As a result significant area saving is observed and the critical path delay of the recoding process is reduced. To optimize the design of AM operator, the direct recoding of the sum of two numbers in its Modified Booth (MB) form are introduced [7],[8],[9],[10]. The direct recoding of the sum of two numbers in its MB form gives an efficient implementation of the fused Add Multiply operator.

### II.RELATED WORK

Recent studies shows that the design of arithmetic components combining operations which share data, can lead to the better performance improvement. Based on the results that an addition can often be subsequent to a multiplication, which is used in the Multiply-Accumulator (MAC) and Multiply-Add (MAD) units were leading to the more efficient implementations of DSP algorithms compared to the conventional ones, which use only primitive resources. Several architectures have been introduced to optimize the performance of the MAC operation in terms of area occupation, critical path delay or power consumption. The MAC components increase the flexibility of DSP data path synthesis, as a large set of arithmetic operations can be efficiently mapped onto them. Apart from the MAC/MAD operations, many DSP applications are based on Add-Multiply (AM) operations. The simplest design of the AM unit, by first allocating

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an adder and then driving its output to the input of a multiplier, increases significantly both area and critical path delay of the circuit.

### III. FUSED ADD MULTIPLY OPERATOR

An optimized design of an Add Multiply operator is based on the fusion of the adder and the MB encoding unit into a single data path block, by direct recoding of the sum to its MB representation. The direct recoding of the sum of two numbers in its MB form leads to more efficient implementation of the Fused Add Multiply (FAM) Unit compared to the conventional one. In this work, we present three new technique for direct recoding of sum of two numbers in the MB representation.

1. SMB 1
2. SMB 2
3. SMB 3

Fig 1.represents the fused design of AM operator

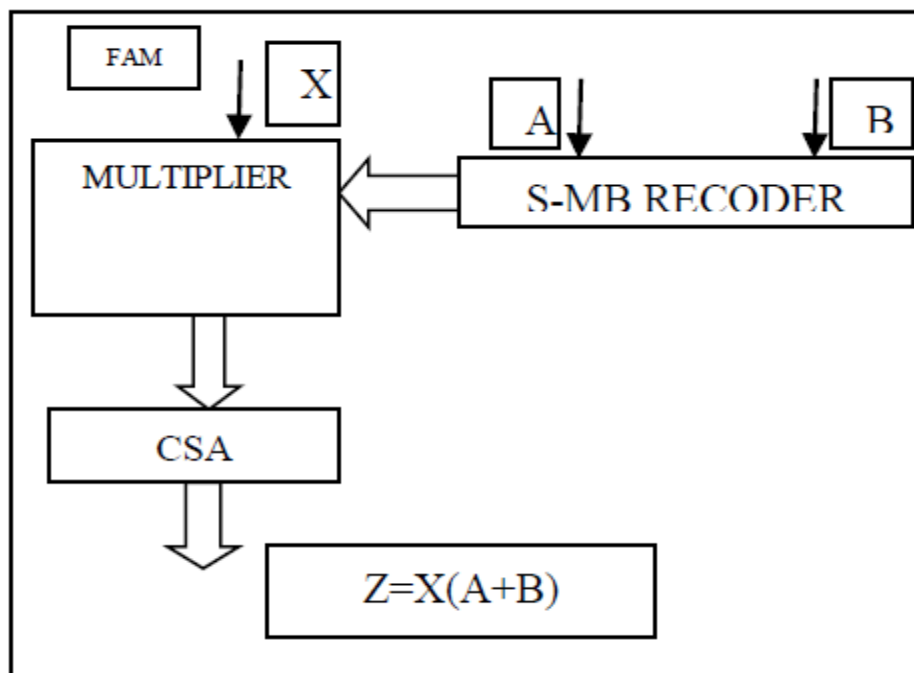


Fig 1:Fused Add Multiply Operator

In conventional design of the AM operator requires that its input A & B are first driven into an adder then the input X and sum Y is driven to a multiplier to get the output. The drawback of using an adder is that it inserts significant increase in both area & critical path delay of the circuit. The conventional design of AM operator is shown in fig 2.

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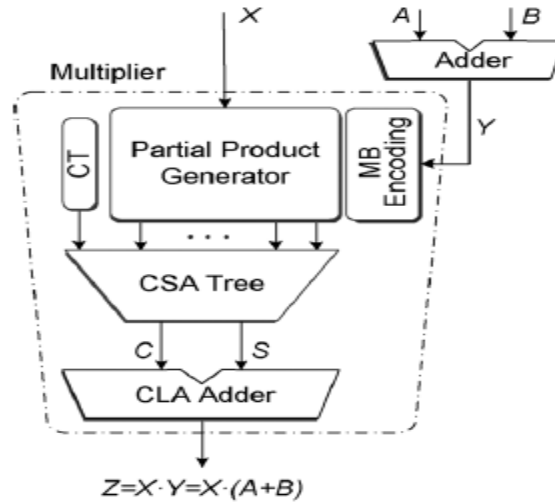


Fig 2: Conventional Design

### III. MODIFIED BOOTH RECODER

Modified Booth (MB) is a prevalent form used in multiplication. It is a redundant signed digit radix-4 encoding technique. Its main advantage is that it reduces the number of partial products by half in multiplication comparing to radix-2 representation.

Let us consider the multiplication of two numbers X & Y with each number consisting of n=2K bits. The multiplicand Y can be represented in MB form as:

$$Y_j^{MB} = 2Y_{2j+1} + Y_{2j} + Y_{2j-1} \quad (1)$$

Digits  $Y_j^{MB} \in \{-2, -1, 0, +1, +2\}$ ,  $0 \leq j \leq k-1$ , correspond to the three consecutive bits  $Y_{2j+1}$ ,  $Y_{2j}$  &  $Y_{2j-1}$  with one bit overlapped and considering that  $Y_{-1}=0$ . Table 1 shows the Modified Booth encoding table. Each digit is represented by three bits named S, ONE, TWO. The sign bit S shows if the digit is negative (S=1) or positive (S=0). Signal ONE shows if the absolute value of a digit is equal to 1 (ONE=1) or not (ONE=0). Signal TWO shows if the absolute value of a digit is equal to 2 (TWO = 1) or not (TWO = 0). Using these three bits we calculate the MB digits  $Y_j^{MB}$  by the following relation:

$$Y_j^{MB} = (-1)^{s_j} [one_j + two_j] \quad (2)$$

TABLE 1 Modified Booth Encoding Table

Binary			$y_j^{MB}$	MB Encoding			Input Carry $c_{m,j}$
$y_{2j+1}$	$y_{2j}$	$y_{2j-1}$		sign= $s_j$	$\times 1=one_j$	$\times 2=two_j$	
0	0	0	0	0	0	0	0
0	0	1	+1	0	1	0	0
0	1	0	+1	0	1	0	0
0	1	1	+2	0	0	1	0
1	0	0	-2	1	0	1	1
1	0	1	-1	1	1	0	1
1	1	0	-1	1	1	0	1
1	1	1	0	1	0	0	0

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## IV. FAM IMPLEMENTATION

The proposed system fuses the adder unit with multiplier to implement  $Z= X(A+B)$  operation which uses the MB encoding technique [11],[12],[13]. Where A and B are the inputs of the adder, whose output Y is driven as an input to the multiplier along with another input X as shown in fig 1.

In optimized AM operator design the adder unit is fused with MB encoding unit to form a single datapath unit. Three new techniques has been introduced to implement this FAM unit. In all techniques separate designs are implemented for an even and odd number of input bits. Three techniques are-

### A) SMB1 Technique:

This technique uses two full adders to implement the design for odd and even width of bits stream. For the even number of bits two FAs are used as FA , a conventional full adder and FA\* whose output value is given as:

$$FA^* = -2c_0 + s = p - q + c_i$$

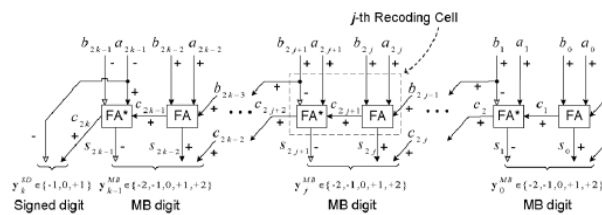


Fig 3: SMB1 Technique For Even Bit Width

For odd bit-width an additional FA\*\* is used at the end whose output value is

$$FA^{**} = -2c_0 + s = -p - q + c_i$$

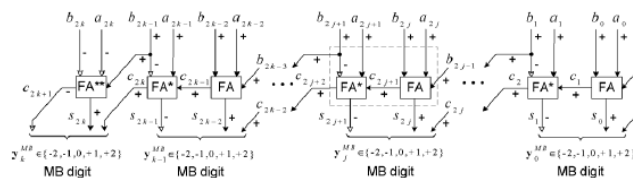


Fig 4: SMB1 Technique For Odd Bit Width

### B) SMB2 Technique:

In this technique , for even bit-width a conventional full adder along with two half adders with the output value

$$HA^* = -2c + s = -p - q$$

are used whereas for odd width of bits an additional fulladder as FA\*\* has been used at the end.

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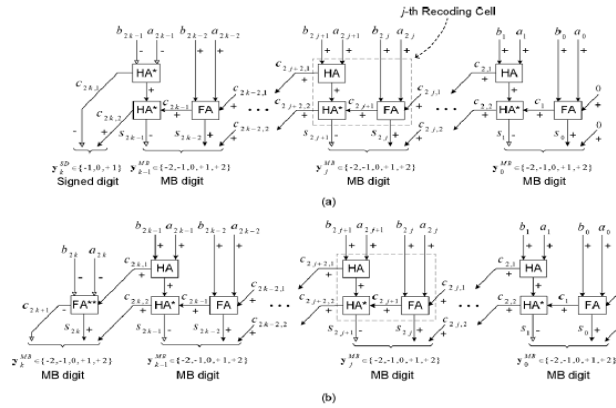


Fig5:SMB2 Technique for (a)Even (b)Odd Number Of Bits

### C) SMB3 Technique:

Here in this proposed scheme for even bit-width of input numbers a conventional full adder along with three different half adders has been used where the half adders are conventional HA, HA\* and HA\*\*. HA\*\* output value is

$$HA^{**} = 2c - s = -p + q.$$

The odd bit-width input uses a conventional FA, HA and HA\* along with and additional FA\*\* at the end of the recoding scheme.

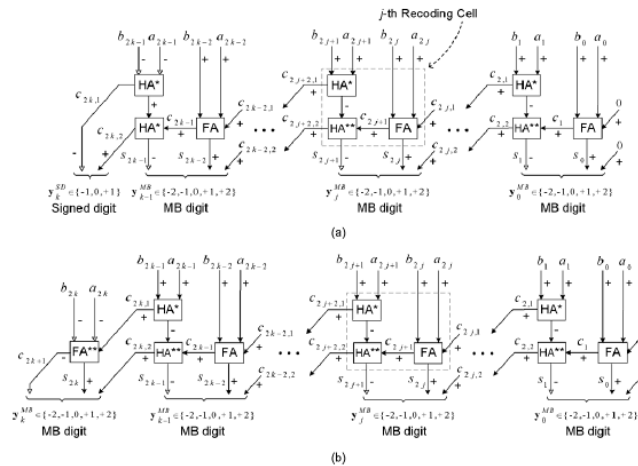


Fig 6: SMB3 Technique For (a)Even (b)Odd Number Of Bits

The output of the Sum-MB recoder, is the direct recoding of sum of two numbers in its MB representation. By using this gate level circuit (fig 7) MB encoding signals are generated that is,  $S_j, ONE_j, TWO_j$ . Then the Booth decoder generates the partial products using the encoded signal and other input X. The partial product reduction is carried out by using Wallace Tree algorithm. It is structured by using halfadders, fulladders and exact compressors. The Wallace Tree computes the last two rows by adding the generated partial products. The last two rows are added to generate the final multiplication results, using the ripple carry addition.

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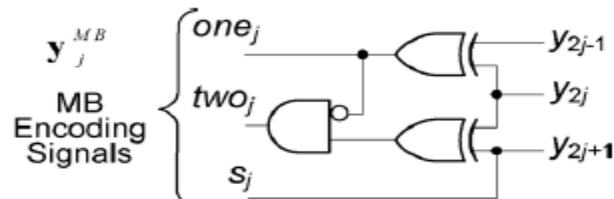


Fig7:Gate Level Implementation For MB Encoding Signals

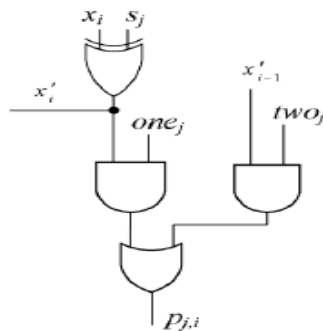


Fig8: Booth Decoders

## Exact Compressor:

A 4-2 compressor consists of five inputs and three outputs. It is called compressor, since it compress four partial products into two. This can be implemented with two stages of full adders (FA) connected in series as shown in Fig.9

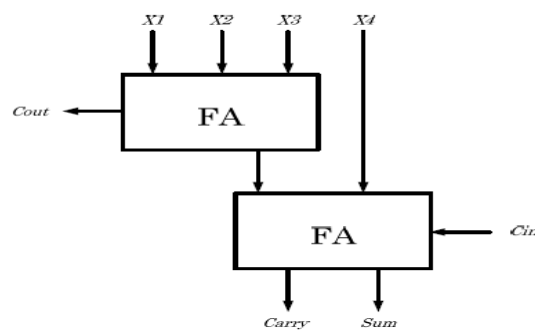


Fig9: Compressor

## V. RESULT

We evaluate the effectiveness of our architecture through architectural simulation. Model sim is used for simulation and Xilinx is used for evaluating the delay, and area for the existing and proposed architecture.

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Fig 10: Shows the simulation result for SMB1, even number of input bits. In this paper We Consider 8 bit input A,B,X.

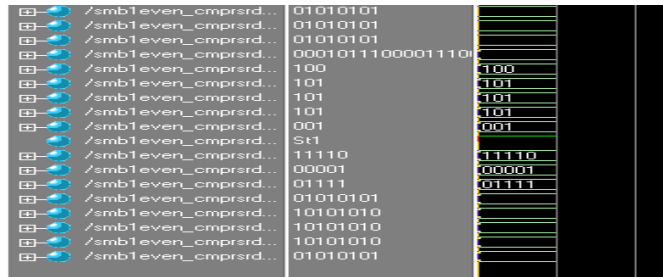


Fig 10:FAM SMB1 even bit width output

Fig 11: Shows the simulation result for SMB2, even number of input bits. In this paper We Consider 8 bit input A,B,X.

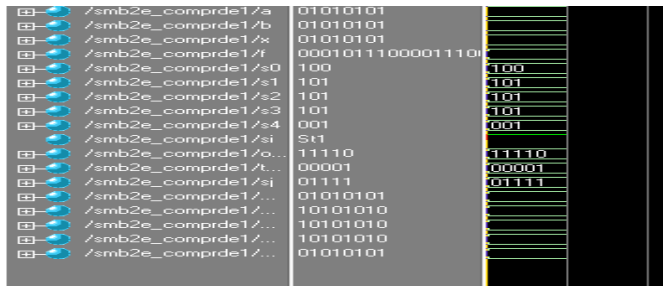


Fig 11:FAM SMB2 even bit width output

Fig 12: Shows the simulation result for SMB3, even number of input bits. In this paper We Consider 8 bit input A,B,X.

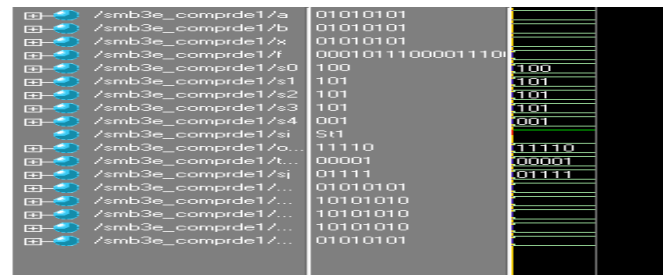


Fig 12:FAM SMB3 even bit width output

Fig 13: Shows the simulation result for SMB1, odd number of input bits. In this paper We Consider 9 bit input A,B,X.

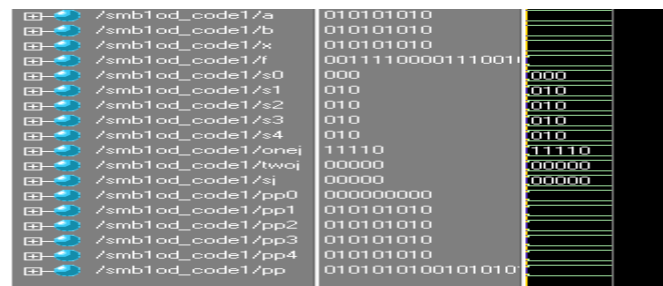


Fig 13:FAM SMB1 odd bit width output

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Fig 14: Shows the simulation result for SMB2, odd number of input bits. In this paper We Consider 9 bit input A,B,X.

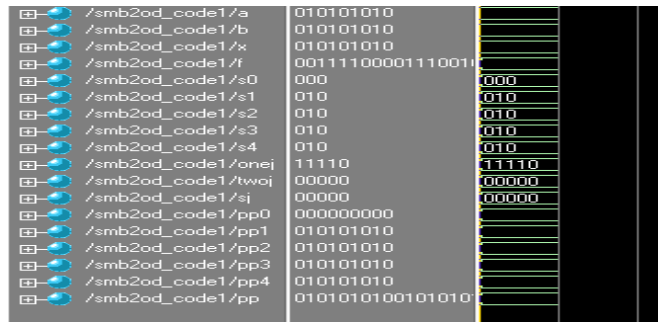


Fig 14:FAM SMB2 odd bit width output

Fig 15: Shows the simulation result for SMB3, odd number of input bits. In this paper We Consider 9 bit input A,B,X.

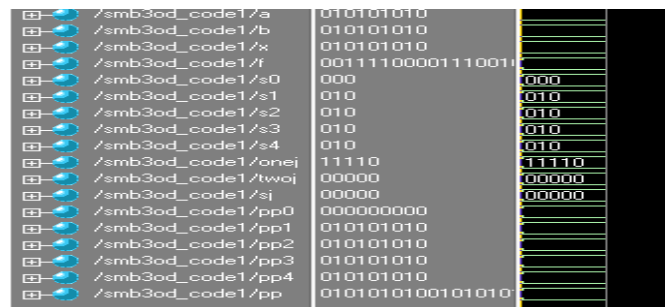


Fig 15:FAM SMB3 odd bit width output

TABLE 2: Comparison Of Existing And Designed FAM

	Conventional		Existing		Proposed	
	Even	Odd	Even	Odd	Even	Odd
Area(Out of 1728 slices)	100	110	99	117	94	111
Delay (in ns)	53.0	55.1	47.5	49.9	51.9	47.9

## VI.CONCLUSION

This paper focus on optimizing the design of the Fused-Add Multiply operator. Proposed system is based on the fusion of the adder and MB encoding unit into a single datapath block. Three different recoding techniques are introduced (SMB1,SMB2,SMB3). The techniques has been designed for the odd and even bit width of the input numbers. Thecomparison with the existing Modified Booth technique has shown an effective optimization in terms of area.

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