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Design and Analysis of Dynamic Comparator

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ABSTRACT: The need for ultra low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double-tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced.

KEYWORDS: Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs),low-power analog design.

I. INTRODUCTION

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many highspeed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra deep submicrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [6]. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods, techniques employing body-driven transistors current-mode design and those using dual-oxide processes,which can handle higher supply voltages have been developed to meet the low-voltage design challenges [10].

Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range
and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock removes the threshold voltage requirement such that body driven MOSFET operates as a depletion-type device [9]. Based
on this approach, in a 1-bit quantizer for sub-1V __
modulators is proposed. Despite the advantages, the bodydriven transistor suffers from smaller transconductance (equal to *gmb* of the transistor) compared to its gate-driven counterpartwhile special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration.

Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. In additional circuitry is added to the conventional dynamic comparator to enhance
the comparator speed in low supply voltages. The proposed comparator of [7] works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz and consumes 18 μW. Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered.

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The structure of double-tail dynamic comparator first proposed in is based on designing a separate input and crosscoupled stage. This separation enables fast operation over a wide common-mode and supply voltage range. In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in , a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced [8]. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.The rest of this paper is organized as follows. Section II investigates the operation of the conventional clocked regenerative comparators and the pros and cons of each structure is discussed. Delay analysis is also presented and the analytical expressions for the delay of the comparators are derived. The proposed comparator is presented in Section III.

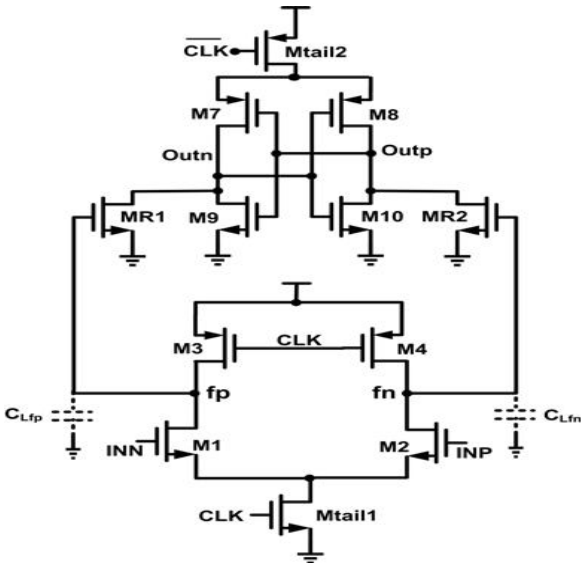
II. CLOCKED REGENERATIVE COMPARATOR

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch [4-5]. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise offset and random decision errors and kick-back noise In this section, a comprehensive delay analysis is presented; the delay time of common structures, i.e., conventional dynamic double-tail comparator are analyzed, based on which the proposed comparator will be presented.

A. Conventional Double-Tail Dynamic Comparator

A conventional double-tail comparator is shown in this topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator [3]. The double tail enables both a large current in the latching stage and wider *M*tail2, for fast latching independent of the input common-mode voltage (*V*cm), and a small current in the input stage (small *M*tail1), for low offset The operation of this comparator is as follows During reset phase (CLK = 0, *M*tail1, and *M*tail2 are off), transistors *M*3-*M*4 pre-charge fn and fp nodes to *V*DD, which in turn causes transistors *M*R1 and *M*R2 to discharge the output nodes to ground. During decision-making phase (CLK =*V*DD, *M*tail1 and *M*tail2 turn on), *M*3-*M*4 turn off and voltages at nodes fn and fp start to drop with the rate defined by *I*Mtail1/*C*fn(p) and on top of this, an input-dependent

Fig. 1. Schematic diagram of the conventional double-tail dynamic comparator



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differential voltage _*V*fn(p*)* will build up. The intermediate stage formed by *M*R1 and *M*R2 passes _*V*fn*(*p*)* to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [2].Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, *t*0 and *t*latch.The delay *t*0 represents the capacitive charging of the load capacitance *CL*out (at the latch stage output nodes, Out*n* and Out*p*) until the first n-channel transistor (*M*9/*M*10) turns on, after which the latch regeneration starts; thus *t*0 is obtained from

$$t_0 = C_L|V_{thp}|/I_{BI} = 2\,VThn CLout/\,Itail2$$

where *I*B1 is the drain current of the *M*9 (assuming *V*INP >*V*INN, see Fig. 3) and is approximately equal to the half of the tail current (*I*tail2) [1].

After the first n-channel transistor of the latch turns on (for instance, *M*9), the corresponding output (e.g., Out*n*) will be discharged to the ground, leading front p-channel transistor (e.g., *M*8) to turn on, charging another output (Out*p*) to the supply voltage (*V*DD). The regeneration time (*t*latch) is achieved according to (2). For the initial output voltage difference at time *t*0, *ΔV*0 we have

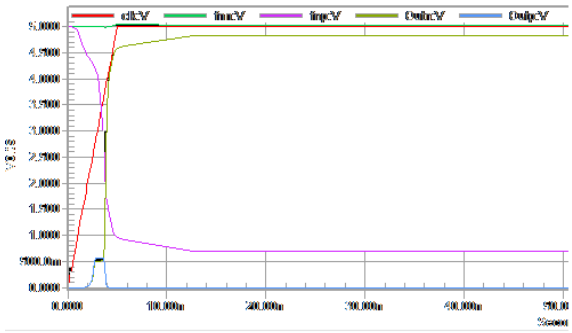
$$\Delta V0 = |Voutp(t = t0) - Voutn(t = t0)| = VThn - IB2t0/\,CLout = VThn(1 - IB2/IB1)$$

where *I*B1 and *I*B2 are the currents of the latch left- and rightside branches of the second stage, respectively.

From the equations derived for the delay of the double-tail dynamic comparator, some important notes can be concluded.

1) The voltage difference at the first stage outputs (*ΔV*fn/fp)at time *t*0 has a profound effect on latch initial differential output voltage (*ΔV*0) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator.

2) In this comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to *V*DD, which means power consumption [11]. The following section describes how the proposed comparator improves the performance of the
double-tail comparator from the above points of view.



II. PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

Fig. 5 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase _*V*fn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (*M*c1 and *M*c2) have been added to the first stage in parallel to *M*3/*M*4 transistors but in a cross-coupled manner [see Fig.5(a)].

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A. Operation of the Proposed Comparator

The operation of the proposed comparator is as follows . During reset phase (CLK = 0, *M*tail1 and *M*tail2 are off, avoiding static power), *M*3 and *M*4 pulls both fn and fp nodes to *V*DD, hence transistor *M*c1 and *M*c2 are cut off. Intermediate stage transistors, *M*R1 and *M*R2, reset both latch outputs to ground.

During decision-making phase (CLK = *V*DD, *M*tail1, and *M*tail2 are on), transistors *M*3 and *M*4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about *V*DD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose *V*INP > *V*INN, thus fn drops faster than fp, (since *M*2 provides more current than *M*1). As long as fn continues falling, the corresponding pMOS control transistor (*M*c1 in this case) starts to turn on, pulling fp node back to the *V*DD; so another control transistor (*M*c2) remains off, allowing fn to be discharged completely.

In other words, unlike conventional double-tail dynamic comparator, in which _*V*fn/fp is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor
(*M*c1) turns on, pulling the other node fp back to the *V*DD.Therefore by the time passing, the difference between fn and fp (_*V*fn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time (this will be shown in Section III-B). Despite the effectiveness of the proposed idea,one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., *M*c1) turns on, a current from *V*DD is drawn to the ground via input and tail transistor (e.g., *M*c1, *M*1, and *M*tail1), resulting in static powerconsumption.

To overcome this issue, two nMOS switches are used below the input transistors [*M*sw1 and *M*sw2, as shown in Fig. 5(b)]. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to *V*DD (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference [12]. Suppose that fp is pulling up to the *V*DD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from *V*DD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch [13].

fig. 5. Schematic diagram of the proposed dynamic comparator. (a) Main idea

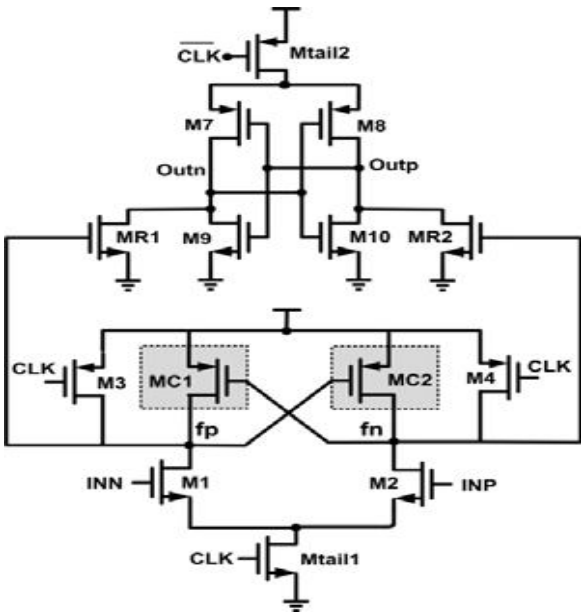

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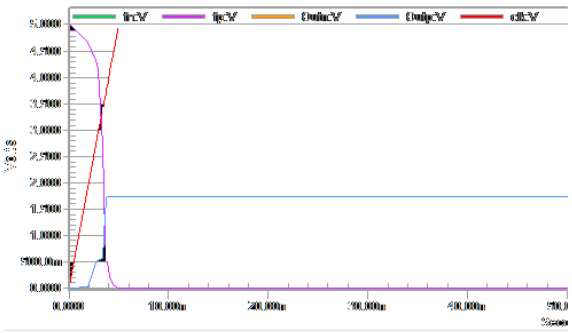
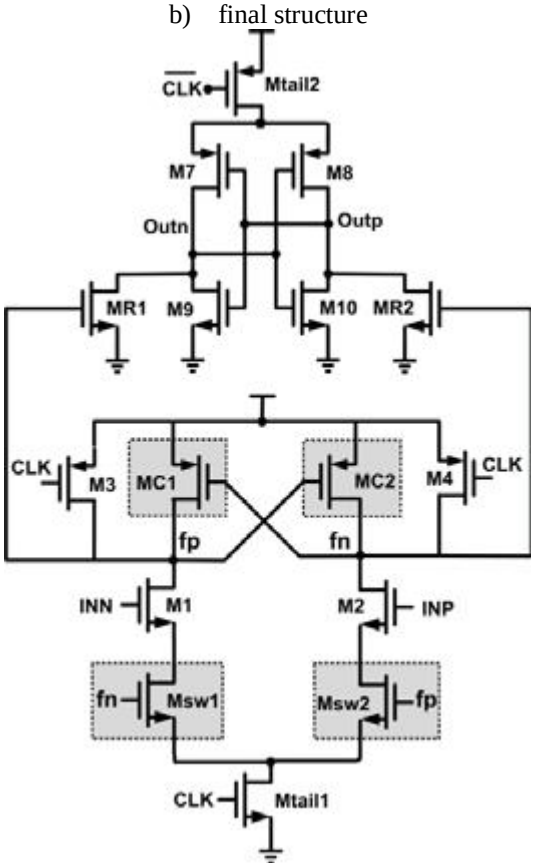
Fig 4) Transient simulations of the proposed double-tail dynamic comparator for input voltage difference



b) final structure



B. Delay Analysis

In order to theoretically demonstrate how the delay is reduced, delay equations are derived for this structure as previously done for the conventional dynamic comparator and the conventional double-tail dynamic comparator [14]. The analysis is similar to the conventional double-tail dynamic comparator, however; the proposed dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference($\Delta V0$) at the beginning of the regeneration ($t = t0$); and second, it enhances the effective transconductace ($g$meff) of the latch. Each of these factors will be discussed in detail.

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1) Effect of Enhancing$\Delta V0$: As discussed before, we define $t0$, as a time after which latch regeneration starts. In other words, $t0$ is considered to be the time it takes (while both latch outputs are rising with different rates) until the first nMOS transistor of the back-to-back inverters turns on, so that it will pull down one of the outputs and regeneration will commence. According to the latch output voltage difference at time $t0$, ($\Delta V0$) has a considerable impact on the latch regeneration time, such that bigger $\Delta V0$ results in less regeneration time. Similar to the equation derived for the $\Delta V0$ of the double-tail
structure, in this comparator we have

$$\Delta V0 = V\text{Thn-}I\text{latch}I\text{B1} \approx 2V\text{Thn-}I\text{latch}I\text{tail2} = 2V\text{Thn}$$

In order to find _Vfn/fp at $t = t0$, we shall notice that the combination of the control transistors (Mc1 and Mc2) with two serial switches (Msw1, Msw2) emulates the operation of a backto- back inverter pair; thus using small-signal model presented in , _Vfn/fp is calculated by

$$\Delta V\text{fn/fp} = \Delta V\text{fn(p)}0 \exp((\text{Av} - 1)t/\tau)$$

2) Reducing the Energy Per Comparison: It is not only the delay parameter which is improved in the modified proposed comparator, but the energy per conversion is reduced as well. As discussed earlier, in conventional double-tail topology, both fn and fp nodes discharge to the ground during the decision
making phase and each time during the reset phase they should be pulled up back to the VDD. However, in our proposed comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status
of control transistors, one of the nodes had not been discharged and thus less power is required [15]. This can be seen when being compared with conventional topologies

III. CONCLUSION

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability
was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18-μm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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