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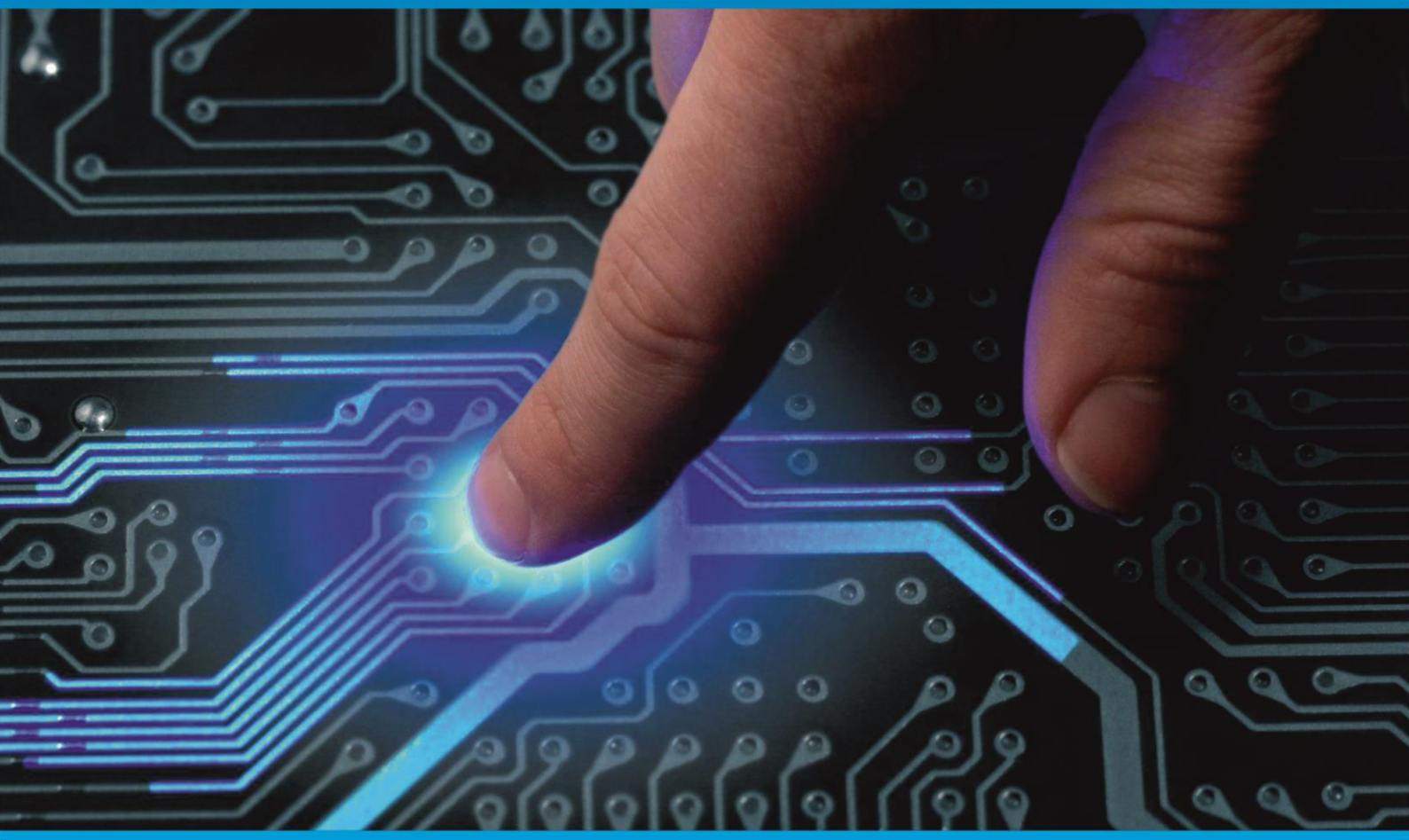

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Low Power FFT Processor Using Radix-8 Booth Multipliers

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ABSTRACT: This paper presents the plan of using radix 8 booth multiplier applied in FFT (Fast Fourier Transform) process to reduce power and area with low partial products. So that execution time of the technique is minimized and output easily generated. VLSI plays an main role in today's electronics it simply means that putting in more and more performance with lesser and lesser power consumption in mm sq. For designing low power implies the ability to reduce the dynamic power, short circuit power and static or leakage power in cmos circuits. In digital signal processing FFT algorithm is used mainly and also frequently. FFT is used in converting the time domain in frequency domain which makes the calculation easier as we always deals with various frequency bands in communication systems and also it can convert the discrete data into a continuous data type which is available at various frequencies.

KEYWORDS: Radix 8, multiplier, booth, FFT processor.

I. INTRODUCTION

The scaling down of technology in terms of area, power and delay.To execute different tasks with high speed computations and multi core processor on single chip application requires parallel processing. To analyse a signal in frequency domain FFT is mainly used in signal processing and communication applications. To evaluate DFT, FFT algorithm is used. FFT of discrete signal is called Discrete Fourier Transform (DFT).
Discrete Fourier Transform (DFT) has many applications, it is mainly used to convert discrete time domain signals into frequency domain signals but the process takes more time to convert so to reduce delay we are using Fast Fourier Transform.

DFT can be computed by following equation

$$X(k)=\sum_{n=0}^{N-1} x(n)W_N^{nk} \qquad (1)$$

Breaking down equation (1) into even and odd terms as

$$X(k)=\sum_{r=0}^{N/2-1} x(2r)W_N^{2rk}+\sum_{r=0}^{N/2-1} x(2r+1)W_N^{(2r+1)k} \qquad (2)$$

Further equation (2) can be reduced as

$$X(k)=\sum_{r=0}^{N/2-1} x(2r)W_{N/2}^{rk}+\sum_{r=0}^{N/2} x(2r+1)W_{N/2}^{rk}W_N^{k} \qquad (3)$$

$$X(k)=G(k)+W_N^{k}H(k) \qquad (4)$$

The above equation shows the multiplication used for FFT computations. The multipliers used in the FFT which are slow performing hardware units results in the degradation of the performance. Hardware implementation needs to be flexible and faster in FFT algorithm, so to increase the performance of FFT radix 8 booth multiplier is used.

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II. LITERATURE REVIEW

In existing method radix 4 booth multiplier is used for power reduction. But using this multiplier partial products are highly generated so that power and area reduction is not that much efficient and also it takes more time for power reduction. As per overview of this basic techniques that constitute the foundations for this work will be given. An example of strategic insertion of 3X calculations into the data path will be presented. Then the basic principles of the On-the-fly Correcting Radix 4 Multispeculative Multiplier will be illustrated.

A. Radix-4 Booth Multiplier

This modified booth multiplier is used to perform high speed multiplications using modified booth algorithm. The computation time and the logarithm of the word length of operands are proportional to each other in this modified booth multipliers. In this multiplier every second column is taken and multiplied by 0 or +1 or +2 or -1 or -2 instead of multiplying with 0 or 1after shifting and adding of every column of the booth multiplier. Based on this multiplier bits, the process of encoding the multiplicand is performed by radix 4 booth encoder. So it is used in FFT algorithm of digital signal processing for reducing power, area and delay but using this multiplier we cannot reduce expected amount of partial products so power, area and delay is also not reduced upto the expected level.

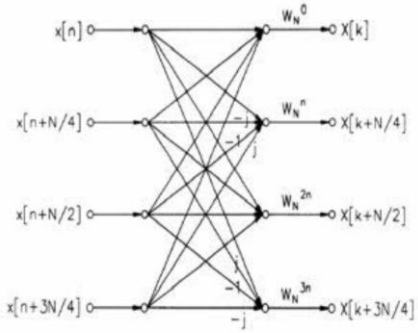

Figure 1: Radix-8 FFT Butterfly

B. Radix 4 Booth Encoder

The process of encoding the multiplicand based on multiplier bits is performed using radix 4 booth encoder. By using overlapping technique 3 bits are compared at a time. Grouping starts from the LSB, and first block uses only two bits of the multiplier and assumes a zero for the third bit. To decide whether the booth encoder calculates redundant computations the detection unit has one of the two operand as its inputs. The functional operation of radix 4 booth encoder is shown in Table 1.

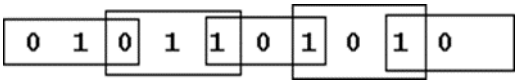

Figure 2: Grouping of the bits from multiplier term

The two bit encoding using this algorithm scans a triplet of bits for multiplication of 2's complement numbers. By considering the bits in blocks of three, such that each block overlaps the previous block by one bit to booth recode the multiplier term. Figure 2 shows the grouping of bits form the multiplier term in booth encoding. Grouping starts from the LSB, and the first block uses only two bits of the multiplier.

Each block is decoded to generate the correct partial products. The encoding of the multiplier Y, using the booth algorithm, generates the following five signed digits, -2, -1, 0, +1, +2. Each encoded digit in multiplier performs a certain operation on the multiplicand, X, as shown in Table 1.

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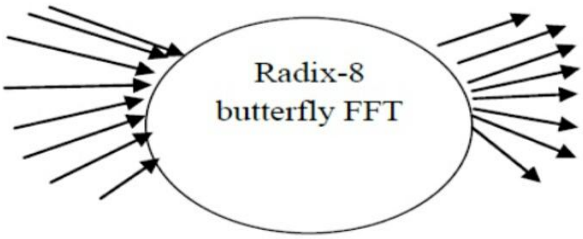
Table 1: Radix 4 booth encoder

Block	Recoded Digit	Operation on X
000	0	0X
001	+1	+1X
010	+1	+1X
011	+2	+2X
100	-2	-2X
101	-1	-1X
110	-1	-1X
111	0	0X



III. PROPOSED FFT PROCESSOR USING RADIX 8 BOOTH MULTIPLER

By using radix 8 booth multiplier which is applied in FFT (Fast Fourier Transform) process to reduce power and area with low partial products. So that execution time of the technique is minimized and output easily generated. In digital signal processing FFT algorithm is used mainly and also frequently. FFT is used in converting the time domain in frequency domain which makes the calculation easier as we always deals with various frequency bands in communication systems and also it can convert the discrete data into a continuous data type which is available at various frequencies**.**

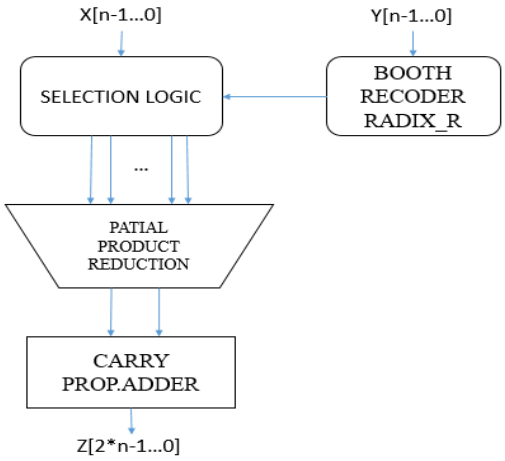


Figure 3: Block diagram for radix-8 multiplier

Figure 3 shows the block diagram of radix 8 booth multiplier first, two multiplier or multiplicand is taken. Then booth encoder is applied for one multiplier or multiplicand. After that choose one of the encoded value for multiplication and output is obtained using carry save adder.

A. Radix-8 FFT processor

A method using radix 8 booth multiplier is applied in FFT(Fast Fourier Transform) process to reduce power and area with low partial products. So that execution time of the technique is minimized and output easily generated. FFT helps in converting the time domain in frequency domain which makes the calculation easier as we always deals with various

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frequency bands in communication systems and also that it can convert the discrete data into a continuous data type available at various frequencies.

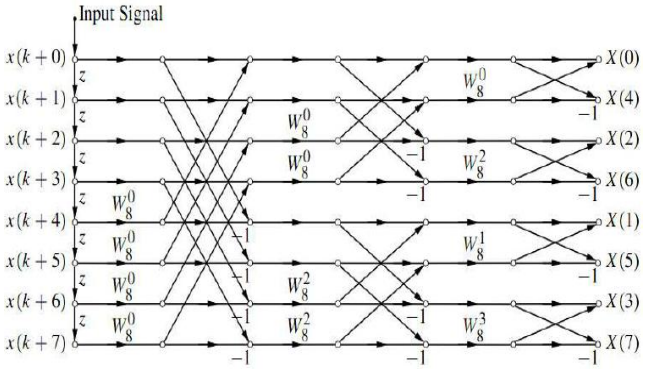

Figure 4: Basic structure of radix 8 FFT

Low generation of partial products so that time taken for the process is reduced. Radix-8 booth multiplier is used to reduce power consumption and area. especially, it is applicable in fast fourier transform (FFT) for less multiplications and reduced memory accesses so power consumption and area can be reduced. so that the processor is easily used for the construction of IC's (Integrated Circuits) with power and area efficient. Radix-8 have an advantage over radix-4 FFT algorithm because single radix-8 butterfly works of eight butterflies which will reduce the computation time.

Figure 5: Flowchart of the radix 8 butterfly FFT process

Figure 4 shows the basic structure of radix 8 FFT process. Discrete Fourier Transform is computed using FFT algorithm which consists of two methods, one is decimation in time (DIT) and decimation in frequency (DIF). Figure 5 shows the flowchart of the radix 8 butterfly FFT process.

IV. SIMULATION RESULTS

Modelsim software is a hardware simulation and debug environment which is targeted at smaller ASIC and FPGA design. That combined the simulation performance and capacity with the code coverage and debugging capabilities that required for simulation of multiple blocks and systems and attain ASIC gate-level sign-off. From the support of Verilog system, Verilog for design, VHDL, and System C that provides a solid foundation for single and multi-language design verification. Modelsim software is very friendly to use and unified debug and for simulation environment provide FPGA designers both the advanced capabilities that they are growing to need and the environment with work productive. It is also called as verification and simulation tool for Verilog System,VHDL,Verilog and mixed language designs.

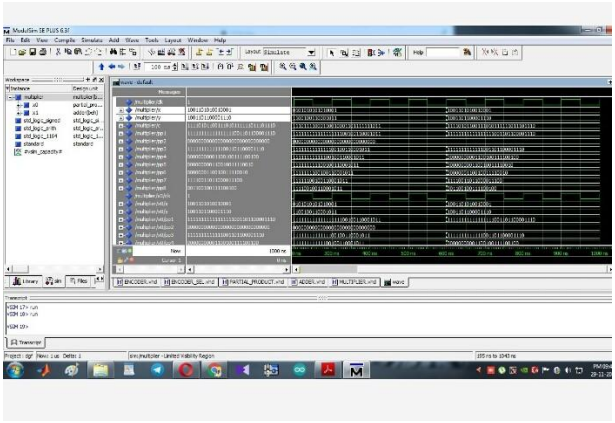

Figure 6: Simulation result of radix 8 FFT process

Xilinx ISE (Integrated Software Environment) is a software tool which is used for synthesis and analysis of HDL designs, that enables the developer to compile their designs, performs timing analysis, examine RTL diagrams,

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simulation of designs reaction to different stimuli, and configure the target device with programmer. To overcome the power challenges associated with the shrinking technologies Xilinx ISE constantly innovates new that provides the HDL and schematic editors, logic synthesizer, fitter, and bit stream generator software and XS tools from XESS provide utilities for downloading the bit stream into the FPGA on the XSA board.

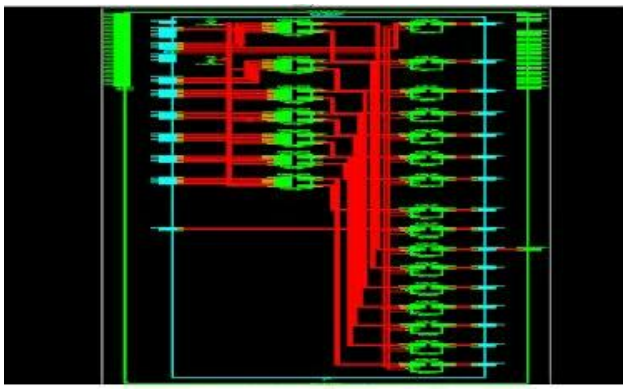

Figure 7: Design and implementation of radix 8 butterfly FFT

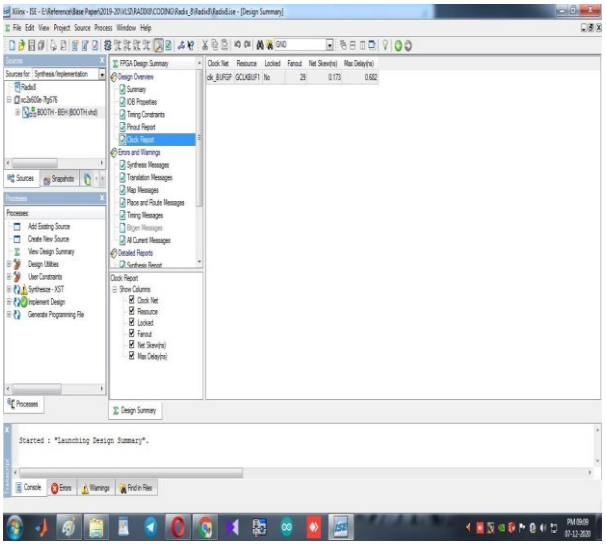

Figure 8: Power analysis

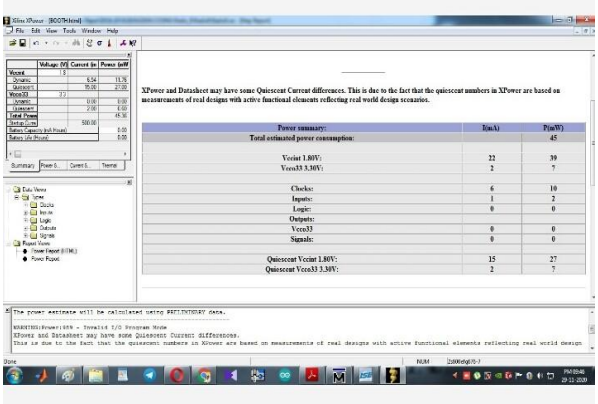

Figure 9: Delay analysis

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The Power Tools can be used for power optimization as well. That can identify which parts in the design are responsible for the most power consumption. Then can find tradeoff to design for power. That can also be coupled with power optimization algorithms available in synthesis and implementation within ISE.

V. CONCLUSION

In this project high speed, less power and area efficient FFT architecture is implemented using radix-8 booth multiplier which highly applicable in DSP applications for less multiplications and reduced memory accesses, power consumption and area can be reduced. so that the processor is easily used for the construction of IC's (Integrated Circuits) with power and area efficient. Radix-8 have an advantage over radix-4 FFT algorithm because single radix-8 butterfly works of eight butterflies which will reduce the computation time. FFT helps in converting the time domain in frequency domain which makes the calculation easier as we always deals with various frequency bands in communication systems and also that it can convert the discrete data into a continuous data type available at various frequencies. 25 percentage of power, area and delay is reduced compare to existing method and also power-delay product is reduced by half.

Table 2: Power comparison

CONSTRAINTS	EXISTING METHOD (Radix 4)	PROPOSED METHOD (Radix 8)
Number of slices latches	54	33
Total estimated power	95mW	43mW
Delay	0.72ns	0.68ns
PDP	0.067pWs	0.036pWs

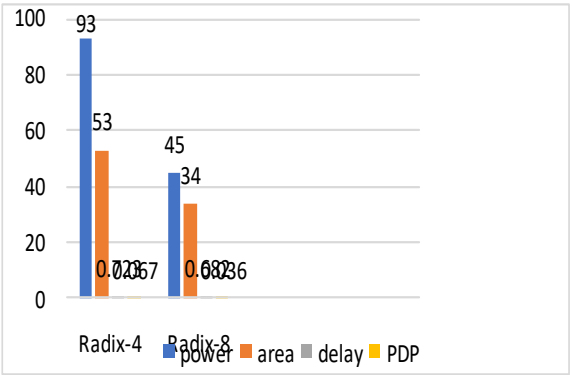

Figure 10: Comparative analysis of power, area and delay between radix 4 and radix 8 FFT process

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