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Power Efficient Destination Address Generator of Direct Memory Access Controller in Multiprocessor SoC

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ABSTRACT: In current scenario to meet the customer needs portable electronic devices are embedded with multiple processors which access the memory through controllers. Direct memory access controller[DMA] is one of the widely used controllers in Multi Processor System on Chip[MPSoC] to access memory. Destination address generator[DAG] is one of the important blocks in the DMA controller. The VLSI trends shows that the designers are concentrating on low power designs [1][2]. In this paper, synthesizable low power destination address register is designed and functionally verified. The proposed 32-bit DAG has given reduction of 38% power and 15% area when compared with conventional type of implementation.

KEYWORDS:MPSoC, DMA, DAG, Memory Management Unit (MMU), GPU, FSM, Address Generator Unit (AGU).

I. INTRODUCTION

Today's System on Chip designs is complex in terms of functionality, performance and integration in order to meet ever demanding customer's functional needs. Single processors may be sufficient for low-performance applications that are typical of early microcontrollers, but an increasing number of applications require multiprocessors to meet their performance goals. Multiprocessor is Parallel processors with a single shared address. It is cost effective processor with high performance than the faster uni-processor. Advancement in VLSI technology permits designers to integrate all the functions required by the end user. Multiprocessor systems-on-chips (MPSoC) are one of the key applications of VLSL technology. It also consists of:

- Multiple processors, software protocol stacks, memories, Real Time Operating System [RTOS]
- Memory block such as RAM, ROM and flash memory.
- On chip buses and many peripheral external interfaces such as USB, Ethernet and SPI.
- Hundreds of digital logic blocks such as Counters, Timers.
- Advanced peripherals such as DMA Controller, Memory management unit (MMU), Graphics processing unit (GPU) and Wi-Fi module.
- Power management circuits and voltage regulators.
- Analog interfaces which includes ADCs and DACs.
- Multimedia which includes MPEG Decoder and JPEG Compression [3] are all integrated in a single chip.

An MPSoC consists of hardware and software which controls multiple processors,DSP cores,peripherals.Design flow for MPSoC develops both hardware and software simultaneously and has many advantages such as high performance, good battery life, miniaturization and cost efficiency [4]. It has much functionality compared to CPU. It is possible to build a computer with a single MPSoC. Hence it is used in many applications like mobile computing, digital cameras, printers, pagers and so on. Since MPSoC integrates millions of gates, heavy power consumption is a major concern. Therefore, it demands expensive packaging, heat sinks and cooling environment. This paper concentrates on reducing the power of an important block in the MPSoC.

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As the process technology shrinks, the complexity in the design and area occupied by the memory also increases. It is observed that embedded memory occupies more than 50% area of the chip. Figure 1 shows the increase in area occupied by memory. It can be seen that the amount of space occupied by memory has increased from 20% to 70% [5]. An efficient real-time system is one where the CPU is used for the maximum number of tasks to yield better real-time responsiveness and lower power consumption while still being flexible enough to support future enhancements.

II. RELATED WORK

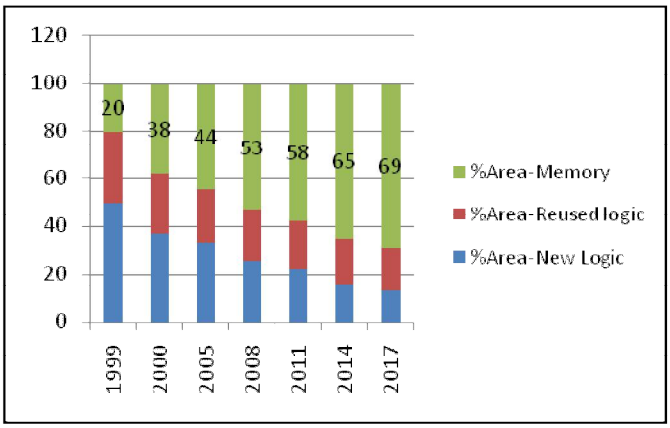

Figure 1: Survey on Area occupied by memory in MPSoC [5]

In order to reduce the CPU time that is being wasted in data transfers, many systems include a peripheral which can do data transfer operations without including the CPU. This peripheral is called the Direct Memory Access (DMA).Hence the performance and yield of MPSoC is largely dependent on memory. Since the data transfer takes place between memory and other peripherals in the MPSoC, Direct Memory Access Controller is an important block. DMA controller is used to transfer data within the chip (intra-chip) in multiprocessor MPSoC. Here DMA is used to transfer data between local memory of a processing element and the main memory. So, this reduces the overhead of CPU [6].

DMA supports various features such as:

- Byte and word transfer.
- Request or non-request mode of transfer.
- DMA transfer through or interrupt or polling.
- Modes of operation-Burst mode, Cycle stealing mode, transparent mode [7].

DMA Controller is an important block in MPSoC which is used to increase the data transfer rate.Its efficiency improves the overall performance of MPSoC. Figure 2 shows the interface of DMA controller in MPSoC used in smart phoneapplication [8]. DMA controller facilitates subsystem to use the main memory without the intervention of CPU. CPU remains busy throughout the read or write cycle without DMA. So it cannot perform any other work. With the help of DMA, CPU receives interrupt signal from DMA controller once the data transfer is complete. This enables to do other operations without wasting CPU time which is illustrated in Figure 3 [9].

Data transfer which takes place without the help of CPU is called zero copy transfer. The best method is to select a processor which has internal DMA so that overhead of entering and exiting DMA mode is minimized [10]. DMA is used in multi core processors for data transfer within the chip. It is used in DSP related applications in which lot of computations are involved. In such case, flow of control is as follows. The DMA sends hold request [HRQ] to theHOLD input of the microprocessor. The processor responds to this by floating its buses in the high impedance state and sends HLDA signal [11].Then, controller performs data movement, while core can perform other operations. Controller sends an interrupt request indicating completion of task. Then the core decides if it should process the data. The speed of data transfer dependson the speed of DMA controller [12]. There are various blocks in DMA controller such as source decoder, destination decoder, and transaction Finite State Machine [FSM]. There are two ports in DMA module: Source port and destination port. DMA controller moves the data from source to destination port as specified by DSP Core. Therefore there are two address generator units: One to provide address for source port and other to provide address for destination port respectively known as *Source Address Generator* and *Destination Address Generator*.

In any memory accessing applications, source and destination address generator are the basic building blocks. Destination address generator is a memory block which is used to generate address for any further process. In order to perform the data transfer, several parameters like step size, transfer length, data size should be considered. Destination address points to location where the data has to be moved. After every transfer is performed, the destination address is

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modified by the generator depending on the input values. The input and the control signals are provided by the other blocks of memory. This module does not require any counter to count the number of words transferred unlike the source generator.

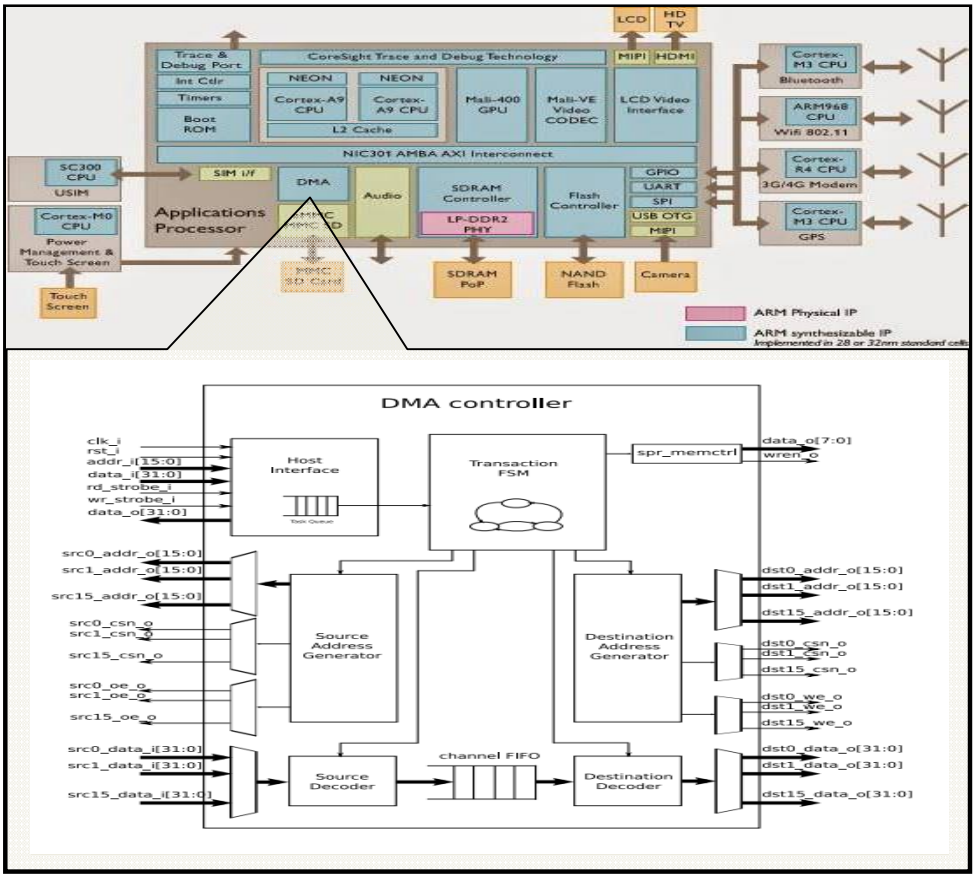

Figure 2: Direct Memory Access Emphasis [8]

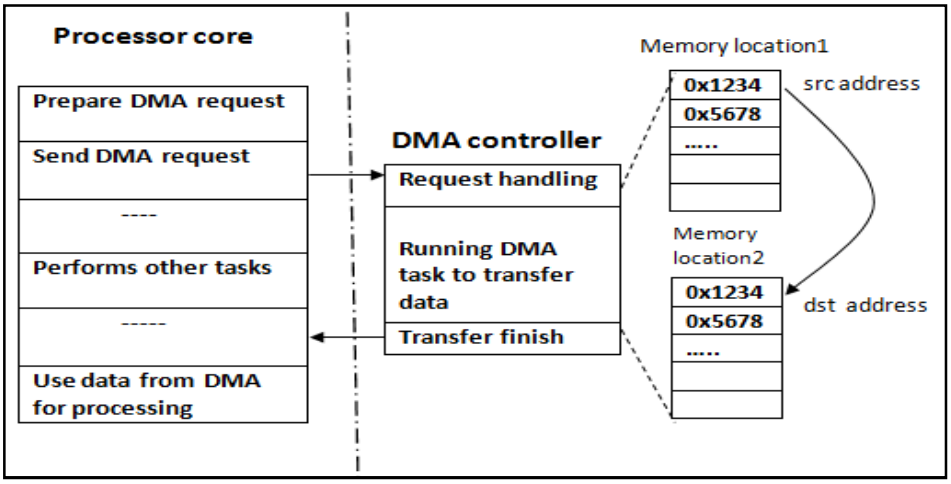

Figure 3:DMA Operation to save CPU Time [9]

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III. MECHANISM OF DESTINATION ADDRESS GENERATOR

The main objective of this unit is to generate the address according to the control signal that is provided by FSM. When *enable_i* signal is HIGH, selection and processing of signals is done. *step_i*→ step size by which the address has to be incremented. Step sizes included in this paper are 1, 2, 4, and 8, the way in which it is selected and added is the crucial step in power reduction. In order to move the data to next location, it is sufficient to increment the previous address by the required step. On the other hand, to move the data to the defined location, the address has to be read from the input. This decision is accomplished by using a select line called *setaddr_i.*The description and the width of various input and output signals are explained in Table 1 [9].

Table 1:Desciption of Destination Address Generator[9]

Signal Description	Width (Bits)	Direction	Description
clk_i	1	Input	Clock input
step_i	2	Input	Step size with which address is incremented.
enable_i	1	Input	Enables AGU
setaddr_i	1	Input	Select line for MUX
addr_i	32	Input	Starting address
addr_o	32	Output	Address output

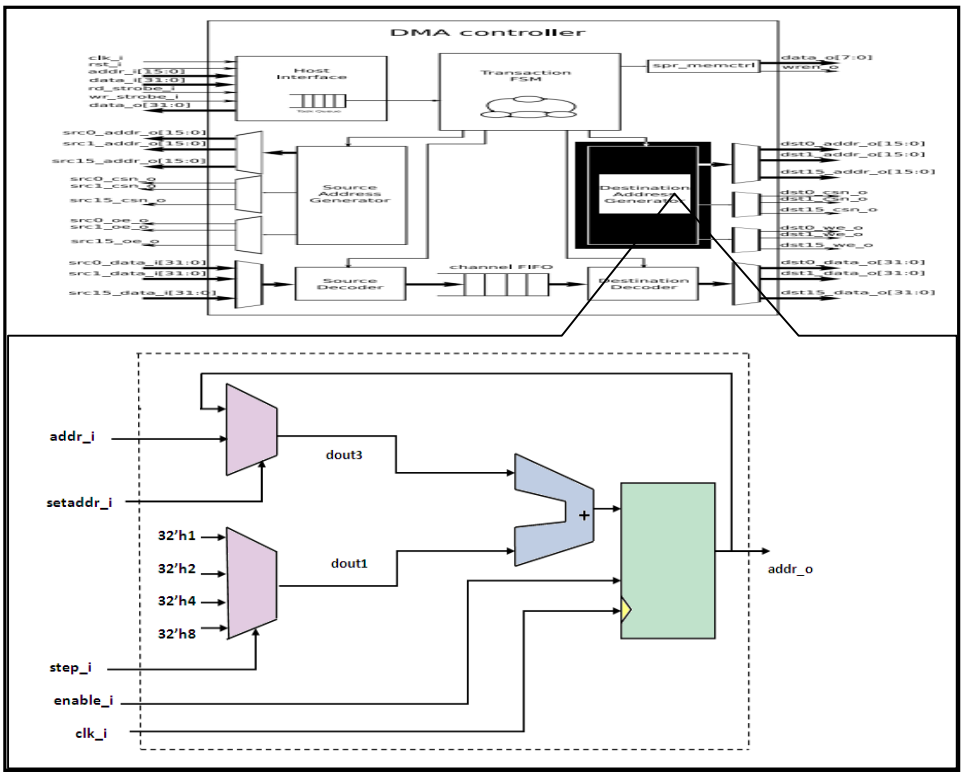

Figure 4 : Destination address generator of DMA Controller [9]

Address generator unit and its association with other units in the DMA controller is shown in Figure4 [9].

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IV. IMPLEMENTATION OF DESTINATION ADDRESS GENERATOR

A. *Design Considerations:*

In this design, step size is added to *addr_i* or *addr_o*directly using addition operator. This selection is made using 2:1 multiplexer. *setaddr_i* is used as select line for this multiplexer. Step size is passed to the adder directly, that means, *step_i*is no longer works as a select line. It is used as a 32-bit input line to the adder. The built-in addition function which is predefined consumes more power. In addition to this, the 32-bit data sent directly to the module contributes to the increase in power. As already mentioned this is just one unit of a complex DMA Controller. The increase in power of this block increases the power of entire DMA controller which is a part of some other multi-core processor. The cumulative increase in power will have adverse effects on the efficiency which in turn decreases the performance of the entire system. This power issue is overcome in the proposed model without altering the functionality of the destination address generator.The block diagram of this design is shown in the Figure 5. *addr_o* is a 32-bit output which gives the next address to which the data should be moved.

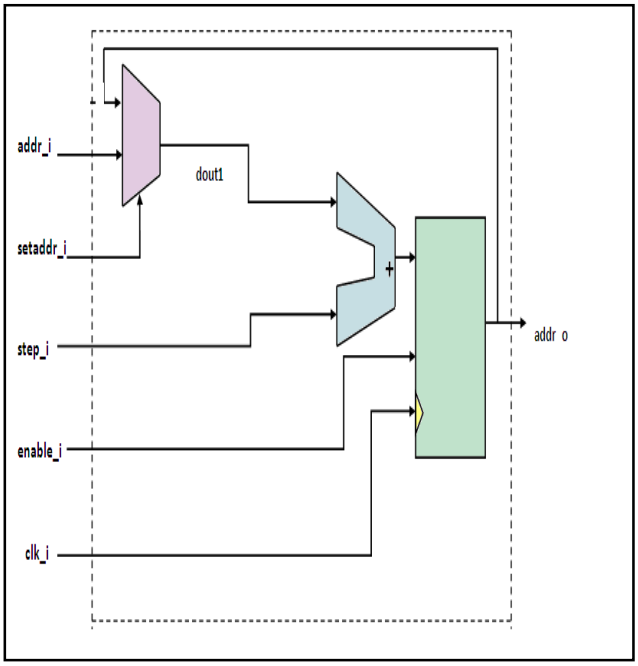

Figure-5: Block Diagram of Destination Address Generator

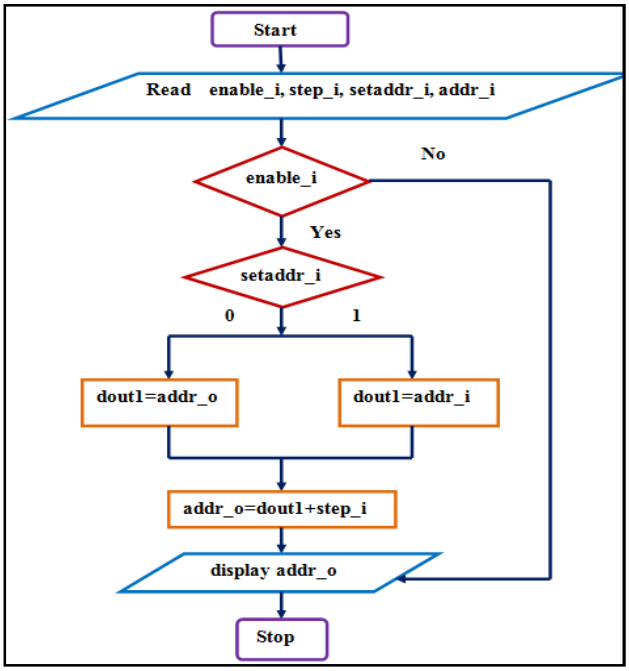

Figure-6: Design Flow Chart of Destination Address Generator

B. *Description of the Proposed Destination Address Generator:*

In the proposed design, *step_i* is used as a select line for 4:1 multiplexer. In some cases, it is not convenient to increment the address by one location. So step sizes other than one are needed. Select line is used to select the step sizes of 1, 2, 4, or 8.Therefore *step_i* is a 2-bit input. This is the main reason for power reduction. Like the normal generator, the input to the adder is a 32-bit input. Besides this, a task is written in Verilog to add the two 32-bit data[12]. This is written in such a way that it consumes less power. This is the major advantage over the normal address generator. All other functionalities remain the same as that of the previous one. This is verified by comparing the simulation results of both.

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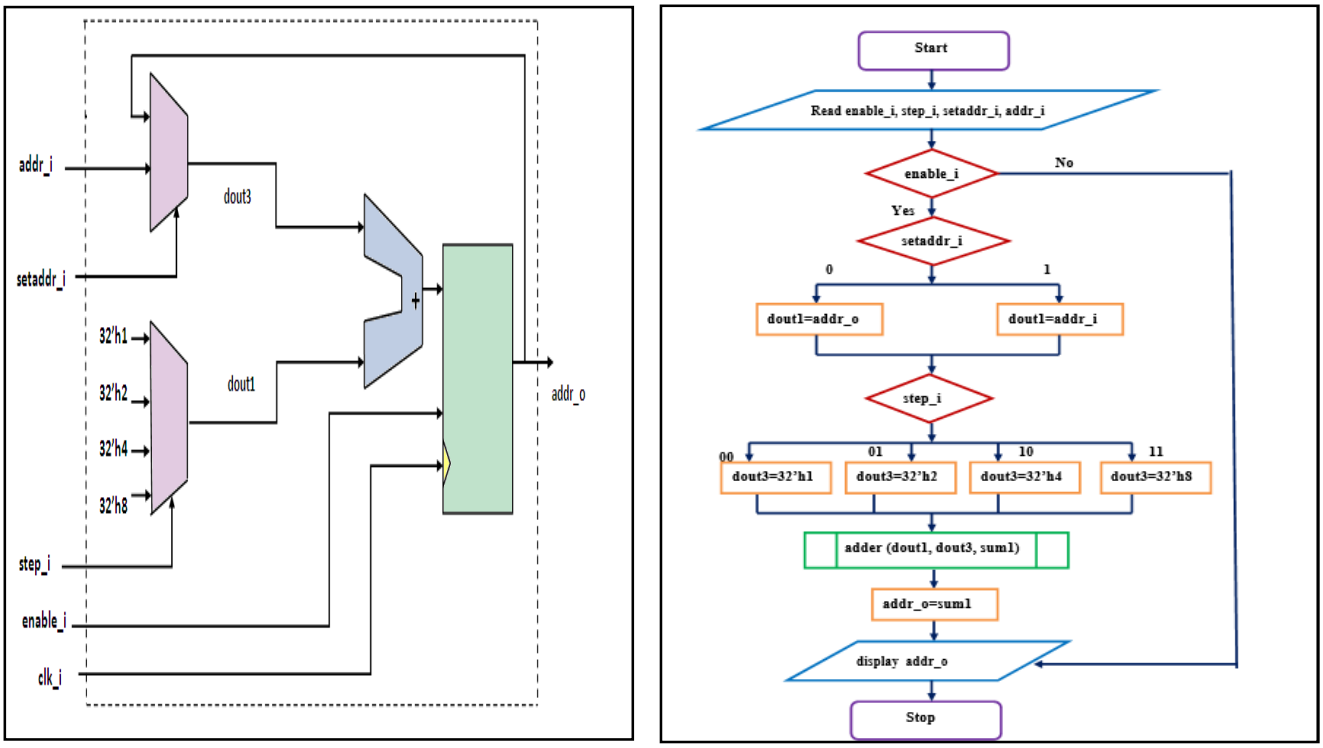

Figure-7(a): Block Diagram 7(b) Flowchart of Proposed low power Destination address generator

The block diagram of the implemented low power design is shown in Figure 7.It should be noted that adder shown in figure 5 is replaced by the code that is written for low power consumption. As seen from the figure 7, a D flip flop is used to enable the generator unit. The design flow of proposed low power address generator is explained in the Figure 8, adder is a Verilog task which stops the sequential execution.

V. SIMULATION RESULTS AND DISCUSSIONS

The simulation result for destination address generator is shown inFigure 8

1. When*enable_i* is HIGH. Select line for *mux*, *setaddr_i* is HIGH. Hence selects addr_i which is equal to 9. step_i is adder adds 9 and 1 to give 10 as the *addr_o* output.
2. When *enable_i* is HIGH. *setaddr_i* is LOW and hence selects *addr_o* which is equal to 11. *step_i* which determines the increment step is 1. Hence the output of the adder is 12.
3. When *enable_i* is LOW. The output of the adder remains unchanged irrespective of any changes in other input signals.
4. When *enable_i* is HIGH. *setaddr_i* is HIGH which selects *addr_i*. Since step_i is 1; *addr_i* which is equal to 1522275410 gets added with 1 to give 1522275411 as *addr_o* output.
5. Both the destination address generator units are designed in Verilog and the functionality is verified by simulations obtained using Xilinx.

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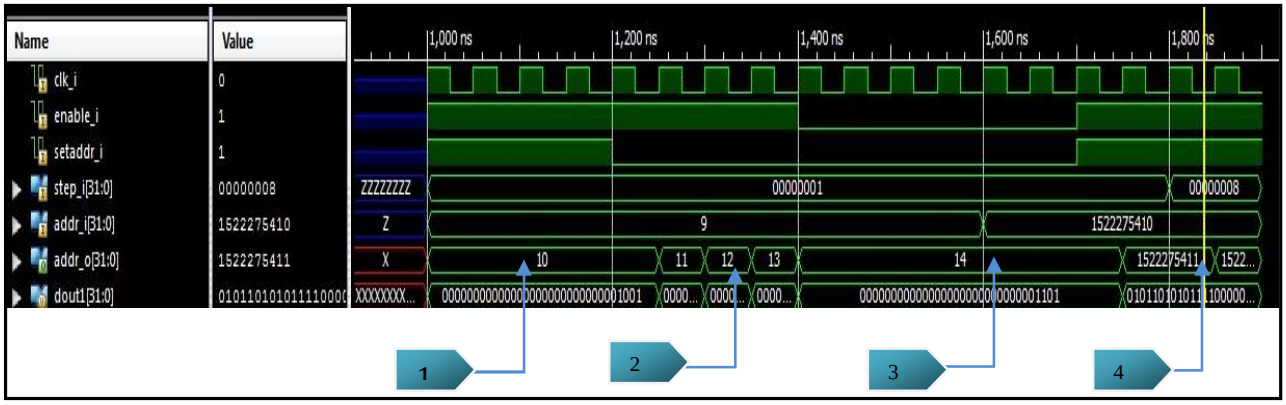

Figure 8: Simulation result for Destination Address Generator

The simulation result for low power destination address generator is given in Figure 9. Output is obtained for various combinations of input signals. Different cases are explained below.

1. When *enable_i* is HIGH. *setaddr_i* is HIGH. So, it selects *addr_i* which is equal to 9. The select line *step_i* is 00. Therefore, it selects step size of 1. Hence the adder output is 10.
2. When *enable_i* is HIGH. *setaddr_i* is LOW which selects *addr_o*. The step size is 1 since *step_i* is 00. Therefore, previous adder output adds with 1 to give 12.
3. When *enable_i* is LOW. The output remains same irrespective of any changes in the input signals. So, the output of the adder is 14.
4. When *enable_i* is HIGH. *setaddr_i* is HIGH which selects the new *addr_i* input 1522275410.The step size is 1 since *step_i* is 00. Therefore, the adder output is 1522275411.

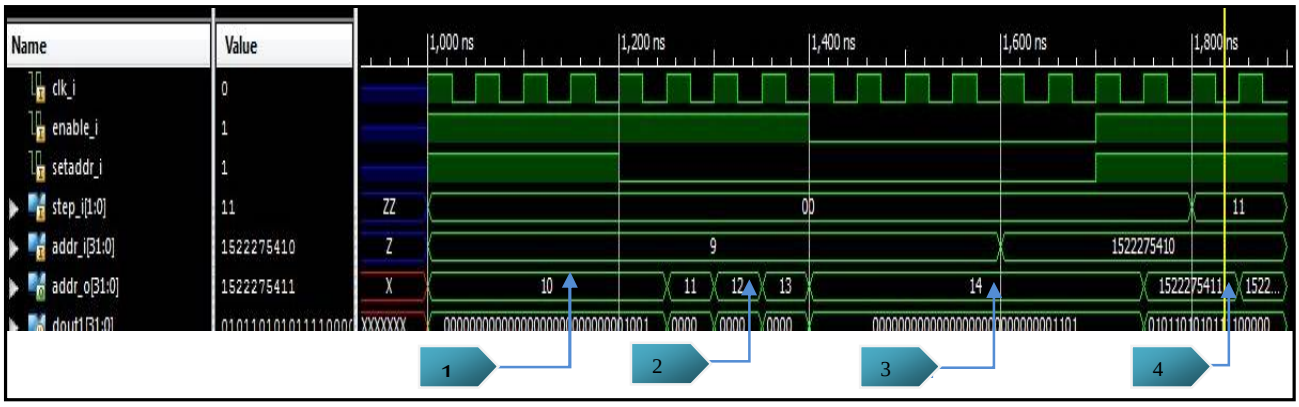

Figure 9: Simulation Results for Proposed Low Power Destination Address Generator

The synthesis report for power and area were obtained after targeting the design to 180nm Slow_nornal.lib using RTL Complier from Cadence.The synthesis reports obtained by both designs are compared Table 2. It can be seen that the implemented block has given *reduction*of *38% power, 15.3% area and 34.8% timing*when compared with the traditional one.

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Table-2: Power, Area and Timing Comparison of 32-bit Data Size

Parameters	Cell Total area	Leakage power(µw)	Dynamic power(µw)	Total power(µw)	Timing(ps)
Destination address generator	1298	4.82	43.29	48.11	6369
Low power model	1099	2.89	26.84	29.74	4087
Percentage Change	15.33% ↓Decrease	40.07% ↓ Decrease	37.98% ↓ Decrease	38.19% ↓Decrease	34.81% ↓ Decrease

Also, Synthesis report for Power, Area and Timing is performed for 8-bit, 16-bit, and 32-bit and is as shown in Table 3. The reduction in power,area and timing is significant in low power model compared to the conventional model for increased data widths.

Table 3: Power, Area and Timing Comparison for different Data Size

Models	Destination address generator			Low power model		
Parameters	*Power(µw)*	*Area*	*Timings(ps)*	*Power(µw)*	*Area*	*Timings(ps)*
8-bit	11.77	315	2021	8.62	286	1465
16-bit	23.99	664	3420	15.62	557	2296
32-bit	48.11	1298	6269	29.74	1099	4087

VI. CONCLUSION AND FUTURE WORK

In this paper, two different methodologies of implementing destination address generators are proposed. It is evident from the result obtained after synthesis that the leakage, dynamic power, area and timing have reduced significantly. This is beneficial in many applications where the low power consumption is in need. In the similar way other blocks of DMA controller can be designed which in-turn reduces the overall power consumed by the direct memory access controller block.

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