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Design of 8 Bit Asynchronous Counter Using Reversible Logic

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ABSTRACT: Reversible logic design is widely used for realizing any Boolean function using the basic reversible gates. It has different areas for its application, those are low power CMOS, advanced computing, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. In this paper we proposed the design of D Flip flop and counter using reversible logic gates and comparison of existing reversible D Flip Flop design with optimized reversible D Flip Flop. Asynchronous counters are designed using the existing and proposed D FF. The proposed counter has found to be better in terms of power consumption by about 50%.

KEYWORDS: Reversible logic, Power dissipation, garbage outputs, constant inputs, Quantum cost.

1. INTRODUCTION

Energy dissipation is one of the main considerations in digital circuit design. The irreversible computation tends to lose information during execution. The information loss dissipates in the form of heat, dissipation of heat results in power dissipation. To reduce the power dissipation a new logic called reversible logic has been introduced. The main idea behind this logic is to reduce power dissipation by preserving information content. By implementing circuits using reversible logic a significant amount of heat energy dissipated can be decreased. Due to their capability to reduce power dissipation; it finds applications in low power VLSI design, quantum computation and optical information processing.

The main difficulties in designing the reversible circuits are to reduce the number of quantum cost, garbage outputs, delay and constant inputs. This paper proposes optimized design for D flip flop and 16-bit asynchronous counter.

II. BASIC DEFINITIONS OF REVERSIBLE LOGIC

2.1. Reversible Function

The multiple output Boolean Function F(x1, x2, ..., xn) of n Boolean variables is called reversible if:

The number of outputs is equal to the number of inputs,

Any output pattern has a unique pre-image.

2.2. Reversible Logic Gate

The gates or circuits that do not loose information are called reversible gates or circuits. A reversible circuit is such a circuit in which the number of input and the number of output is equal. Reversible logic has unique mapping between input and output bit pattern. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.

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2.3. Ancilla inputs/ constant inputs

The input that is added to a function to make it reversible is called constant input. This refers to the number of inputs that are to be maintain constant at either 0 or 1 to synthesize the given logical function.

2.4. Garbage outputs

Garbage output is defined as the outputs that are not primary output or output that are not used as input to another gate. More formally, unwanted or unused or unutilized outputs which are needed only to maintain reversibility of a reversible gate is known as garbage output. Additional inputs or outputs can be added to make the number of inputs and outputs equal whenever necessary.

Input + constant input = output + garbage

2.5. Quantum cost

Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated to know the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The cost of all 2*2 gates are same and it is 1 and 0 for 1*1. Every circuit can be constructed from those 1*1 and 2*2 quantum primitives and the cost of circuit is the total sum of used 2*2 gates.

2.6. Gate Level

This refers to the number of levels in the circuit which are required to realize the given logic functions.

2.7. Power

This refers to the total power dissipated during logical operation in entire design by using CMOS logic.

2.8. Hardware Complexity

This refers to the total number of logic operation in a circuit. It means the total number of AND, OR and EXOR operation in a circuit.

2.9. Delay

The path which consist maximum number of gates for any input to any output in the circuit is known as critical path. Delay of a reversible circuit is the delay of this critical path. The delay of each 1*1 and 2*2 reversible gates is taken as unit delay,1.

2.10. Design Constraints for Reversible Logic Circuits

Reversible logic gates do not allow fan- outs.
Reversible logic circuits should have minimum quantum cost.
The design can be optimized to produce minimum number of garbage outputs.
The reversible logic circuits must use minimum number of constant inputs.
The reversible logic circuits must use a minimum gate level.
Reversible logic circuits should have minimum power.
The reversible logic circuits must use minimum hardware complexity.

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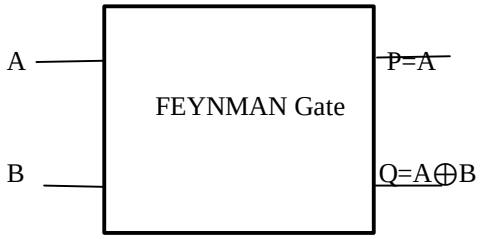
III. BASIC REVERSIBLE LOGIC GATES

3.1. FEYNMAN Gate

Feynman gate is a 2*2 one through reversible gate. It is also called as controlled NOT gate (CNOT). The input vector is I (A, B) and the output vector is O (P, Q). Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs. The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is l. It is a one through gate since one of its input is the output.



3.2. FREDKlN Gate

The Fredkin gate (3*3) is a reversible 3-bit gate that swaps the last two bits if the first bit is 1, i.e., a controlled-swap operation. It is used as a 2:1 mux and out of three inputs, one input acts as enable. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A'B ⊕ AC and R=A'C ⊕ AB. Quantum cost of a Fredkin gate is 5. It is also a one through gate since one of its input is the output. The transistor implementation of the Fredkin Gate that needs only four transistors.

A P=A

is defined by P=A, Q=A'B ⊕ AC, R=A'B ⊕ AC

B FREDEKIN Gate

Q= A'B ⊕ AC
⊕ D and S=AB ⊕ A'C ⊕ D. The quantum cost of

Sayem gate is 14.

C R=A'C ⊕ AB

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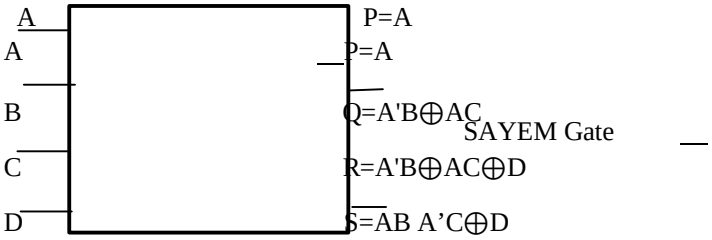
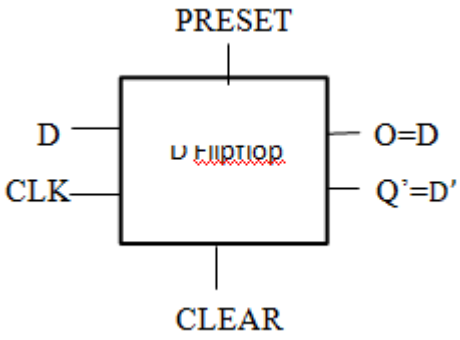
3.3. TOFFOLI Gate

TOFFOLI gate which is a 3*3 gate with the input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=B, R=AB
⊕ C. It has Quantum cost five. It is also known as the Controlled-Controlled-NOT(C-C-NOT) gate.



4. EXISTING D FLIPFLOP

A flip-flop is a device which stores a single bit of data, one of its two states represents a "one" and the other represents a "zero". The D flip-flop is also known as a "data" or "delay" flip-flop. The D flip- flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change.



5. EXISTING ASYNCHRONO

A counter is a device which can count any particular event based on how many times the particular event is occurred. An Asynchronous counter where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. A counter may count up or count down or count up and down depending on the input control.

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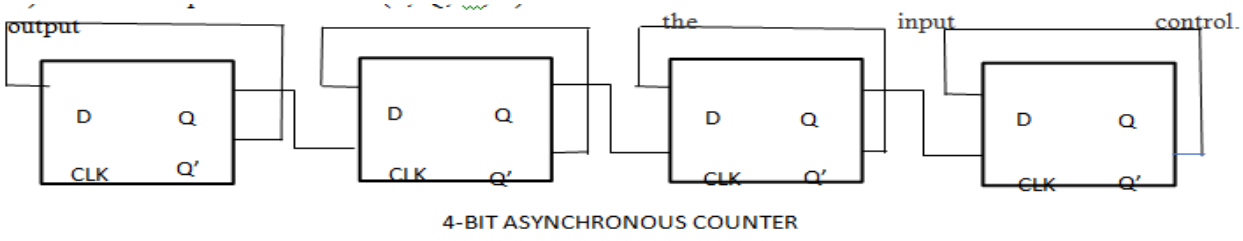
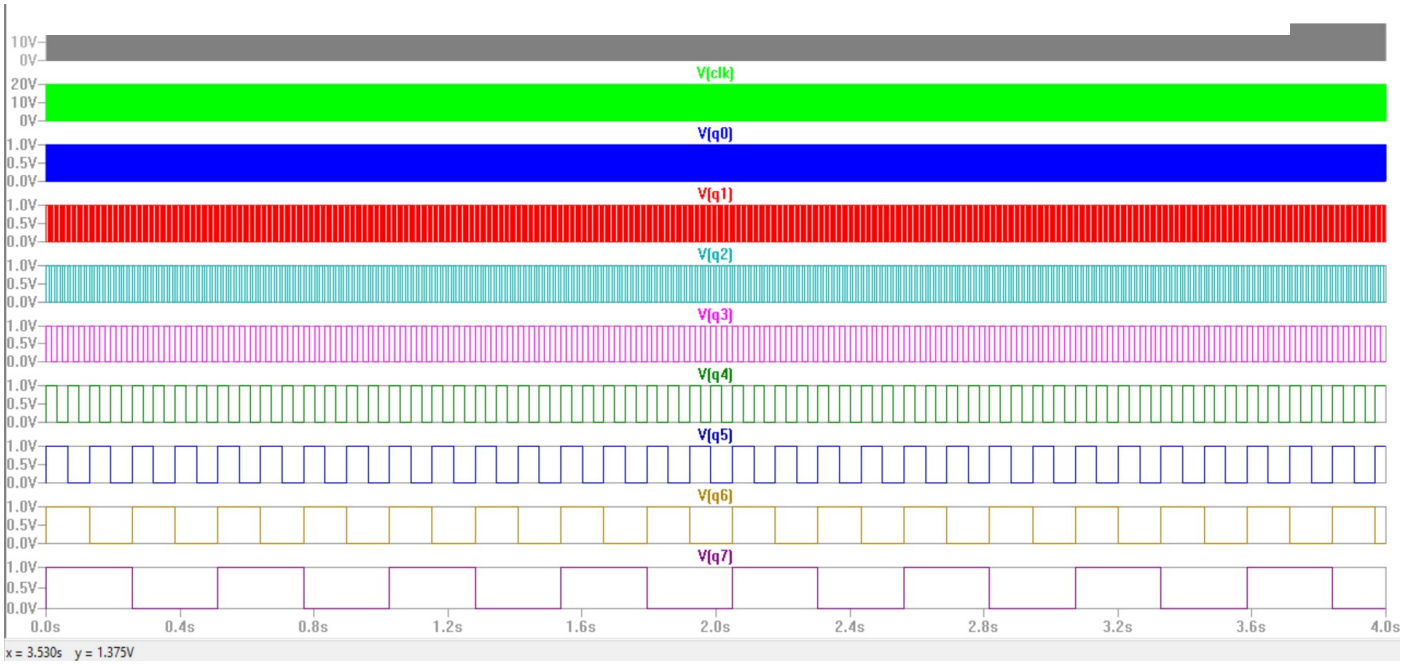


4-BIT ASYNCHRONOUS COUNTER



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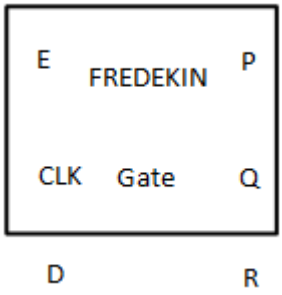
6. PROPOSED D FLIPFLOP

The Fredkin gate (3*3) is a reversible 3-bit gate that swaps the last two bits if the first bit is 1, i.e., a controlled-swap operation. It is used as a 2:1 mux

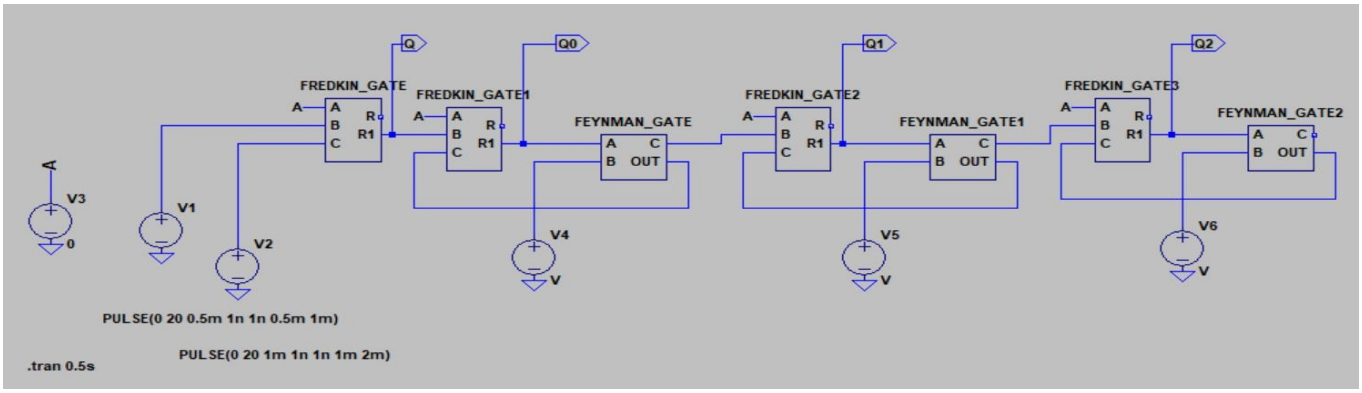
Gate Qis O (P, Q, R). The output is defined by P=A, Q=A'B □ AC and R=A'C □ AB.

7. PROPOSED ASYNCHRONOUS COUNTER

The combination of Fredkin and Feynman gate is used for the proposed asynchronous counter. The use Feynman Gate as a copying gate. Since a fan-



out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.



4-BIT ASYNCHRONOUS COUNTER

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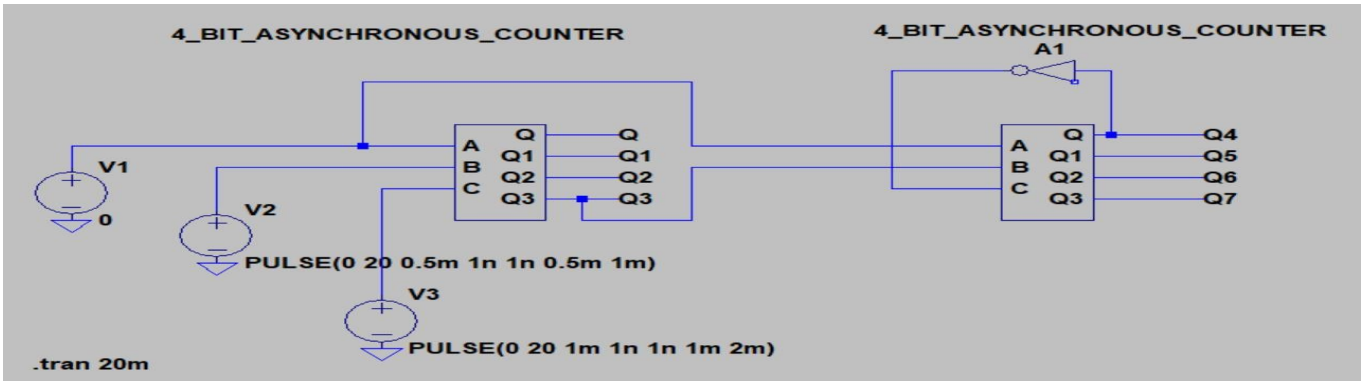
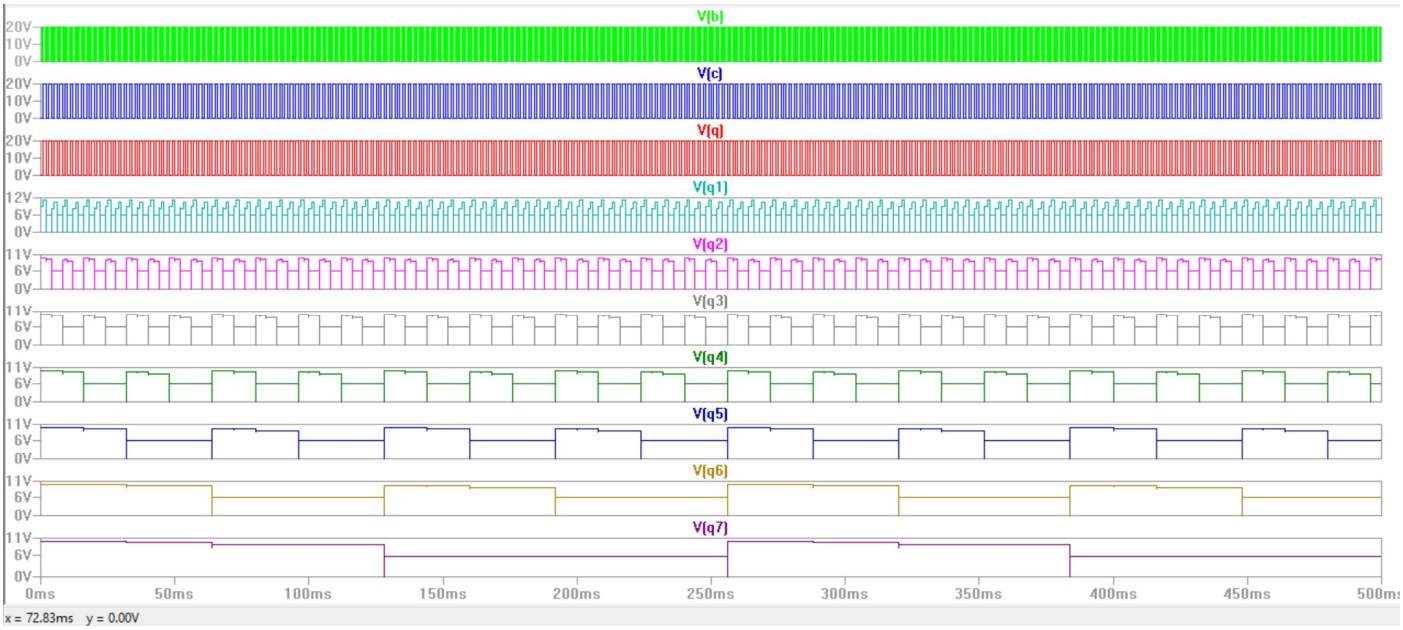


8-BIT ASYNCHRONOUS COUNTER



VIII. COMPARISON 0F EXISTING AND PROPOSED COUNTERS

	NUMBER OF TRANSISTORS	POWER CONSUMPTION
EXISTING D FLIPFLOP	18	516.4e-6
PROPOSED D FLIPFLOP	4	278.8e-6
EXISTING COUNTER	144	2.11e-3
PROPOSED COUNTER	53	913.2e-6

IX. CONCLUSION

By using Reversible logic, the number of transistors needed for the designing of 8-bit asynchronous counter is reduced. The power dissipation happened at the time of lose of information also eliminated here. Thus, the consumption of power also decreased automatically.

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