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A 10-Bit 50-Ms/S Monitoring SAR ADC with A Monotonic Capacitor Switching Procedure

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ABSTRACT: The proposed system presents a low-power 10-bit 50-MS/s successive approximation register (SAR) analog-to-digital converter (ADC) that uses a monotonic capacitor switching procedure. When compared to the converters which generally use the conventional or the old procedure, the average switching energy and total capacitance are reduced by about 81% and 50%, respectively. In the switching procedure, the input common-mode voltage gradually converges to ground. An improved comparator diminishes the signal-dependent offset caused by the input common-mode voltage variation. The prototype was fabricated using 0.13- m 1P8M CMOS technology. At a 1.2-V supply and 50 MS/s, the ADC achieves an SNDR of 57.0 dB and consumes 0.826 mW, resulting in a figure of merit (FOM) of 29 fJ/conversionstep. The ADC core occupies an active area of only 195 X 265 μ ㎡. Thus the proposed system guarantees low power consumption , reduced delay power and high performance.

KEYWORDS: Successive approximation register, Analog to digital convertor, CMOS, MOSFET, Comparator.

I. INTRODUCTION

SAR is an abbreviation for **Successive Approximation** Register. A **SAR ADC** uses a series of comparisons to determine each bit of the converted result. Therefore, a **SAR ADC** needs at least n+1 clock cycles to convert an analog input to the **ADC** to a result, where n is the number of bits of the **ADC**.

SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) require several comparison cycles to complete one conversion, and therefore have limited operational speed. SAR architectures are extensively used in low-power and low-speed (below several MS/s) applications. In recent years, with the feature sizes of CMOS devices scaled down, SAR ADCs have achieved several tens of MS/s to low GS/s sampling rates with 5-bit to 10-bit resolutions. Although flash and two-step ADCs are preferred solutions for low-resolution high-speed applications, time-interleaved and multi-bit/step SAR ADC structures have been demonstrated as feasible alternatives. Mediumresolution time-interleaved SAR ADCs suffer from channel mismatch . Interleaved ADCs must use digital calibration or post-processing to achieve sufficient performance. For single-channel architectures, the non-binary [and passive charge sharing architectures work at several tens of MS/s and medium resolution (8 to 10 bits) with excellent power efficiency and small area.

An ADC with a medium sampling rate (a few tens to hundreds of MS/s) and a medium resolution is a necessary building block for 802.11/a/b/g wireless networks and digital TV applications where pipelined ADCs are extensively used. However, the pipelined architecture requires several operational amplifiers, which results in large power dissipation. Moreover, the restrictions for advanced CMOS processes make high performance amplifier design challenging. Drain-induced barrier lowering results in limited gain in short channel devices. Reduced supply voltage also limits the signal swing. With a limited signal swing, the sampling capacitance must be large enough to achieve a high signal-to-noise ratio (SNR), which leads to large current consumption. However, in SAR architectures, no component consumes static power if preamplifiers are not used. A SAR ADC can easily achieve a rail-to-rail signal swing, meaning that a small sampling capacitance is sufficient for a high SNR. The conversion time and power dissipation become smaller with the advancement of CMOS technologies. Since SAR ADCs take advantage of technological progress, for some high-conversion-rate applications, power- and area-efficient SAR ADCs can possibly replace pipelined ADCs in nanometer scaled CMOS processes. In SAR ADCs, the primary sources of power dissipation are the digital control circuit, comparator, and capacitive reference DAC network. Digital power

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consumption becomes lower with the advancement of technology. Technology scaling also improves the speed of digital circuits. On the other hand, the power consumption of the comparator and capacitor network is limited by mismatch and noise. Recently, several energy-efficient switching methods have been proposed to lower the switching energy of the capacitor network. The split capacitor method reduces switching energy by 37%, and the energy-saving method reduces energy consumption by 56%. Although these methods reduce the switching energy of capacitors, they make the SAR control logic more complicated due to the increased number of capacitors and switches, yielding higher digital power consumption. This paper proposes a capacitor switching method that allows less than 1-mW power consumption for a 10-bit 50-MS/s SAR ADC fabricated using 0.13- m CMOS technology . The proposed monotonic switching method reduces power consumption by 81% without splitting or adding capacitors and switches.The MTCMOS technique helps in reducing the static power in a wide range .The total capacitance in the DAC capacitor network is reduced by 50%.The switching has also been reduced in a higher level leading to low power consumption. In addition, the switching method improves the settling speed of the DAC capacitor network.This system also presents an improved comparator design to avoid the linearity degradation.

II.PROPOSED SYSTEM

A **successive-approximation ADC** is a type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation using a binarysearch through all possible quantization levels before finally converging upon a digital output for each conversion.

The successive-approximation analog-to-digitalconverter circuit typically consists of four chief subcircuits:

1. A sample-and-hold circuit to acquire the input voltage V_{in}.
2. An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR).
3. A successive-approximation register subcircuit designed to supply an approximate digital code of V_{in} to the internal DAC.
4. An internal reference DAC that, for comparison with V_{ref}, supplies the comparator with an analog voltage equal to the digital code output of the SAR

The successive approximation register is initialized so that the mostsignificant bit (MSB) is equal to a digital 1.

This code is fed into the DAC, which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in}, then the comparator causes the SAR to reset this bit; otherwise, the bit is left as 1.

Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the SAR at the end of the conversion (EOC).

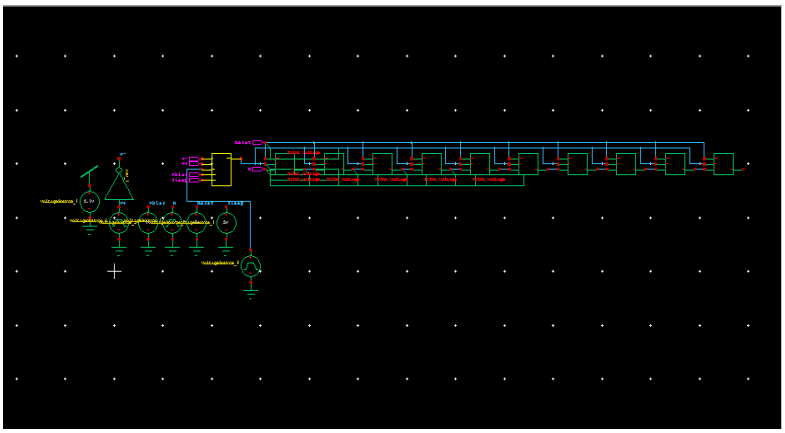

Fig 2.1 Proposed 10-Bit SAR ADC

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III.EXPERIMENTATION AND METHODOLOGY:

Software Required:

Fig 3.1Tanner EDA

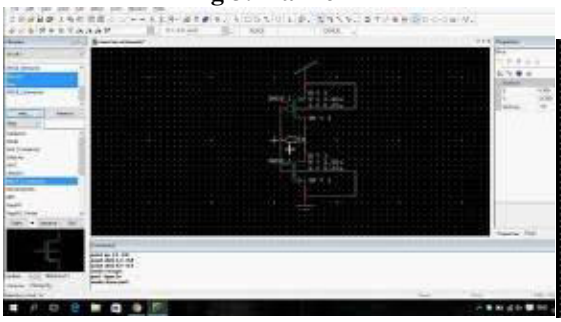


Fig 3.2 S-Edit

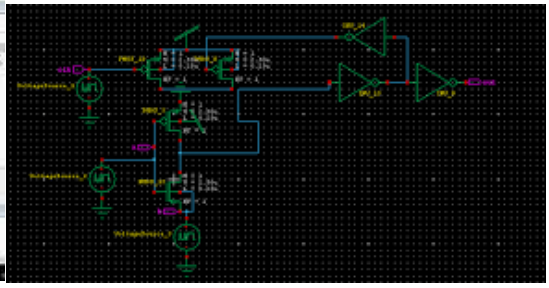


Fig 3.3 WEdit

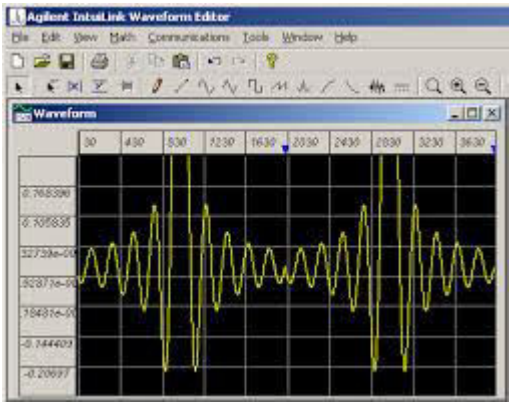
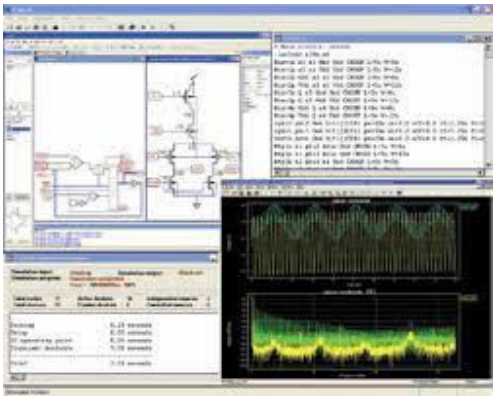


Fig 3.4 Tspice



Design and Simulation of a High Speed CMOS Comparator:

The double tail comparator offers a large current in the regenerative stage for fast regeneration and enables less current in the input differential stage to reduce offset.

During the reset phase when *Clk* =0, nmos transistor NMOS_5 is off or in cut-off mode, nmos transistors NMOS_3 and NMOS_4 are off whereas pmos transistors PMOS_1 and PMOS_2 are on, these pmos transistors will charge the drains of PMOS_1 and PMOS_2 transistor towards *DD V* . And subsequently NMOS_6 and NMOS_9 will cause the output nodes out+ and out- to discharge towards ground since *Clkb* =1 so pmos transistor PMOS_11 will be in cut-off mode.

During the regeneration phase when *Clk* = *DD V* the tail transistors NMOS_5 and PMOS_11 will turn on and the voltages at the drain terminals of PMOS_1 and PMOS_2 drop down. Nmos transistors NMOS_3 and NMOS_4 are on whereas pmos transistors PMOS_1 and PMOS_2 are off.

The transistors NMOS_6 and NMOS_9 are then used to pass the differential voltage from the input nodes to the re-generating stage. The cross coupled inverters start to re-generate the differential voltage as NMOS_6 and NMOS_9 can't clamp the outputs to ground.

The design is simulated using 0.25µm CMOS Technology using Tanner EDA Tools, with a 1.0 V supply.
Sleep Circuit is connected with PMOS_7 and NMOS_7.Sleep is directly connected to PMOS_7 and Sleep is given to a NOT Gate and hence sleep inverse is connected to NMOS_7.

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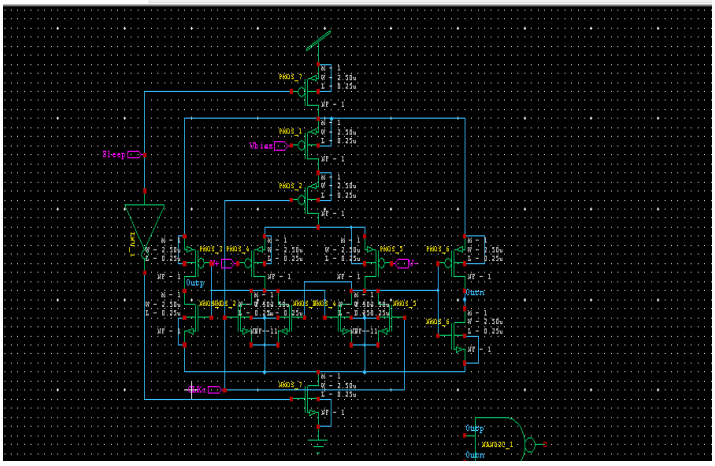

Fig 3.5 High Speed CMOS Comparator

Design Process of this Work:

A high speed latched comparator using positive feedback based back to back latch stage, suitable for pipelined Analog to Digital converter, with reduced delay and high speed is proposed.

During the RESET PHASE, when *Clk* is LOW (*Clk* =0), transistor NMOS_3 is in off state and pmos transistors PMOS_3, PMOS_9, PMOS_4, PMOS_10 are in on state.

Transistors NMOS_1 and NMOS_2 are in cutoff mode. Switch transistors PMOS_3,PMOS_9, PMOS_4, and PMOS_10 will charge the drains of transistors NMOS_ 1 and NMOS_2 and the output nodes Outp and Outn towards *DD V* .During the REGENERATION PHASE,*Clk* is HIGH (*Clk* =1)

ADC ARCHITECTURE

To achieve 10-bit accuracy, a fully differential architecture suppresses the substrate and supply noise and has good common-mode noise rejection. SAR ADCs usually use a binary-weighted capacitor array rather than a C-2C capacitor array for better linearity.

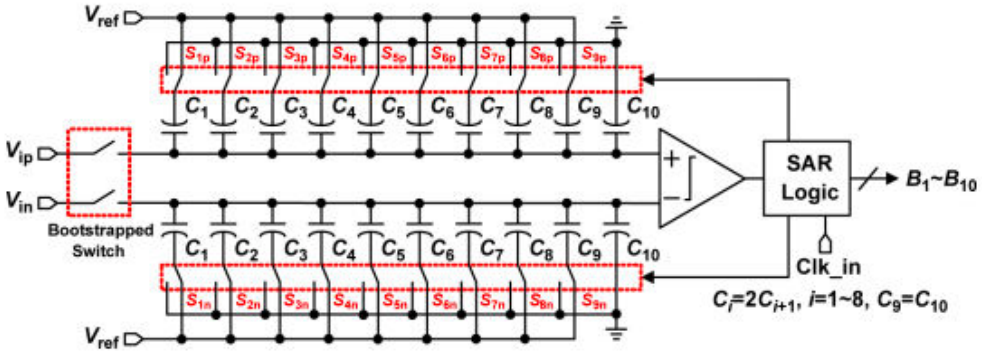

Fig 3.6 The proposed SAR ADC Architecture

The fundamental building blocks are the comparator, sample-and-hold (S/H) circuit, capacitor network, and successive approximation registers. In this charge-redistribution based architecture, the capacitor network serves as both a S/H circuit and a reference DAC capacitor array. Therefore, this architecture does not require a monolithic S/H circuit. Since this ADC is fully differential, the operation of the two sides is complementary. For simplicity, only the positive side of the ADC operation is described below. At the sampling phase, the bottom plates of the capacitors are charged to , and the top plates are reset to the common-mode voltage cm. Next, the largest capacitor is switched to and the other capacitors are switched to ground. The comparator then performs the first comparison. If it is higher than , the most significant bit (MSB) is 1. Otherwise, it is 0, and the largest capacitor is reconnected to ground. Then, the second largest capacitor is switched to . The comparator does the comparison again. The ADC repeats this procedure until the least significant bit (LSB) is decided. Although the trial-and-error search procedure is simple and intuitive, it is not an

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energy efficient switching scheme, especially when unsuccessful trials occur.The proposed SAR ADC, where the proposed switching procedure can be either upward or downward. For fast reference settling, i.e., discharging through n-type transistors, downward switching was selected in this ADC. The proposed ADC samples the input signal on the top plates via bootstrapped switches, which increases the settling speed and input bandwidth. At the same time, the bottom plates of the capacitors are reset to . Next, after the ADC turns off the bootstrapped switches, the comparator directly performs the first comparison without switching any capacitor. According to the comparator output, the largest capacitor on the higher voltage potential side is switched to ground and the other one (on the lower side) remains unchanged. The ADC repeats the procedure until the LSB is decided. For each bit cycle, there is only one capacitor switch, which reduces both charge transfer in the capacitive DAC network and the transitions of the control circuit and switch buffer, resulting in smaller power dissipation.

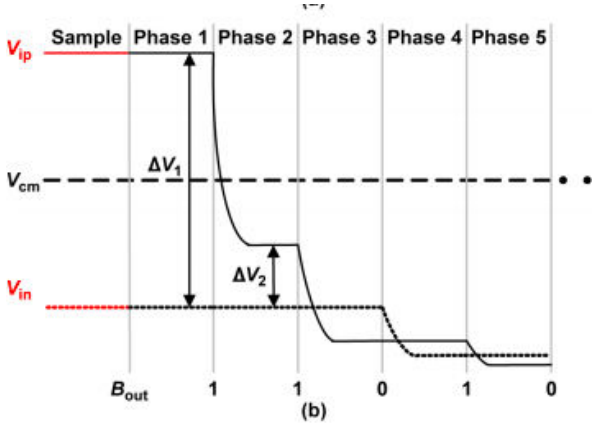

Fig 3.7 Waveform of the proposed architecture

One of the major differences between the proposed method. The proposed switching sequence does not require upward transition. At the same transistor size, the on-resistance of a nMOS switch is only about 1/3 that of a pMOS one. Having no upward transition speeds up the DAC settling. In addition, since sampling is done on the top plate, the comparator can do the first comparison without any capacitor switching. For an -bit ADC, the number of unit capacitors in a capacitor array is only half that of the conventional one. Fig. 4.6 shows 3-bit examples of the conventional and proposed switching methods. The conventional switching method is based on a trial-and-error search procedure. Fig. 4.5(a) shows all possible conversions. The quantitative energy consumption of each switching phase is also shown in the figure. The conventional switching sequence is efficient when all the attempts are successful, as in the upper cases. However, the switching sequence consumes a lot of energy when attempts are unsuccessful, as in the lower cases.After the sampling switches turn off, the comparator directly performs the first comparison without switching any capacitor. Therefore, the proposed switching sequence consumes no energy before the first comparison. In contrast, the conventional sequence is consumed before the first comparison. The subsequent switching sequence of the proposed method is also more efficient than that of the conventional one.For a 10-bit case, the conventional switching procedure consumes 1365.3 while the proposed switching procedure consumes only 255.5 . The proposed technique thus requires 81% less switching energy than that of the conventional one. Split capacitor and energy-saving switching methods provide only 37% and 56% reductions, respectively. The proposed method has the best power efficiency. The proposed architecture not only has the lowest switching power consumption but also the fewest switches and unit capacitors, which simplifies digital control logic. Therefore, the proposed ADC is very hardware efficient as well.Moreover the difference between the proposed and the existing circuit is that it has a MTCMOS (Multi Threshold CMOS) Technology.It has a sleep circuit which controls the static power.The existing circuit only controls the dynamic power

IV. RESULTS

The project is implemented and executed in S-edit , T-spice and W-edit . The power consumed in this project is 5.822418e-003 watts which are 50% less than the existing system. This also includes both static and dynamic power by using sleep in the circuit. Speed turns down to 4.04 seconds which is 2.23 seconds lesser. Switching is reduced by minimizing the MOSFET.

In this paper we are going to propose a low voltage low power SAR ADC Comparator. The proposed comparator works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz and consumes low power. To

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overcome the static power consumption issue two NMOS switches are used below the input transistors.This could be having low power consumption compared to the conventional comparator. Then also the delay could be reduced in this comparator.

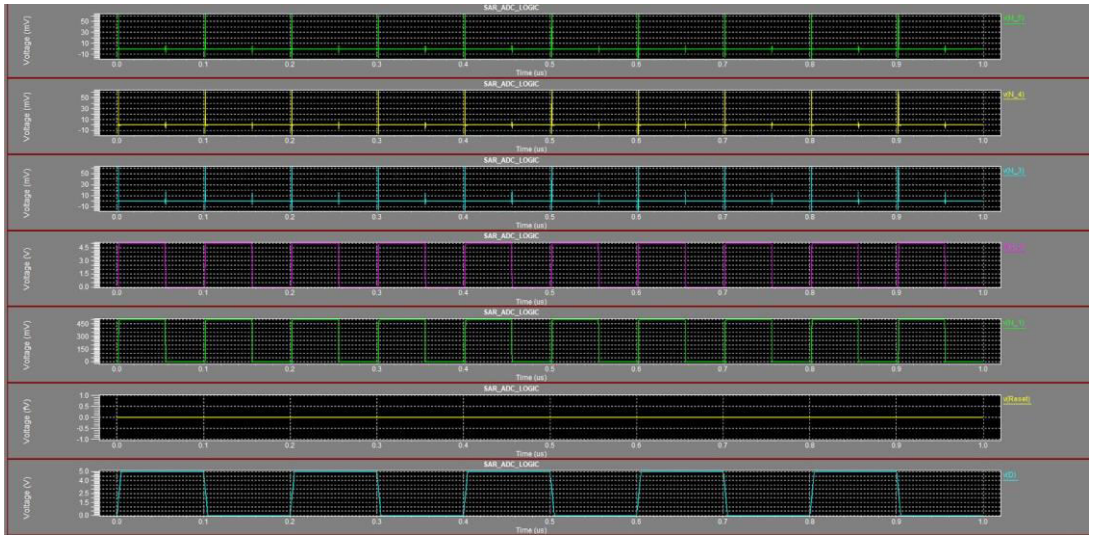

Fig 4.1 Result

V. CONCLUSION

In this project, a low-power SAR ADC based on area-efficient and low-energy switching scheme was presented. The proposed CDAC architecture can substantially reduce the total required capacitance while also reducing the switching energy and minimizing the quantity of controlled switches required. Moreover, the switching energy of the proposed CDAC was uniformly distributed over the entire range of the digital output codes compared with the conventional CDAC structure, the monotonic switching scheme, and Vcm based switching scheme. Finally, successive operations can be accomplished without increasing the complexity of the digitally controlled logic circuit. The prototype achieves a 50-MS/s conversion rate with power consumption of 5mW from 1.2 V supply. The resulting FOM is 21.68 fJ/conversion-step. Therefore, the proposed SAR ADC is very suitable for low-power applications

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