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Low Power Pulse Triggered Flip Flops using Clock Gating Cell

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ABSTRACT: A clock system consumes above 25% of the total system power. Flip-flops (FFs) are widely used as the basic storage element in all kinds of digital structures. The use of pulse-triggered flip-flops (P-FFs) in digital design provides better performance than conventional flip-flop designs. This paper presents the design of a new power-efficient implicit pulse-triggered flip-flop suitable for low power applications. Two important features are embedded in this flip-flop architecture. Firstly, the enhancement in width and height of trigger pulses during specific conditions gives a solution for the longest discharging path problem in existing P-FFs. Secondly, the clock gating concept reduces unwanted switching activities at sleep/idle mode of operation and thereby reducing dynamic power consumption. The power produced by the logic gates in combination with the clock circuit and the power exerted by the residual part of the FF are the two factors of power utilization within FFs. It is analyzed that all the signal transitions happen at the active operating mode because of the active clock and there will not be any transitions at the sleep/idle operating mode due to the inactive clock. But regrettably, unnecessary signal transitions happen at the sleep/idle operating mode because of the active behavior of the clock and thereby increasing the total power utilization.

KEYWORDS: - Flip Flop, Low Power, Clock Gating Cell, Pulse Trigger

I. INTRODUCTION

FFs are the widely used fundamental memory element in all types of advanced digital structures. It is additionally approximated that the power utilization of the clock system, is as high as 20%-40% of the complete system power as investigated [1, 2]. Thus, the contributions of FFs play a significant role in the speed, area and power performance of the total system. In power-constrained and speed improved applications, the P-FF shows preferable execution over regular FFs in master-slave configurations as stated [3]. P-FFs consist of a single latch structure and this made them more efficient in power and speed than master-slave FFs and Transmission Gate (TG) based FFs as stated [4]. Pulse generator and latches are the two essential subsystems in the design of a P-FF structure as investigated [5]. The pulse generator generates the trigger pulses at the transition clock edges. The data is latched from the input side to the output by the latch structure. Depending upon the trigger pulse generation method, P-FFs are classified as single and double edge-triggered types. In the case of single edge-triggered FFs, the trigger pulses are generated only at the rising or falling edges of the clock signals and in double-edge triggered FFs, the trigger pulses are generated at both rising and falling edges of the clock signals. Based on the connection of pulse generation logic and latch, P-FFs are named as implicit and explicit as stated [6]. In implicit case, the pulse generator is connected inside the latch. The connection of the pulse generator is outside to the latch in the case of explicit. It is evaluated that power efficiency is more for implicit P-FFs than explicit types. It is because the control of the discharge path happens in implicit P-FF but in the explicit P-FF pulses need to be generated physically as stated [7]. In any case, the latches of explicit P-FF have a favorable position to share the pulse generator. The overhead due to the external pulse generator can be diminished by the sharing.

In explicit P-FF dual-edge trigger mechanism can be executed effectively yet it is hard to employ in certain implicit designs as stated. The utilization of dynamic power legitimately relies upon the frequency of activity as proposed [8]. In dual-edge-triggered FFs, 50% of the frequency is diminished because of the latching of input at both edges of the clock. This reduced frequency increases power-saving as investigated [9]. In explicit, the height of the discharge path will be not as much as that of implicit P-FF this likewise prompts a decrease in power utilization. Both implicit and explicit P-FFs face the discharge path issue in the latch structure. This increases the size of the transistors and delay of the inverters used at the pulse generator to enlarge the width and height of trigger pulses for the sufficient capturing of data as stated. This is the pulse width control issue. The pulse width control issue and unwanted switching activities will affect the speed and power performance of the P-FFs.

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II. LITERATURE REVIEW

Sonam Gour et al. [1], in the process of large scale integration lot of transistors are implemented in a very minimum area. Combinational logic has very useful in quantum and many industrial designs. Reducing the power and delay is the principle object in VLSI design. Suppressing sub-threshold leakage current in large scale integration is essential for achieving green computing and facilitating the more usage of power electronics. In this paper the shift register is implemented with or without MTCMOS technique. The Cosmos Scope tool is used to analyze the power delay with the simulation in HSPICE. The Shift Register is fabricated by using the 32nm and 45nm BPTM model file. With the help of MTCMOS technique in Shift Register a reduction in leakage power is 44% in 32nm with the applied voltage of 0.7V and 57% in 45nm with the applied voltage of 0.9V. Energy is reduced by the 5% for 0.7V for 32nm and 21 % for 0.9V at 45nm.

Bhupendra Sharma et al. [2], for low power, high speed design of flip-flop having less number of transistors and only one transistor being clocked by short pulse train which is true single phase clocking (TSPC) flip-flop. Compared to Conventional flip-flop, it has 5 Transistors and one transistor clocked, thus has lesser size and lesser power consumption. It can be used in various applications like Shift Registers, Counters, Digital VLSI clocking system, Buffers, Microprocessors etc. The analysis for various flip flops for power dissipation and propagation delays at 0.18µm, 0.12µm and 90nm technologies is carried out. The leakage power increases as technology is scaled down. The leakage power is reduced by using best technique among all run time techniques viz. MTCMOS. Thereby comparison of different conventional flip-flops and TSPC flip-flop in terms of Power consumption, Propagation delays, Product of Delay-Power (PDP), Area and Leakage power with Microwind simulation results is presented. Applications like Shift Registers, Counters are implemented in terms of Power consumption, Propagation delay and Leakage power.

Karthik. B et al. [3], high-performance flip-flops are analyzed and classified into two categories: the conditional precharge and the conditional capture technologies. This classification is based on how to prevent or reduce the redundant internal switching activities. A new flip-flop is introduced: the conditional discharge flip-flop (CDFF). It is based on a new technology, known as the conditional discharge technology. This CDFF not only reduces the internal switching activities, but also generates less glitches at the output, while maintaining the negative setup time and small -to- delay characteristics. With a data-switching activity of 37.5%, the proposed flip-flop can save up to 39% of the energy with the same speed as that for the fastest pulsed flip-flops.

G. Prakash et al. [4], Quantum-dot Cellular Automata (QCA) is emerging nanotechnology that can represent binary information using quantum cells without current flows. It is known as a promising alternative of Complementary Metal–Oxide Semiconductor (CMOS) to solve its drawbacks. On the other hand, the shift register is one of the most widely used practical devices in digital systems. Also, QCA has the potential to achieve attractive features than transistor-based technology. However, very small-scale and Nano-fabrication limits impose a hurdle to the design of QCA-based circuits and necessitate for fault-tolerant analysis is appeared. Therefore, the aim of this paper is to design and simulate an optimized a D-flip-flop (as the main element of the shift register) based on QCA technology, which is extended to design an optimized 2-bit universal shift register. This paper evaluates the performance of the designed shift register in the presence of the QCA fault. Collected results using QCA Designer tool demonstrate the fault-tolerant feature of the proposed design with minimum clocking and area consumption.

Namrata Joshi et al. [5], recent VLSI technologies to design any circuit main prime factors are speed and power with downscaling of chip size.Shift registers are used for temporary storage of data in processors and sequential circuits. The paper enumerates an efficient design of shift register in terms of speed and power consumption using 180 nm technology.Serial In Serial Out (SISO) and Serial In Parallel Out (SIPO) shift register has been designed using BICMOS logic. These shift registers have implemented by master slave D flip flop as a storage element.Cadence EDA tool has used to implement the proposed shift registers. Proposed design results compared with conventional design results implemented using CMOS technologyand concluded that proposed design has low power consumption and high speed compared to conventional design.

Anjan Kumara et al. [6], multi-threshold CMOS (MTCMOS) is a well known strategy to diminish the standby current when the circuit is non operatory mode. However conventional MTCMOS strategies for limiting standby current can't be specifically utilized as a part of sequential circuit for two reasons (i) Present ground fluctuation noise during standby mode to dynamic mode move and (ii) Absence of information maintenance ability during standby mode. Here an analysis of ground fluctuation noise because of active mode move in sequential MTCMOS design is proposed. An inventive information saving MTCMOS configuration is proposed, which not only focusing on the lessening of peak

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amplitude of ground fluctuation noise during mode change will likewise give an approach to control the sub-threshold current in standby mode. The proposed MTCMOS design will have stepwise turning on capabilities and also an extra hardware to additionally decrease the quick current moving through high th V transistors during move from Dream mode to Dynamic mode. Its extra current control circuits give higher decrease in peak amplitude of ground fluctuations noise (up to 98.4%) when contrasted with other comparative techniques.

Dr. B. Karthik et al. [7], high-performance flip-flops are analyzed and classified into two categories: the conditional precharge and the conditional capture technologies. This classification is based on how to prevent or reduce the redundant internal switching activities. A new flip-flop is introduced: the conditional discharge flip-flop (CDFF). It is based on a new technology, known as the conditional discharge technology. This CDFF not only reduces the internal switching activities, but also generates less glitches at the output, while maintaining the negative setup time and small -to- delay characteristics. With a data-switching activity of 37.5%, the proposed flip-flop can save up to 39% of the energy with the same speed as that for the fastest pulsed flip-flops

Roshni Oommen et al. [8], large scale integration process, lots of transistors are implanted on a single silicon substrate for setting up of intricate circuits. Accordingly, major problem of power dissipation comes into the picture. Linear Feedback Shift Register (LFSR) is a commonly used pseudo random sequence generator to generate random 1s and 0s. It is used in applications such as Built-in-self test (BIST), cryptography etc. LFSR's are having high level of fault coverage so they are used in several coding schemes. In this paper, LFSR is implemented using Complementary Metal Oxide Semiconductor (CMOS), Gate Diffusion Input (GDI), modified GDI(mGDI) and Multi Threshold CMOS (MTCMOS) techniques in Cadence Virtuoso using 180nm technology. Simulations of these circuits are done and different parameters like power, propagation delay and area are compared. mGDI gives a reduction of 30%, 39%, 49% with respect to CMOS in power, delay and area respectively and a reduction of 6%, 14% with respect to GDI in power, and delay respectively. Thus, mGDI LFSR design can be employed for low power testing.

Roshan R Chavhan et al. [9], Low power and less area in an electronics devices having very high demand in the world because of user want to fast mobility with less power consumption and also not compromising with the area. By using multiple stages of flip flop and latches to compare area and power. The main objective to designing a flip-flop with respective pulse latches is consume less power. For solving timing problem a new technique is use, in which of pulsed latches and multiple non-overlapping delayed version of pulsed clock signal are uses. In this system, single clock pulse signal uses and combine this latches to multiple sub-shifter register and further for only a limited period of time storage latches. In this minimum number of clock pulse signal use by groping latches to multiple sub shift register and using short-term storage latches. 8, 16, 32, upto 256-bit shift register using pulsed latches was fabricated using 180nm cmos process with vdd is 1.8V. This proposed system implementation by using cadence tool.

Rakesh Biswas et al. [10], limited size and power budgets of space-bound systems often contradict the requirements for reliable circuit operation within high-radiation environments. In this paper, we propose the smallest solution for soft-error tolerant embedded memory yet to be presented. The proposed complementary dual-modular redundancy (CDMR) memory is based on a four-transistor dynamic memory core that internally stores complementary data values to provide an inherent per-bit error detection capability. By adding simple, low-overhead parity, an error-correction capability is added to the memory architecture for robust soft-error protection. The proposed memory was implemented in a 65-nm CMOS technology, displaying as much as a 3.5×1 smaller silicon footprint than other radiation-hardened bitcells. In addition, the CDMR memory consumes between 48% and 87% less standby power than other considered solutions across the entire operating region.

III. METHODOLOGY

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate [7]. Without generating pulse signals explicitly, implicit type P-FFs are in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an n-bit register). In this brief, we will thus focus on the explicit type P-FF designs only. To provide a comparison, some existing P-FF designs are reviewed first. Fig. 1 shows a classic explicit P-FF design, named data-close to-output (ep-DCO) [7].

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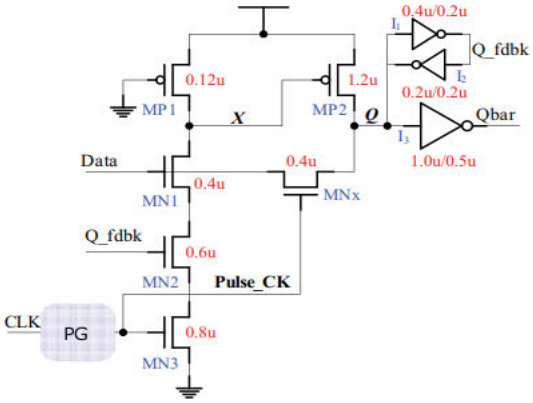

Fig. 1: Schematic of the P-FF design

It contains a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation.

FF Based Clock Gating Cell

In FF based clock gating, the control component used is a FF. During the negative half cycle of the clock signal, the difference of Enable will be mirrored on the output of the FF. If the generated output of the FF is HIGH, the sequential circuit is triggered by the clock. The duration of the sleep period is longer in FF based clock gating compared to latch based design. It means there is a greater chance to miss the change that happens on the Enable signal. There are two types of FF based clock gating cells. One is without the Reset signal, which is shown in Figure 2, and the second is with Reset, which is shown in Figure 3 as stated [11, 12].

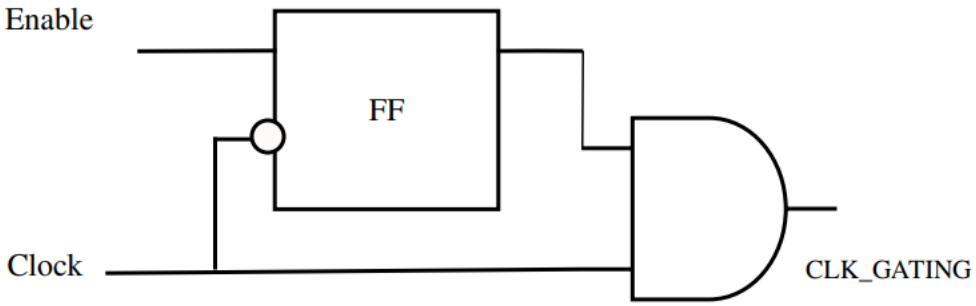

Fig. 2: FF Based Clock Gating Cell without Reset

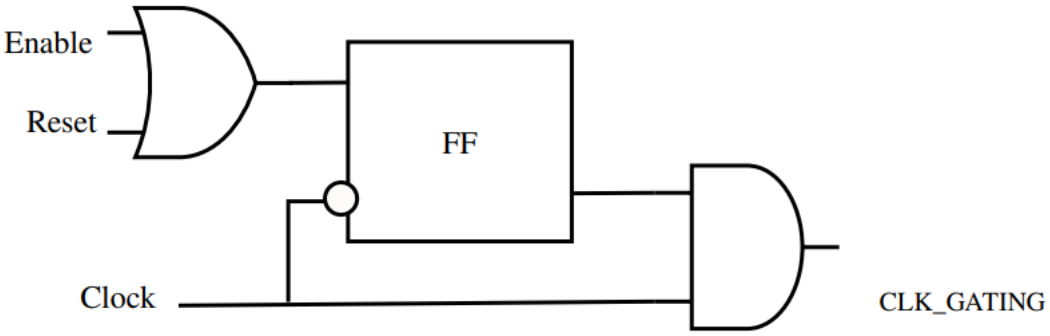

Fig. 3: FF Based Clock Gating Cell with Reset

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IV. CONCLUSION

The clock gating can be used to avoid the unwanted switching activity of the clock during sleep/idle mode of operation. The clock circuit is disabled by inactivating the NOT gates connected to the clock input of the P-FFs in the idle/sleep mode and thus take out both the clock circuit and the remaining circuit power. The key idea was to provide a signal feedthrough from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. Extensive simulations were conducted, and the results did support the claims of the proposed design in various performance aspects.

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