ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijircce.com

Vol. 7, Issue 1, January 2019

Design and implemented low power Conventional Wallace Multiplier in CMOS Technology

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ABSTRACT: Multiplier is an arithmetic circuit that is extensively used in DSP, microprocessors and communication applications like, FFT, Digital Filters etc. Today entire world is demanding compact and small digital devices which should perform fast with low power consumption. Multiplier is the basic building block in almost all digital devices and it impacts the speed, power and area of a device significantly reconfigurable 8x8 Wallace Tree multiplier using CMOS and GDI technology is designed in 180nm. Wallace Tree multiplier is efficient in power and regularity without increase in delay and area. The main idea is the generation of partial products in parallel using AND and or gates. The adding of partial products is reduced help of Wallace Tree which is hierarchically divided into levels. Therefore there will be a significant reduction in the power consumption, since power is provided only to the level that is involved in computation and the remaining two levels switched off.

I. INTRODUCTION

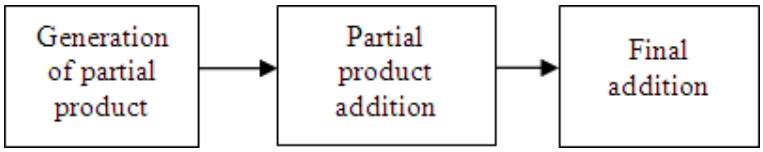

Fig.1.Block diagram of multiplier architecture

II. BASICS OF MULTIPLIERS

Multiplication is an operation that occurs frequently in digital signal processing and many other applications. However, multipliers occupy a much larger area and incur much longer delays than adders. Therefore it is imperative that special techniques be used to speed up the calculation of the product while maintaining a reasonable area.
The product is the result of multiplying the multiplicand to the multiplier. The multiplication operation is performed in two main steps. First is the partial product formation, which consists of AND-ing each bit of the multiplier with the multiplicand. Each successive partial product belongs one place to the left of the previous partial product. The second step is partial product accumulation, where the partial products are combined to form the result.

Application of Multipliers

- Used in digital signal processing operations such as filtering, convolution and analysis of frequency.
- Image processing.
- Arithmetic units in Microprocessors.
- Used in graphics and computation system.
- Cryptosystems

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2.1Types of Multiplier

Multipliers differ in terms of partial product generation and partial product addition to produce the final result . Many researchers have tried to design multipliers which offer either of the following- low power consumption, high speed, regularity of layout and hence less area or even grouping of them in multiplier. However, the two design criteria are often in conflict and that improving one particular aspect of the design constrains the other. Many algorithms have been introduced in search of fastest multiplier. Based on these algorithm there are different types of multiplier

- Array multiplier
- Wallace Tree Multiplier
- Dadda Multiplier
- Modified Booth multiplier.
- Hierarchical Array of Array Multiplier
- Vedic multiplier

- **Modified Booth Multiplier**

Block diagram of the Modified Booth multiplier is shown infig3.6. This circuit takes two 8-bit binary numbers and produces the 16-bit product. The multiplier, X[7:0], is divided into four groups: 0, X0, X1; X1, X2, X3; X3, X4, X5; X5, X6, X7.

Each of these groups is passed into a Booth encoder, which outputs bits corresponding to the operations described in table 3.1. Each group of these selection bits are sent to a Booth decoder block, which outputs the appropriate partial product term based on the selected operation. These partial products are then sign extended so that sign bits are taken in to account during the summing.

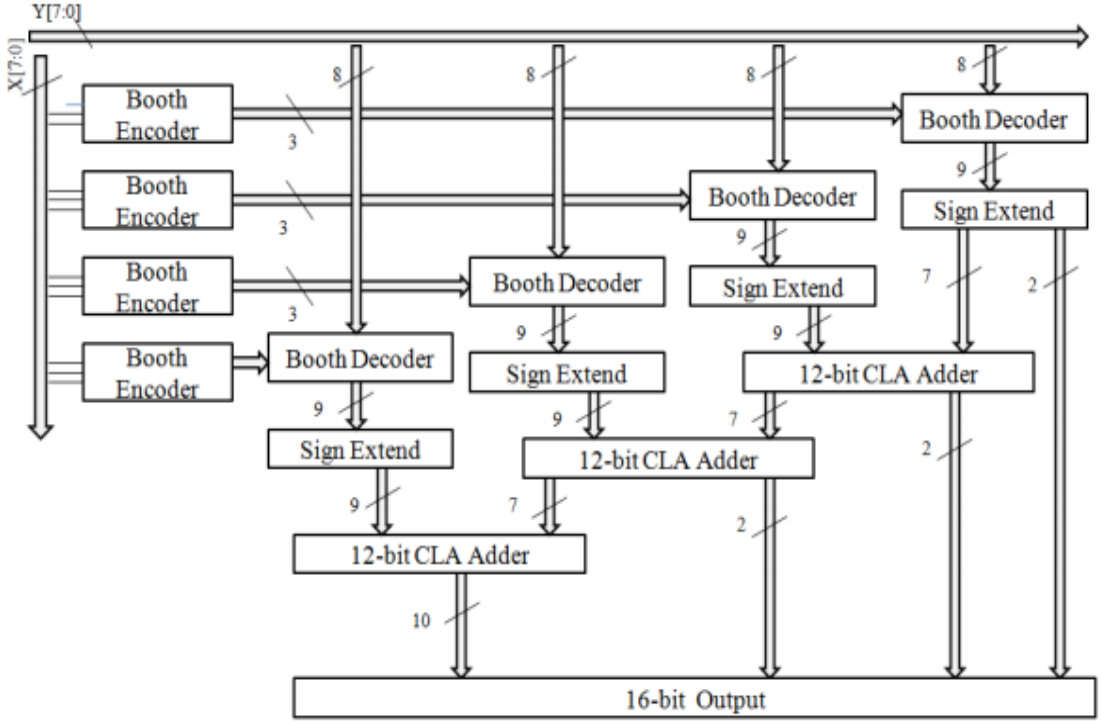

Fig 2: Modified Booth Multiplier

Finally, the canonical shift and add multiplication is implemented using 12-bit carry look ahead adders (CLA). The first two bits of each partial product are passed directly to the output to account for the shifting. A standard array multiplier

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would typically require 8partial products, and thus 8 adders. However, this implementation reduces the number of partial products to only four, significantly improving speed. Furthermore, the CLA provides another speed boost to the system.

4-BIT MULTIPLIER

After designing 2 x 2 multiplier, 4-bit multiplier is also designed using wallace tree method as shown in fig

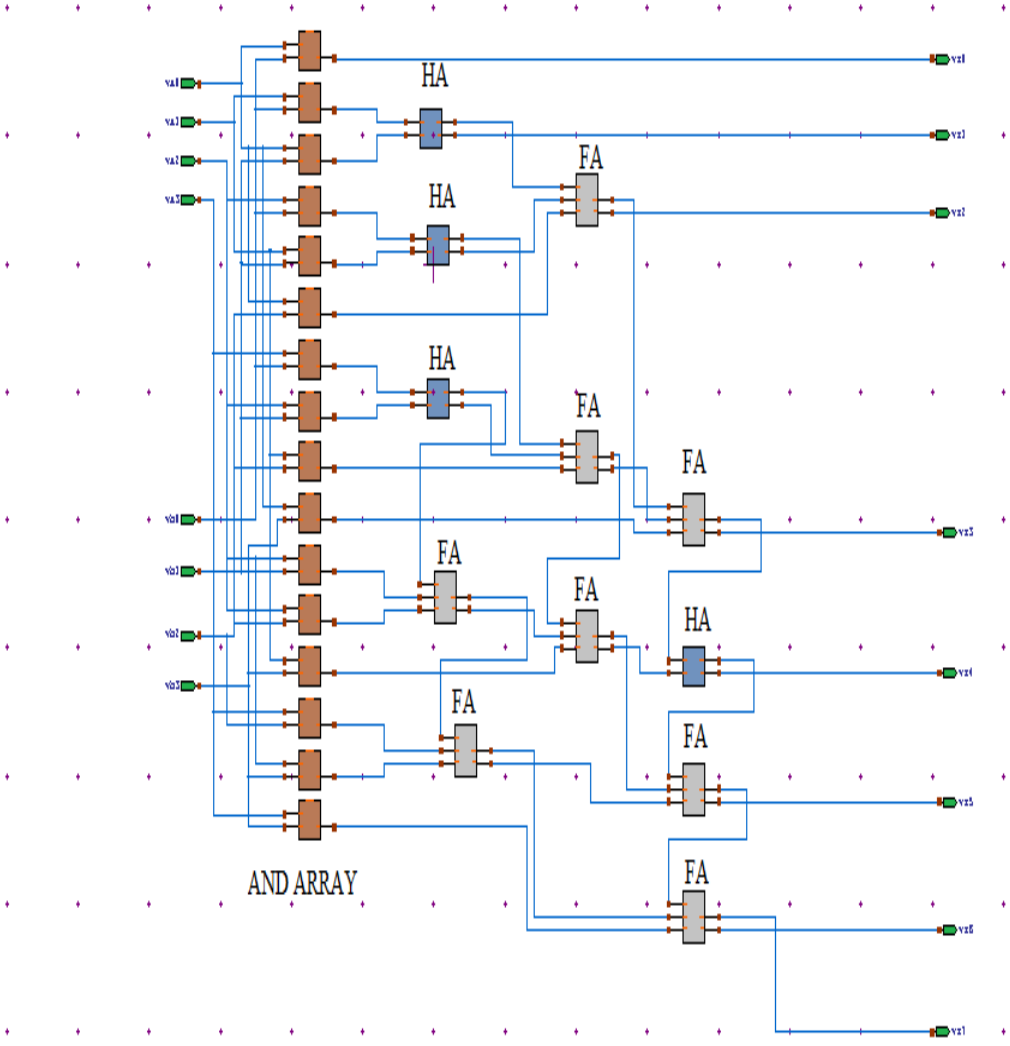

Fig 3: 4-Bit Multiplier

8-BIT MULTIPLIER

8x8 bit multiplier architecture based on Wallace Tree is shown , which is efficient in terms of power and regularity without increase in delay and area. The idea involves the generation of partial products in parallel using AND gates .The addition of partial products is done using Wallace tree, which is hierarchal, divided into levels. There will be a reduction in the power consumption, since power is provided only to the level that is involved in computation. Hardware realization of 8 x 8 multiplier is shown in fig.

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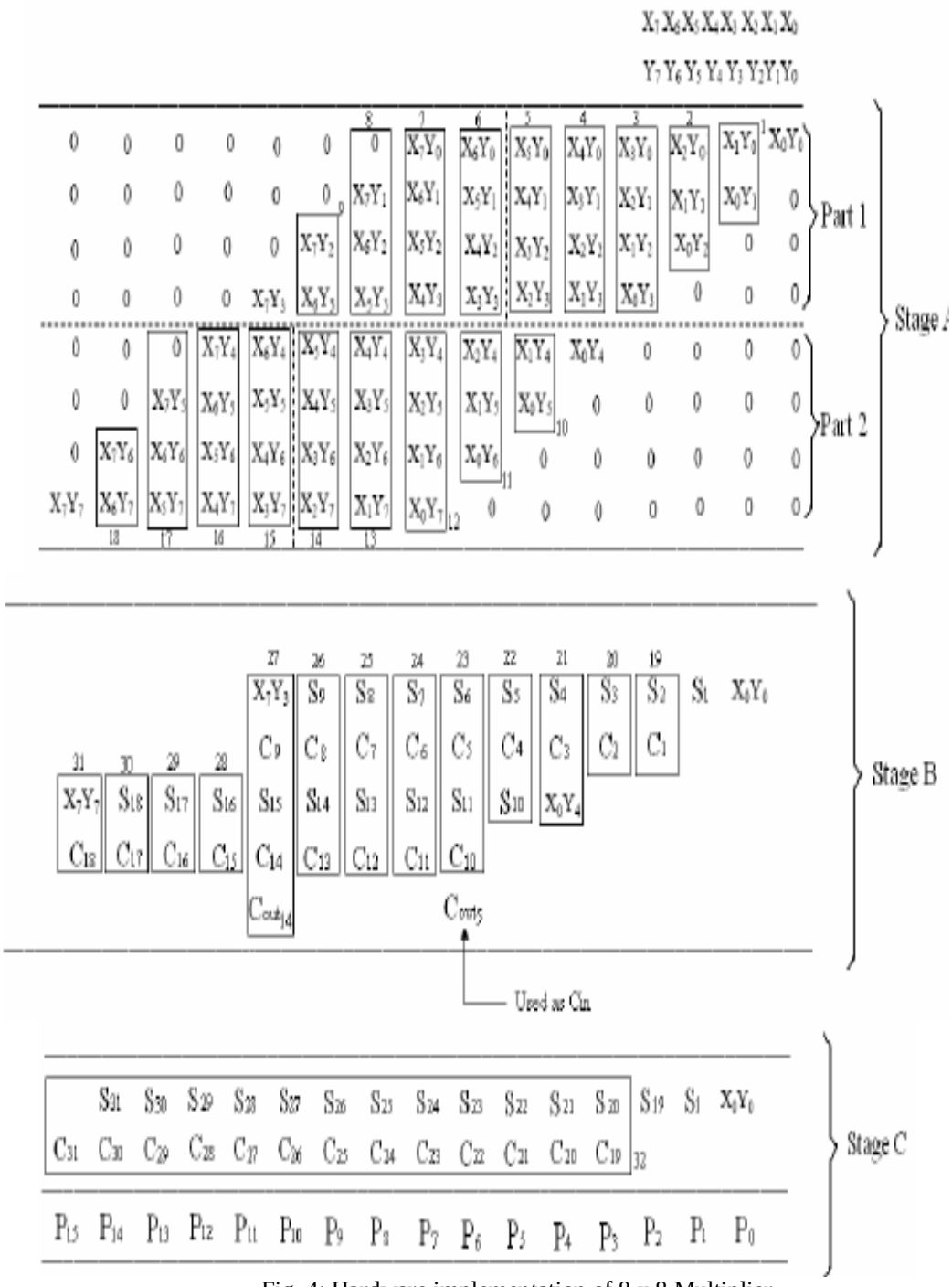

Fig 4: Hardware implementation of 8 x 8 Multiplier

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Schematic diagram of GDI based 8 x 8 multiplier is shown in fig 4.19.

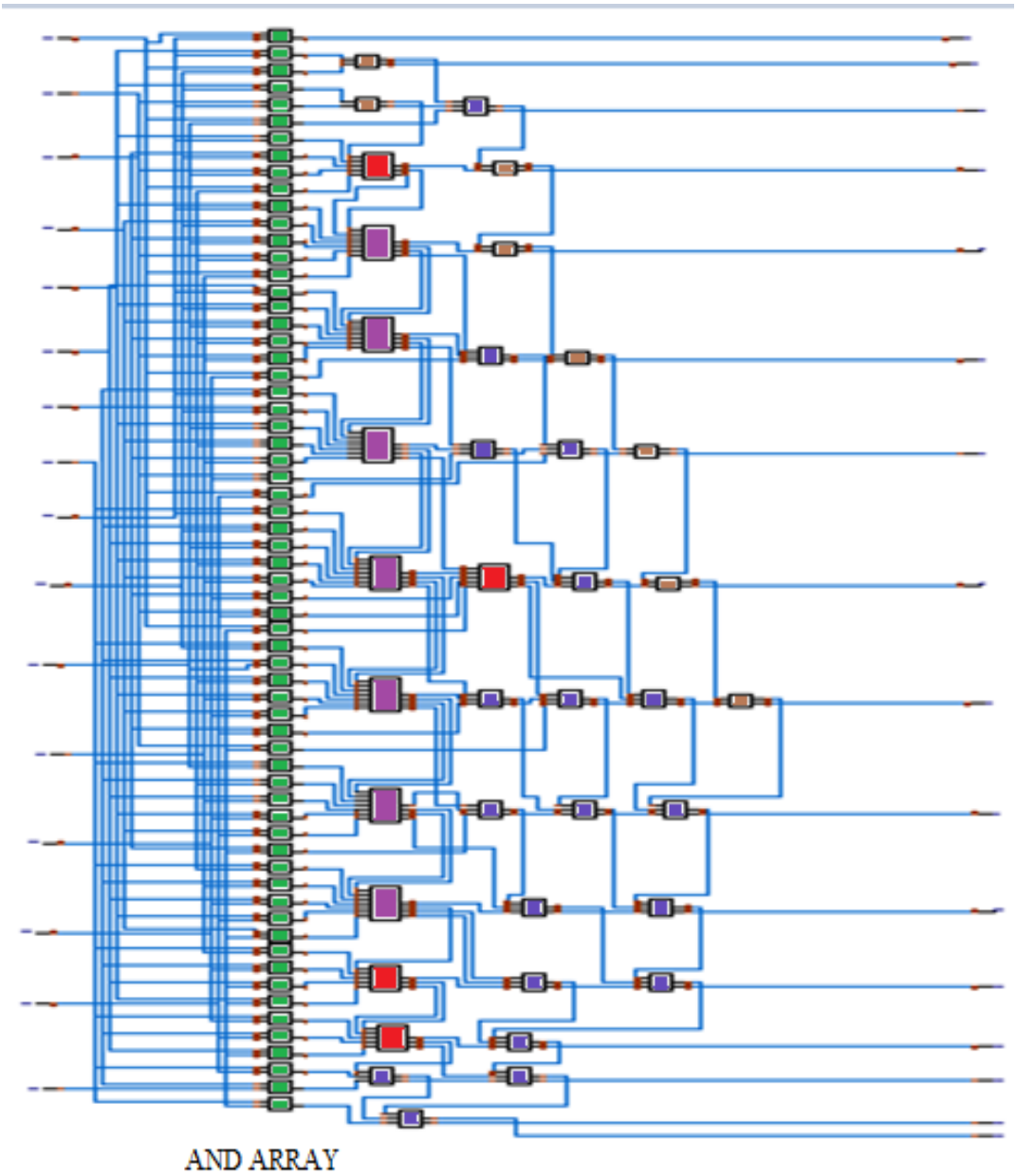

Fig 5: 8-Bit Multiplier

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III. SIMULATION RESULT AND ANALYSIS

4-BIT MULTIPLIER

Simulated waveform of 4-bit GDI based multiplier is shown in fig 5.12. Multiplier and multiplicand inputs each are of 4 bits. After multiplication 8-bit partial products are generated. Here both CMOS and GDI based 4 x 4 multiplier are designed and analysed. GDI based multiplier gives better results in terms of propagation delay, power dissipation and area by using transistor count.

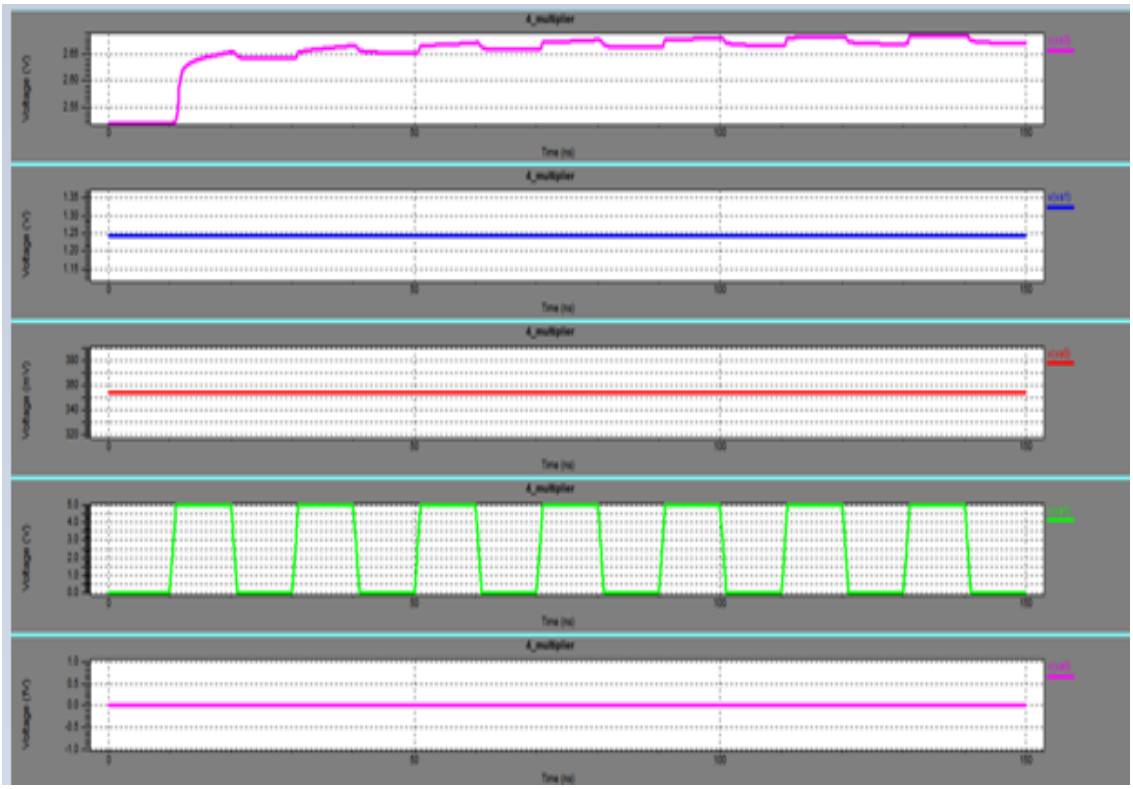

Fig 6 : Waveform of 4-bit GDI based Multiplier

Propagation delay and power dissipation of both 4-bit CMOS multiplier and 4-bit GDI multiplier is listed below in table 1and table 2 respectively.

Table 1
Parameter of 4-bit CMOS multiplier

Vdd (V)	Delay (ns)	Power Dissipation (mW)
1.8	0.185	5.7252
1.6	0.225	4.4303
1.4	0.289	2.6030
1.2	0.359	1.5436
1.0	0.411	0.7801

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Table 2
Parameter of 4-bit GDI multiplier

Vdd (V)	Delay (ns)	Power Dissipation (mW)
1.8	0.012	5.6982
1.6	0.056	4.2103
1.4	0.075	2.3864
1.2	0.195	1.3488
1.0	0.278	0.6865

3.1 8-BIT MULTIPLIER

Simulated waveform of 8-bit GDI based multiplier is shown in fig 5.13. Multiplier and multiplicand inputs each are of 8 bits. After multiplication 16-bit partial products are generated.

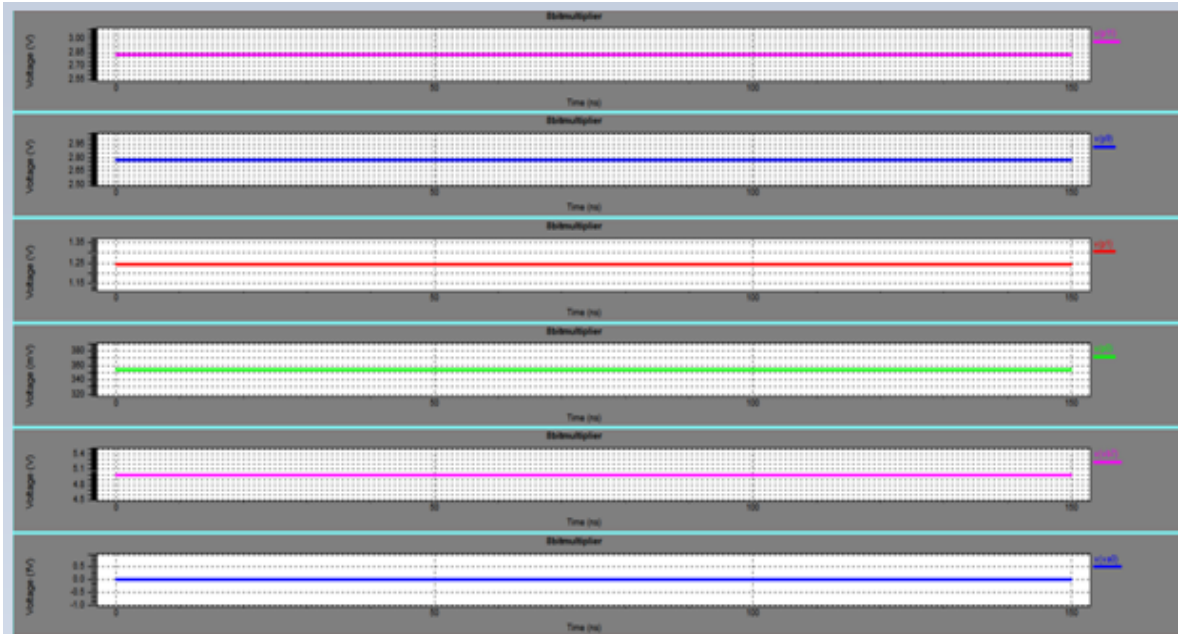

Fig 7 : Waveform of 8-bit GDI based Multiplier

Propagation delay and power dissipation of both 4-bit CMOS multiplier and 4-bit GDI multiplier is listed below in table 3 and table 4 respectively.

Table 3
Parameter of 8-bit GDI multiplier

Vdd(V)	**Delay(ns)**	**Power Dissipation (mW)**
1.8	0.02	8.854
1.6	0.40	8.395
1.4	0.65	7.975
1.2	0.72	7.414
1.0	0.82	6.756

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Table 4
Parameter of 8-bit CMOS multiplier

Vdd(V)	Delay(ns)	Power Dissipation(mW)
1.8	0.17	9.64
1.6	0.56	9.19
1.4	0.70	8.57
1.2	0.80	7.84
1.0	0.95	6.95

IV. CONCLUSION

Multiplier is one of the most important components of many digital signal processing, general purpose processing, image processing and other digital application. Multiplier performance can be measured by using performance factors like Power, Delay and area. In efforts to identify the most efficient multiplier, this research makes the following conclusions.

The GDI based wallace tree multiplier occupies smaller silicon area with higher resolution than the conventional wallace tree multiplier. Various parameters like delay and power dissipation of other circuits are also calculated with respect to different power supply. Result shows that Power dissipation and delay of GDI based Wallace tree multiplier at 1.8V power supply is 8.8mW and 0.02 nS respectively and total transistor count is 912.

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