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Comparative Analysis and FPGA Implementation of Vedic Multiplier for various Bit Lengths using Different Adders

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ABSTRACT: This paper describes the design of Vedic Multiplier based on Urdhva Trigbhyam technique of multiplication. It is one of the ancient Vedic sutras for multiplication it means vertical & crosswise. The paper compares the design of Vedic Multiplier for different bit lengths based on Ripple Carry Adder & Kogge Stone Adder. For the highly efficient processor, multiplier plays an important role. It has been found that Kogge Stone Adder is fastest Parallel Prefix Adder, hence the delay in Vedic Multiplier based on Kogge Stone Adder is less as compared to that based on Ripple Carry Adder.The delay for 16bit Vedic Multiplier using Ripple Carry Adder has been found to be 29.051ns whereas using Kogge Stone Adder has been found as 27.499ns. The design has also been compared based on levels of logic, memory utilization. The proposed algorithm has been designed using Verilog HDL. Implementation has been done using Xilinx 14.4 with family Spartan6, device as xc6slx45, package csg324 with speed grade of -3.

KEYWORDS: KSA, RCA, Urdhva Trigbhyam, Vedic Multiplier

I. INTRODUCTION

Multiplication is an important function in many mathematical computations. It is nothing but a sequence of additions carried out on partial products as suggested by Jagadguru Swami [1]. The VLSI design is considered in terms of logic utilization, power, area, delay, levels of logic, total memory usage. A good multiplier is designed considering all these factors. Here the multiplier has been designed using URDHVA TRIGBHYAM sutra one of the 16 Vedic sutras based on ancient Vedic mathematics [2]. The adders used are Ripple Carry Adder in which the carryout of next stage depends on carryout of previous stage & Kogge Stone Adder which is the fastest parallel prefix adder.

II. URDHVA TRIGBHYAM

It means vertical and crosswise multiplication. It requires less computation time as suggested by M. Poornima [3] than other Vedic sutras like Ekadhikena Purvena, Nikhilam, Navatascara-mam Dasatah etc .It is employed as one of the ancient Vedic multiplication technique [4]. A general method of multiplication is as shown below :-

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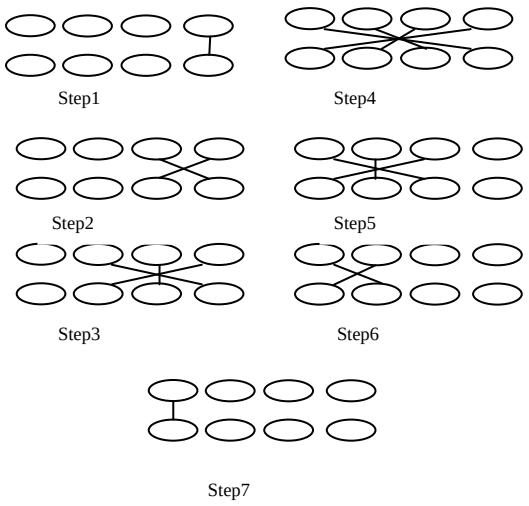

Fig. 1- 4 bit Vedic Multiplication

The method shown in fig. 1 is for 4 bit Vedic multiplication as the number of bits increases area and gate delay increases at a fader rate in Urdhva multiplication as compared to other techniques, therefore the techniques has been employed here for Vedic multiplication.

III. ADDERS

A. *Ripple Carry Adder*

It is a type of digital adder [5, 6] used in many logic circuits. In this adder the carry and sum bits are produced alongside. The carryout of the next stage depends on the carryout of previous stage. The carryout of one stage acts as carry in of the next stage. Fig. 2 shows the basic hierarchical block diagram of 4 bit adder using 1 bit adder.

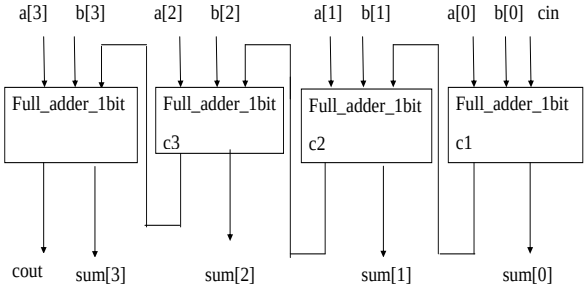

Fig. 2- 4 bit Ripple Carry Adder

B. *Kogge Stone Adder*

It is one of the fastest parallel prefix adder. It generates the carry signals in O(log n) time[7-8]. It uses group generate and propagate functions. It uses three stages

i) Pre-processing
ii) Carry look-ahead network
iii) Post-processing

In Pre-processing stage, propagate (p) and generate (g) functions are calculated as

p=a xor b;
g=a and b;

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In Carry look-ahead network, group propagate and generate functions are calculated as:-

cp[i]=p[i] and p[i-1]
cg[i]=g[i] or (g[i-1] and p[i])

In Post-processing network, sum and cout is calculated

sum[i]=p[i] xor cg[i-1]

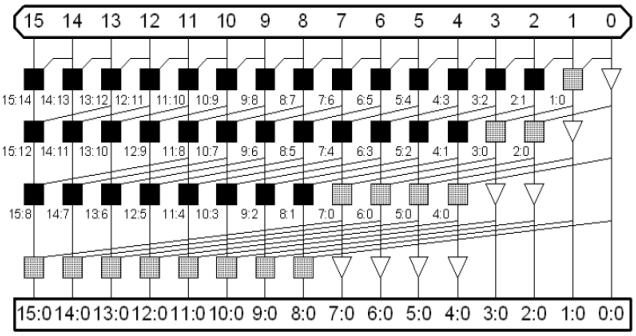

Fig. 3 - 16-bit Kogge Stone Adder network

IV. IMPLEMENTATION

A. *4 Bit Vedic Multiplier*

Firstly the 2 bit Vedic Multiplier has been designed using two half adders[9, 10] & four and gates. Next the four 2 bit Vedic Multipliers and three Ripple Carry Adders & also by Kogge Stone Adders each of 4 bit, 6 bit, 6 bit are needed for design of 4 bit Vedic Multiplier. The schematic could be as shown:-

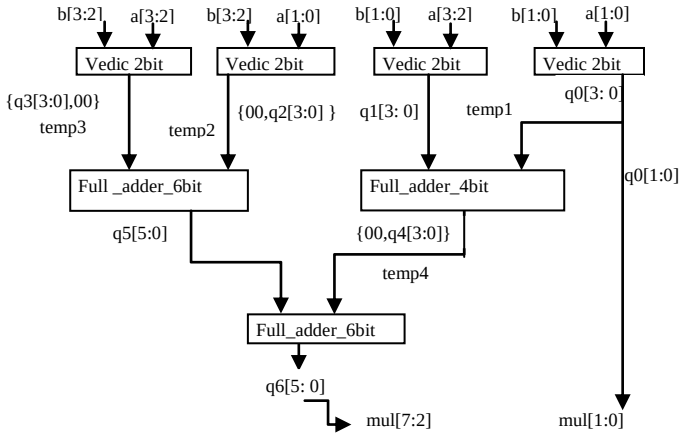

Fig. 4(a) - Schematic for 4 bit Vedic Multiplier

B. *8 Bit Vedic Multiplier*

The 8 bit Vedic Multiplier has been designed using four 4 bit Vedic Multipliers and three Ripple Carry Adders as well as Kogge Stone Adders each of 8 bit, 12 bit, 12 bit as shown:-

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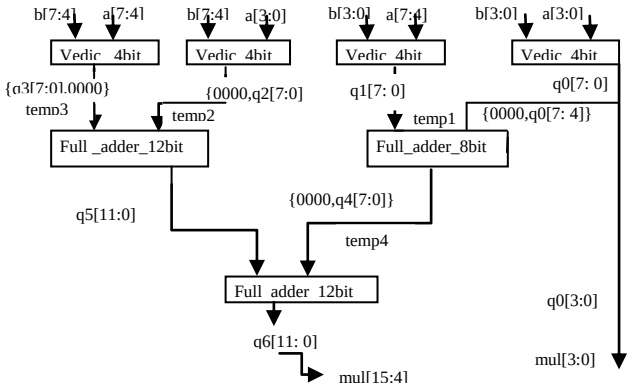

Fig. 4(b) - Schematic for 8 bit Vedic Multiplier

C. *16 Bit Vedic Multiplier*

The 16 bit Vedic Multiplier has been designed using four 8 bit Vedic Multipliers and three Ripple Carry Adders as well as Kogge Stone Adders each of 16 bit, 24 bit, 24 bit. It is found that as the number of bits increases in the multiplier the performance of the system increases. Therefore the schematic for the 16 bit Vedic Multiplier could be as shown:-

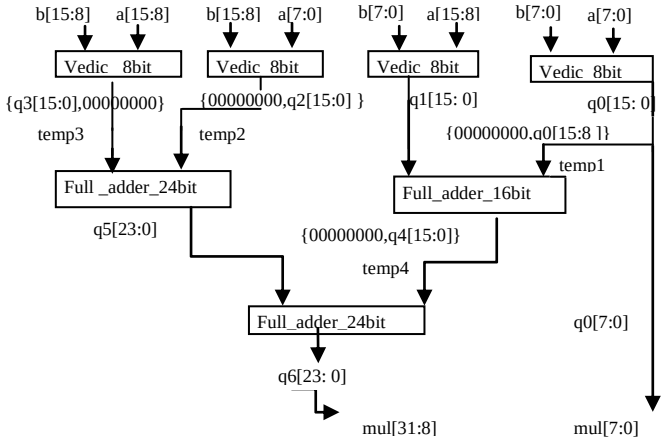

Fig. 4(c) - Schematic for 16 bit Vedic Multiplier

V. SYNTHESIS & SIMULATION

The synthesis of Vedic Multiplier has been performed using Xilinx 14.4 ISE & simulation has been done using Isim simulation tool on Spartan6 FPGA. The family is spartan6, device xc6slx45, package csg324, speed -3.

The technology Schematic of 8 bit Vedic Multiplier using RCA which requires more computational time compared to KSA has been shown in fig 5 (a) below:-

The technology Schematic of 8 bit Vedic Multiplier using which employs more complex hardware however speed grade is superior compared to RCA has been shown in fig 5(b) below:-

The simulation view of 8 bit Vedic Multiplier which displays the result of multiplying two 8 bit numbers has been shown in fig 5(c) below:-

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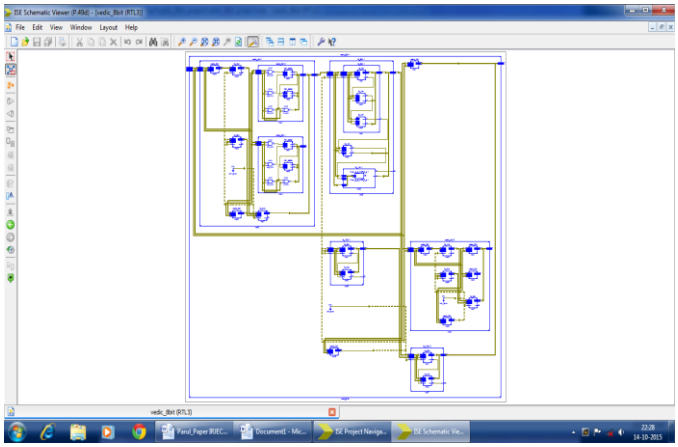

Fig. 5(a) -Technology Schematic of 8 bit Vedic Multiplier using RCA

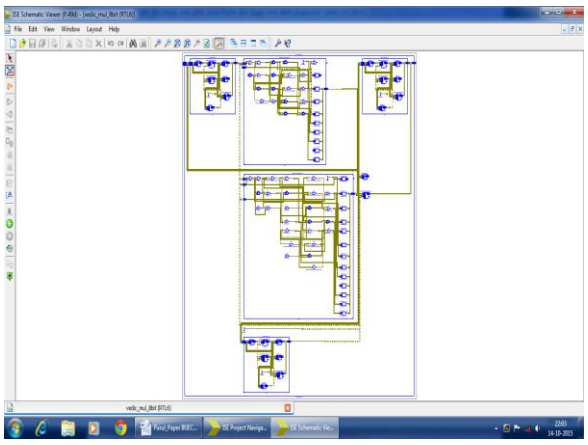

Fig. 5(b) -Technology Schematic of 8 bit Vedic Multiplier using KSA

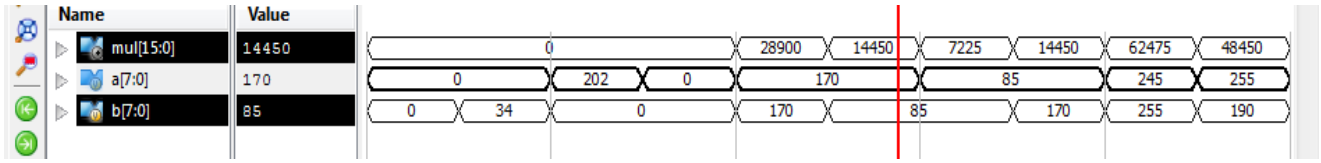

Fig. 5(c) - Simulation result of 8 bit Vedic Multiplier

The technology Schematic of 16 bit Vedic Multiplier using RCA which has lower processing speed and therefore produces more delay in computation as compared to KSA has been shown in fig 5 (d) below:-
The technology Schematic of 16 bit Vedic Multiplier using KSA which is considered as one of the fastest parallel prefix has been shown in fig 5(e) below:-
The simulation view of 16 bit Vedic Multiplier which displays the result of multiplying two16 bit numbers has been shown in fig 5(f) below:-

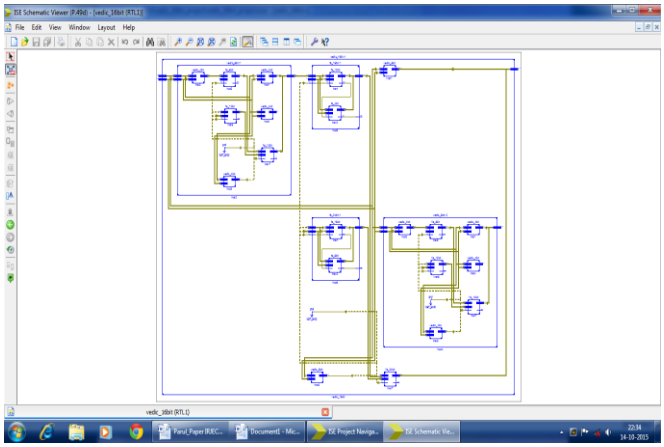

Fig. 5(d) -Technology Schematic of 16 bit Vedic Multiplier using RCA

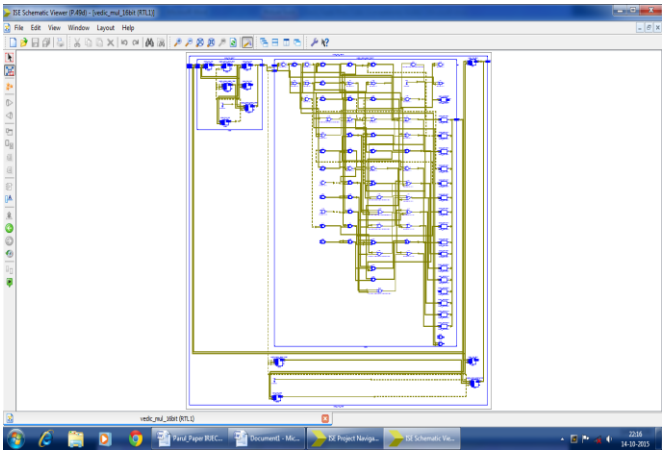

Fig. 5(e) -Technology Schematic of 16 bit Vedic Multiplier using KSA

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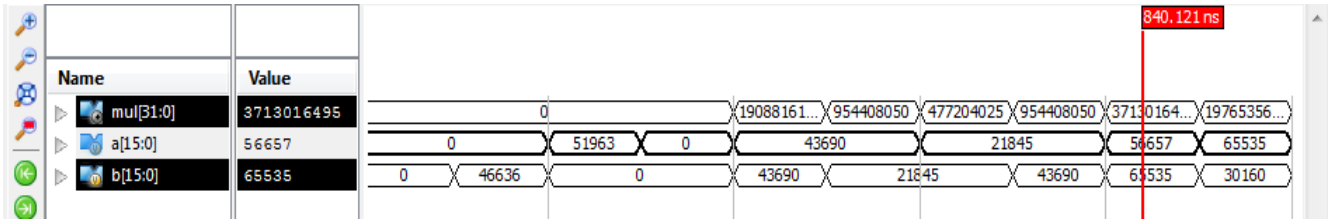

Fig. 5(f) - Simulation result of 16 bit Vedic Multiplier

The obtained results i.e. Delay, Levels of Logic, No. Of LUTS, Memory for the Vedic Multiplier (4/8/16 bit) designed using RCA and KSA for the device Spartan 6 Xc6slx45~3csg324 has been shown in table 1 below. It has been found that value of delay is less in the design of Vedic Multiplier using KSA as compared to RCA however the memory requirement increases.

Table 1- Obtained Results

Device-Spartan6 Xc6slx45~3csg324	**Using Ripple Carry Adder**				**Using Kogge Stone Adder**			
Vedic Multiplier	Delay (ns)	Levels of Logic	No. of slice LUTs	Memory (KB)	Delay (ns)	Levels of Logic	No. of slice LUTs	Memory (KB)
4 Bit	9.380	6	22	253328	9.813	7	22	253584
8 Bit	17.318	13	112	253200	15.713	13	130	254224
16 Bit	29.051	23	505	254800	27.499	22	647	256592

The delay comparison graph for the Vedic Multiplier (4/8/16 bit) designed using RCA and KSA for the device Spartan 6 Xc6slx45~3csg32 has been shown in fig 6 below. It has been found that the value of delay is less in KSA compared to RCA for the design of Vedic Multiplier(4/8/16 bit) as the number of bits of Vedic Multiplier increases the result becomes more accurate.

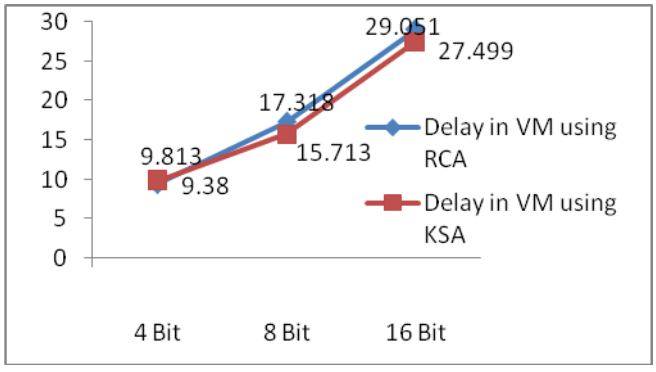

Fig. 6- Delay Comparison Graph for Vedic Multiplier (4/8/16 bit) using RCA & KSA

VI. CONCLUSION

This paper compares the design of Vedic Multiplier using Ripple Carry Adder and Kogge Stone Adder one of the fastest parallel prefix adder .It has been found from Table 1 that delay in 16 bit Vedic Multiplier using Kogge Stone Adder is 27.499ns which is less as compared to that by Ripple Carry Adder i.e. 29.051ns, also the memory required in the design using Kogge Stone Adder is more i.e.256592KB whereas that for Ripple Carry Adder is found to be

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254800KB. Hence it can be concluded that the design using Kogge Stone Adder is more efficient in terms of speed as it produces less delay however more memory as compared to Ripple Carry Adder.

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BIOGRAPHY

Parul Agrawal, received the BE degree in Electronics & Telecommunication Engineering from the Chhattisgarh Swami Vivekanand Technical University, INDIA in 2014. Presently pursuing M.E. (Communication) from Chhatrapati Shivaji Institute of Technology, DURG (CG). Her research interest includes Adders & Multipliers.

Rahul Sinha, received the ME (Communication) from the Swami Vivekanand Technical University, INDIA in 2013 and BE degree in Electronics & Telecommunication from the Pt. Ravishankar Shukla University, INDIA in 2005. He has done Advanced PG Diploma in VLSI Design in 2006. He has served as an ASIC engineer in a private organization for more than two years. Presently working as Assistant Professor in Department of Electronics & Telecommunication, Chhatrapati Shivaji Institute of Technology, DURG (CG). His research interest includes signal processing & VLSI.