ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 3, March 2015

Designing of MCAM Using 22nm Technology

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ABSTRACT: The main objective of our project work deals with the design and analysis of high speed performance Memristor based content addressable memory for future search engines to develop low power consumption and no loss of store data in a cell even if the power supply is turn OFF. The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development towards more compact design rules and, consequently, toward higher data storage densities.

KEYWORDS: Content addressable memory(CAM), memory resistor-based CAM (MCAM), SRAM, CMOS, 22nm technology, Microwind 3.1, Modelling.

I.INTRODUCTION

In this project we look at conceptualization, propose and modeling of memory cell as a part of a Memristor based Content Addressable Memory (MCAM) architecture using a combination of switch having some fixed resistance value as memristor and n-type MOS devices (i.e. NOR-TYPE MCAM CELL and NAND-TYPE MCAM CELL). A typical Content Addressable Memory (CAM) cell forms a SRAM cell that has two n-type and two p-type MOS transistors, which requires both V_{DD} and GND connections as well as well-plugs within each cell. Construction of a SRAM cell that use memristor technology, which has a non-volatile memory performance and can be fabricated as an extension to a CMOS process technology with nanoscaled geometry, addresses the major thread of modern CAM research towards reduction of power utilization. The propose of a CAM cell is based on fourth passive circuit element, the memristor predicted by Chua in 1971 and generalized by Kang. Chua postulated that new circuit elements defined by the single valued relationship dø=Mdq must exist; whereby current moving through memristor is proportional to the flux of magnetic field that flows through the substance. Therefore memristor-based CAM cells have the potential for significant saving in power indulgence.

Power has become one of the most important paradigms of design convergence for multi gigahertz communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. This project introduces design aspects for layout design of static RAM memory cell, conventional CAM memory cell and memristor-based CAM (MCAM) memory cell using VLSI technology. These cells are designed using latest 22nm CMOS technology parameters, which in turn offer high speed performance at low power. There is a large variety of types of ROM and RAM are available. These arise from the variety of applications and also the number of technologies available. This means that there are a large number of abbreviations or acronyms and categories for memories ranging from Flash to MRAM, PROM to EEPROM, and many more.

II.MEMRISTOR SWITCHING BEHAVIOR

The memristor behaves as a switch, much like a transistor. However, unlike the transistor, it is a two terminal rather than a three-terminal device and does not require power to retain either of its two states. A memristor changes its resistance between two values and this achieved via the movement of mobile ionic charge within an oxide layer. This behavior influences the architecture of CAM systems, where the power supply of CAM blocks can be disabled without loss of stored data. Therefore, memristor-based CAM cells have the potential for significant saving in power dissipation.

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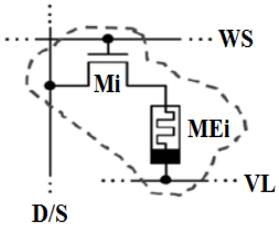
(a) "OFF" state, high resistance(b)"ON" state, low resistance Fig.1. Memristor switching behaviour

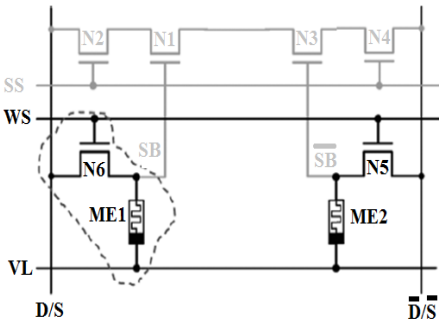
The key feature of memristor is it can remember the resistance once the voltage is disconnected. . In (a), L and *W* are the thin-film thickness and doped region thickness, respectively.In (b) "doped" and "undoped" regions are related to Ron and Roff, respectively. The dopant consists of mobile charges The memristor can be modeled in terms of two resistors in series, namely the doped region and undoped region each having vertical width of w and L-w, respectively, as shown in Fig.3

A.Generic Memristor n-MOS Circuit:

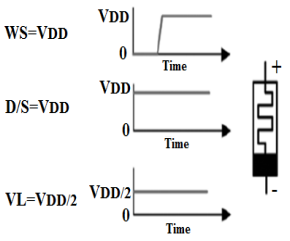
Fig.2. shows the basic structure for a memristor-nMOS storage cell. For writing logic "1," the memristor receives a positive bias to maintain an "ON" state. This corresponds to the memristor being programmed as logic "1." To program a "0" a reverse bias is applied to the memristor, which makes the memristor resistance high. This corresponds to logic "0" being programmed.



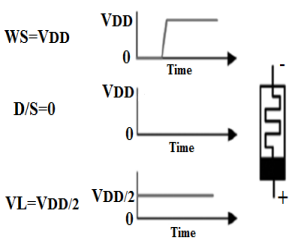
(a)Structure of write mode



(b)Basic cell



(c) Program "Low" resistance "1"



(d) Program "High" resistance "0"

Fig.2. Basic memristor-nMOS storage cell and the timing diagram

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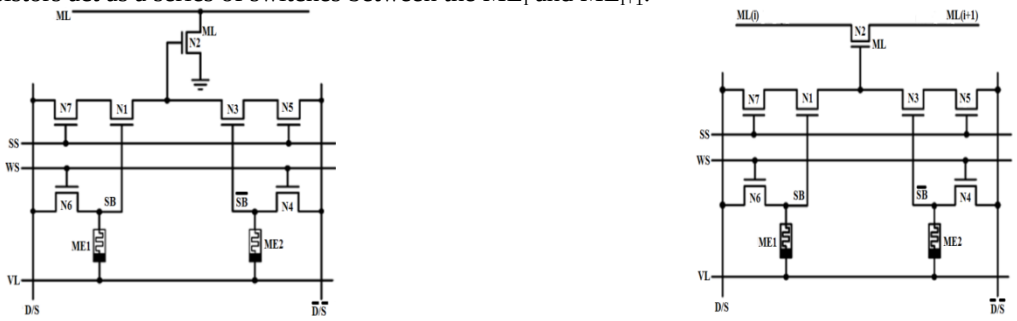
(a) Shows write mode part of the ith cell in a row. (b) Basic cell circuit without the match line transistor. (c) "Low" resistance, R_{ON}, programming, equivalent to logic "1". (d) "High" resistance, R_{OFF}, programming, equivalent to logic "0".

III.MEMORY ARCHITECTURE OF PROPOSED MCAM CELL

A. Proposed MCAM cell structure:

Fig.3.1 illustrates several variations of the MCAM core whereby bit-storage is implemented by memristors ME1 and ME2. Bit comparison is performed by either NOR or alternatively NAND-based logic as part of the match-line ML_i circuitry. The matching operation is equivalent to logical XORing of the search bit (SB) and stored bit (D). The match-line transistors (ML) in the NOR-type cells can be considered as part of a pull-down path of a precharged NOR gate connected at the end of each individual ML_i row. The NAND-type CAM functions in a similar manner forming the pull-down of a precharged NAND gate. Although each of the selected cells in Fig.3.1 have their relative merits, the approach in Fig.3.1 (a) where Data bits and Search bits share a common bus is selected for detailed analysis. The structure of the 7-T NAND-type, shown in Fig.3.1 (b), and the NOR-type are identical except for the position of the ML transistor. In the NOR-type, ML makes a connection between shared ML and ground while in the NAND-type; the ML transistors act as a series of switches between the ML_i and ML_{i+1}.



(a) 7-T NOR-type MCAM cell (b) 7-T NAND-type MCAM cell

Fig.3.1 Cell configurations of possible MCAM structure

B. Layout Design of proposed MCAM Cell:

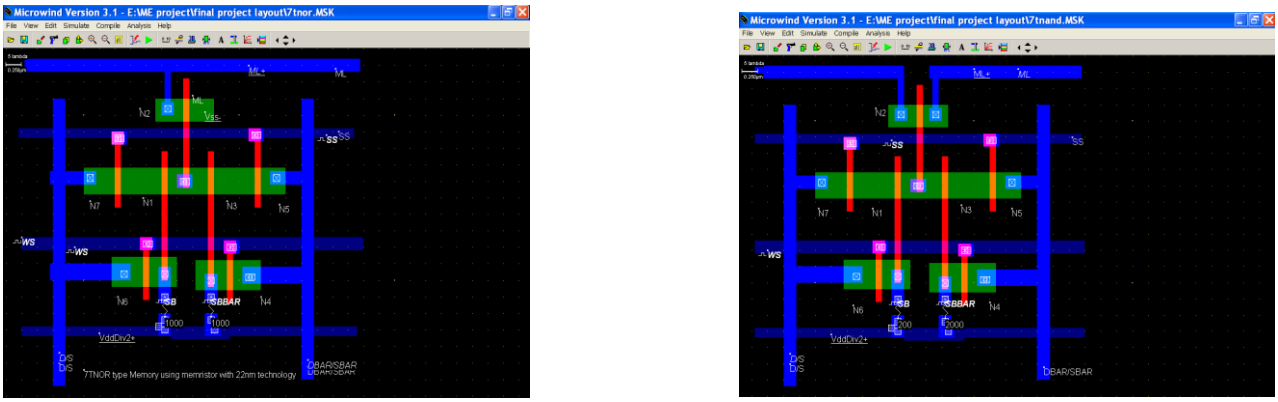


Fig.3.2. Layout design of 7 transistor, 2-Memristor NOR-type MCAM cell and Layout design of 7 transistor, 2-Memristor NAND-type MCAM cell

Fig 3.2 are the layout design of 7-T NOR-type MCAM cell and 7-T NAND-type MCAM cell respectively. Match Line i.e. ML is connected in parallel and series to 7-T NOR-type MCAM cell and 7-T NAND-type MCAM cell respectively to form array of cell. ML is a DC supply having DC voltage level at 0.35V. As this both cells do not have the p-MOS transistor, there is reduction in the chip silicon area.

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C.Design parameters of transistors of MCAM Cell:

Design parameters of each 7 transistor used to form 7-Transistor proposed MCAM cell is given in the following table 1. It consists of 7 n-MOS transistors and no p-MOS transistors. Width and length of each MOS transistor of both 7-T NOR-type MCAM cell and 7-T NAND-type MCAM cell are same and are measured in micrometer. Their current parameter is measured in microampere.

Table 1: Size and current of each transistor of MCAM Cell

MOS Transistor	W(µm)	L(µm)	W(Lambda)	L(Lambda)	Current Through MOS Transistor(mA) for NOR-type	Current Through MOS Transistor(mA) for NAND-type
N1	0.400	0.100	8	2	0.132	0.179
N2	0.350	0.100	7	2	0.209	0.022
N3	0.400	0.100	8	2	0.205	0.059
N4	0.450	0.100	9	2	0.455	0.459
N5	0.400	0.100	8	2	0.289	0.033
N6	0.450	0.100	9	2	0.443	0.419
N7	0.400	0.100	8	2	0.019	0.209

IV- DESIGN METHODOLOGY

To achieve the proposed target following steps are included in the design and analysis of proposed MCAM.

1. Schematic design of proposed MCAM using CMOS transistors.
2. Performance verification of the above for different parameters.
3. CMOS layout for the proposed MCAM using VLSI backend.
4. 4Verification of CMOS layout and parameter testing.

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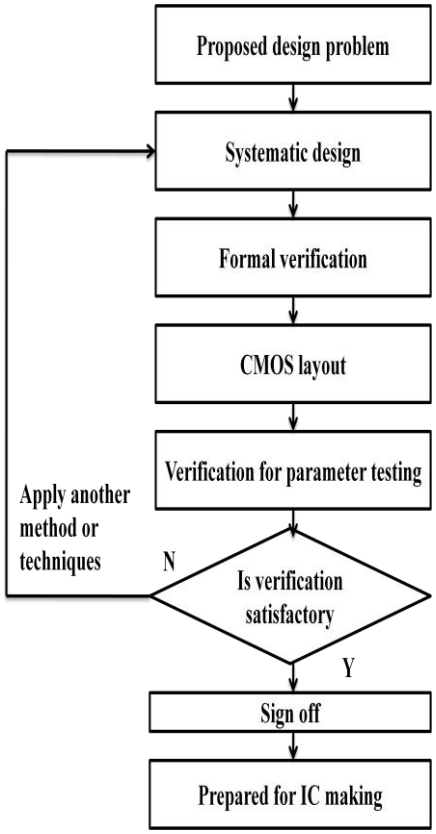

Fig.4. Design Flow Chart

If the goal is achieved for all proposed parameter including detail verification, sing off for the design analysis and design will be ready for IC making. If detail verification of parameters would not complete then again follow the first step with different methodology. The operational voltage is usually from 0.8 V to 1.2 V, depending on the technology variant. In Microwind, it decided to fix VDD at 1.0 V in the cmos22nm.RUL rule file, which represents a compromise between all possible technology variations available for this 22-nm node. Effort has been taken to design Low Power, High performance Memristor based Content Addressable Memory (MCAM) cell, using VLSI technology. The design process, at various levels, is usually evolutionary in nature. It starts with a given set of requirement. When the requirements are not met, the design has to be improved. More simplified view of the VLSI technology consists of various representations, abstractions of design, logic circuits, CMOS circuits and physical layout. Here for the design using VLSI technology microwind3.1 VLSI Backend software is used. This software allows designing and simulating an integrated circuit at physical description level. The proposed work is designed using 45nm CMOS/VLSI technology in Microwind 3.1software. The main novelties related to the 22nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 22 nm technology is 12nm. Some of the key features of 22nm technologies from various providers like TSMC and Intel are as given below. [13]
Compared to 45-nm technology, 22 nm technology must offer:

- 37% performance increases at low voltage.
- 50 % Power reduction at constant performance
- Improved switching characteristics(on current vs off current)
- 3D transistor are an important innovation needed to continue Moore's law.

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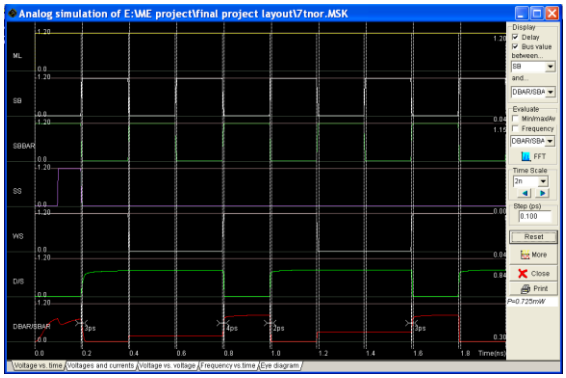
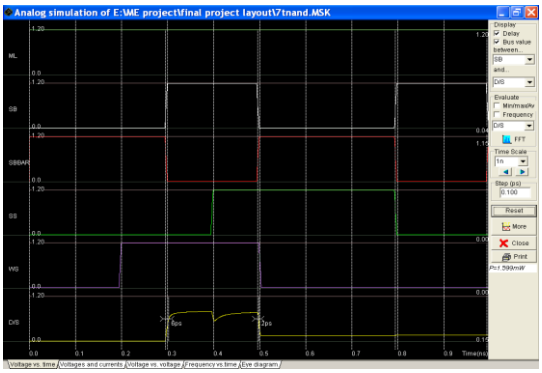
Considering the advantage of 22 nm technologies over 65 nm & 45 nm technologies, the proposed work is done with latest 22 nm technologies.

V.CELL CONFIGURATION OF MCAM CELL

A.7-T NOR-type MCAM Cell and 7-T NAND-type MCAM Cell:





5.1 Simulation of 7-T NOR-type MCAM Cell and 7-T NAND-type MCAM Cell

The simulation of the 7T NOR-type and 7T NAND-type MCAM cell is proposed in Fig 5.1 respectively. ML is applied to 7T NOR-type MCAM cell and 7T NAND-type MCAM cell in series and parallel respectively. Match Line (ML) is used only to connect one cell with another cell i.e. to form an array structure. Supply is given from WS LINE. When WS LINE is at logic 1 value then the transistors N6 and N4 are 'ON' and when WS LINE is at logic 0 value then the transistors N6 and N4 are 'OFF'.

When WS LINE is at logic 1 value, SB LINE gives its input data to output data i.e. D/S LINE and SB BAR LINE gives its input data to output data i.e. D BAR/S BAR LINE. When WS LINE is at logic 0 value, current flows through ME1 and ME2 via VDD/2 voltage supply having fixed resistance value. It means, when power supply is 'OFF' then also SB LINE takes its input data from ME1 and occurs this input data to output data i.e. D/S LINE while SB BAR LINE takes its input data from ME2 and occurs this input data to output data i.e. D BAR/S BAR LINE. This means that, memristor gives output even if power supply is OFF.From Fig, when WS LINE is at logic 1 value then SB LINE shows its output at D/S LINE and SB BAR LINE shows its output at D BAR/S BAR LINE. When WS LINE is at logic 0 value, then also SB LINE shows its output at D/S LINE and SB BAR LINE shows its output at D BAR/S BAR LINE because of memristor.From Fig 5.1, it is observed that, at time 0.0ns, WS LINE is at logic 1 value and SB LINE is at logic 0 value, so the output at D/S LINE is also at logic 0 value and SB BAR LINE is at logic 1 value, so the output at D BAR/S BAR LINE is at logic 1 value. At time 0.2 ns, WS LINE is at logic 1 value and SB LINE is at logic 1 value, so the output at D/S LINE is also at logic 1 value. At time 0.4ns, WS LINE is at logic 0 value and SB LINE is at logic 0 value but the output at D/S LINE is also at logic 1 value. This means that, SB LINE shows its output at D/S LINE even if the WS LINE (i.e. supply is OFF) is at logic 0 value. SB LINE shows its output at D/S LINE as it is until the next WS LINE is selected to logic 1 value. The power consumed by 7T NOR-type MCAM cell chip is 0.725mw and 7T NAND-type MCAM cell chip is 1.599mW.

VI.APPLICATIONS

1) **Non-volatile memory applications:** Non-volatile random access memory, or NVRAM, is pretty much the first to-market memristor application we'll be seeing.

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2) **Low-power and remote sensing applications:**
Coupled with memcapacitors and meminductors, the complementary circuits to the memristor which allow for the storage of charge, memristors can possibly allow for nano-scale low power memory and distributed state storage, as a further extension of NVRAM capabilities. These are currently all hypothetical in terms of time to market.

3) **Crossbar Latches as Transistor Replacements or Augmentors:**
The hungry power consumption of transistors has been a barrier to both miniaturization and microprocessor controller development.

4) **Analog computation and circuit Applications:** Analog computations embodied a whole area of research which, unfortunately, were not as scalable, reproducible, or dependable (or politically expedient in some cases) as digital solutions.

5) **Circuits which mimic Neuromorphic and biological systems (Learning Circuits):** The ability to map people brain activities under MRI, CAT, and EEG scans is leading to a treasure trove of information about how our brains work. But **modeling a brain using ratiocinated mathematics is like using linear algebra to model calculus.**

6) **Application for future search engines:**
The memory is required to search data i.e. to read the data in Google, Mozilla, etc.

VII. CONCLUSION

The proposed Memory is designed using 22 nm CMOS/VLSI technology with Microwind 3.1. The main novelties related to the 22 nm technology are the high-k gate oxide, metal gate and very low-k interconnect .The Software used in program allows us to design and simulate an integrated circuit at physical description level. The non-volatile characteristic and nanoscaled geometry of the memristor together with its compatibility with CMOS process technology increases the memory cell packing density, reduces power dissipation and provides for new approaches towards power reduction and management through disabling blocks of MCAM cells without loss of stored data.

The conventional 10T NOR-Type CAM cell has more silicon area as compare to other cells but it has advantage over 6T SRAM cell that it has low power consumption. 7T NOR-TYPE MCAM CELL and 7T NAND-TYPE MCAM CELL use memristor to overcome the disadvantage of loss of stored data when power supply is turned 'OFF'. When memristor is used in cell then the input data is stored in the memory as it is, even if the supply is OFF until next power supply is turned ON. From the analysis of various parameters of 7T NOR-TYPE MCAM CELL and 7T NAND-TYPE MCAM CELL it is observed that all the parameters of cells are same except the power consumption parameter. Hence, 7T NOR-TYPE MCAM CELL having power consumption of 0.725mw is more preferable as compare to 7T NAND-TYPE MCAM CELL having power consumption of 1.599mw. Matching Line (ML) is connected to cell to form array.

VIII. FUTURE SCOPE

- As the technology increases, performance speed of chip increases, power consumption decreases, chip area decreases, etc. The same layout design of 22nm technology can be used in increasing technology such as 18nm, 11nm and so on.
- Memristor based Content Addressable Memory is used for high performance future search engines.

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