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Design and Implementation of Digital System for Memories

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ABSTRACT: The memories are one of the key components associated with any digital system. They play a key role in the working of any system in an efficient manner. The optimization of memory usage and various other functionalities which are associated with memory and to be optimized and make judicial use of it in order to maximize the efficiency and also reduce the amount of memory used, When we come to know the developments of FPGA along with the limitations we can execute the parts of memory directly on the FPGA which is together with some idea or it can be logic. So it must contain separate design to implement for each memory. FPGA must have to support memories widely and therefore should be flexible to store (shapes and width).our paper is focused on describing the FCM architecture with many memory units and also mapping units which combine these units of memory.

KEYWORDS: Mapping units, logic memories, FPGA, FCM, Digital System.

I. INTRODUCTION

Memory is the core of the present electronic system. Memory filling is quick in the secondary memory device unit and being utilized in the execution of computer comments orders [1]. Furthermore, when we take more at memory proficiency in space, or the idea of the words put away in the memory.Non-volatile memory is exceptionally famous among advanced media; it is generally utilized in memory chips for USB memory [2]. Non-volatile memory eradicates the requirement for slow storage secondary memory system, including disk. Non- volatile memory is otherwise called non- volatile storage. Non- volatile memory is normally utilized for the assigning of memory storage[3].

In the field of VLSI, there is fast innovation which has prompted decreased electronic system and expanded transistor bulkiness of IC's. The devices like Field Programmable Gate Arrays we are getting headway from the past decade which has been opened new ways for digital systems. We can execute digital circuits from Field Programmable Gate Array (FPGAs) which are generally utilized these days yet that have little memory. Numerous FPGAs are having both logic memory to incorporate with digital circuits. Here we have programmable cells that are interconnected and cells are having easy logic work which is characterized by CAD tool designer. FPGAs have memory-based structures. The main work of these memories to store numbers of shapes of memories, because we need different memory for different requirements of device. FPGAs cannot handle the huge memory alone so we can use a special memory called Field Configurable Memory (FCM). When we consider a particular microchip for an embedded system it consists of several computational elements. On-chip FPGAs give high memory than that of off-chip. FPGA can change for every power-up .so we can structure effectively by making changes to FPGA with less cost but it is less storage in memory. These days we have FPGAs that use an on-die processor of 28Gbps.FPGA means the devices on the circuit board that increases the readability of devices. There are numerous FPGAs which are offering restricted memory capacity. When we consider on-chip FCM they have a huge transmission capacity than off-chip memory. So as we know few drawbacks in FPGA i.e. they give less memory and also in some cases flexibility is not good or performance is affected sometime. Therefore to resolve this issue and make all these three properties together we will be implementing memories to be fast and also flexible with very good supporting memory. In this paper we are designing and implementing FCM that fast and flexible which should also non-volatile.

II. BRIEF ARCHITECTURE OF FCM

Here we will describe a group of Field Configurable Memory models like the FiRM FCM. The FCM architecture is shown in Figure 1, comprises of b bits partitioned equally among n exhibits that can be combined (i.e. considering data and address mapping blocks) to actualize logic memory configurations[4].

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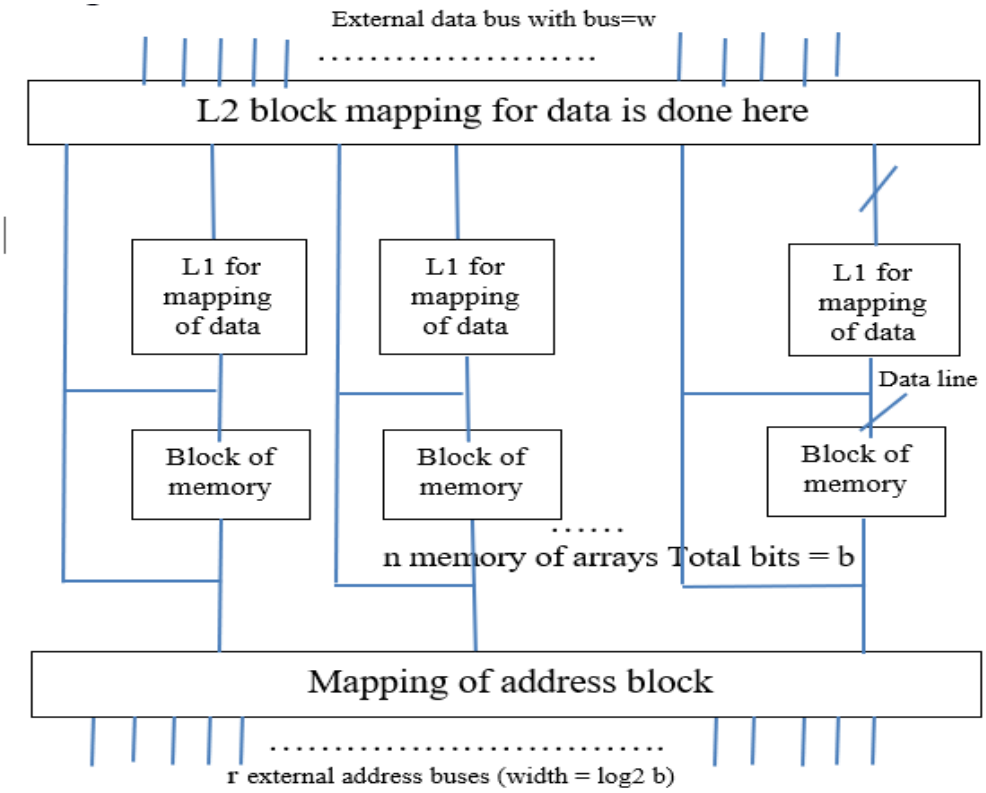

Fig.1. common architecture of the centralized FCM

The parameters used to describe every individual from this building family are given in Table 1.
here in this architecture we can implement a minimum number of m, r, and n.

Parameter	Meaning
B[4]	Total number of bits
N[4]	Number of arrays
M[4]	Number of external data buses
R[4]	Number of external address buses
W[4]	Nominal data width of each array
Weff [4]	Set of allowable effective data widths of each array

Table 1: Parameters for Architecture

The essential FCM structure comprises of a many basic Memory Blocks (BMBs) associated by a programmable interconnect structure. The BMBs are the physical memory units which can be utilized alone or together to make logical memories. the structure which is interconnected gives connections between BMBs and to the outer world as shown in figure 2[5].

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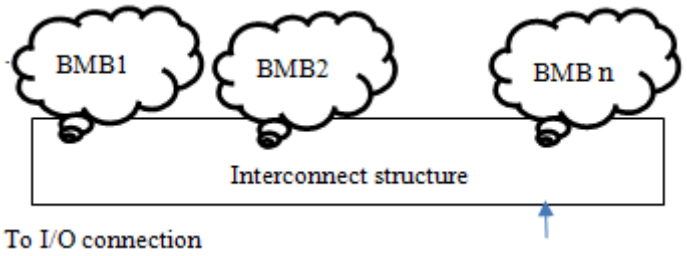

Fig.2. Simple Architecture of FCM

Here we can connect the memory units in 2 ways Horizontally and vertically . in which horizontal connections will give wider memory space and vertical will give deeper memory space. So as to expand the general adaptability or flexibility of the FCM, there is requirement to make each BMB configurable into many aspect ratio[5].
We will allude to the memory necessities of a given application circuit as a logic memory configuration[4]. Every free memory inside the logical (free space) memory configuration is called logical memory. Numerous configurations contain many logical memory. Example like, the decoder that is shown in table 2 need four (free space) logical memory. The functions like width ,speed makes the necessity of logic memory configuration. The table 2 we have consider circuits need to differ memories locations and memory sizes. FCM architecture should be efficient and implemented with many logic memory configuration[7].

Device	Usage of memory
Viterbi decoder	28x16 in 3 number, 28x3 in one number
Chip used in Graphics	128x22 in eight number, two number of 16x27
Chip for neural network	16x80 in one number , 16x16 in one number

Table 2: Example system

Now when we consider these BMB blocks the aspect ratio can be accepted when programmed up to ratio of 1K x 1. Here there is mapping block that is surrounding the array of memory as shown in figure 3. We have pass transistor as the main component in the mapping block that is used to connect the 8 bit M bus which is having fixed width to the memory array of D bus. A0 to A6 are the address lines they are used to connect the memory block one of 128 bytes[5].

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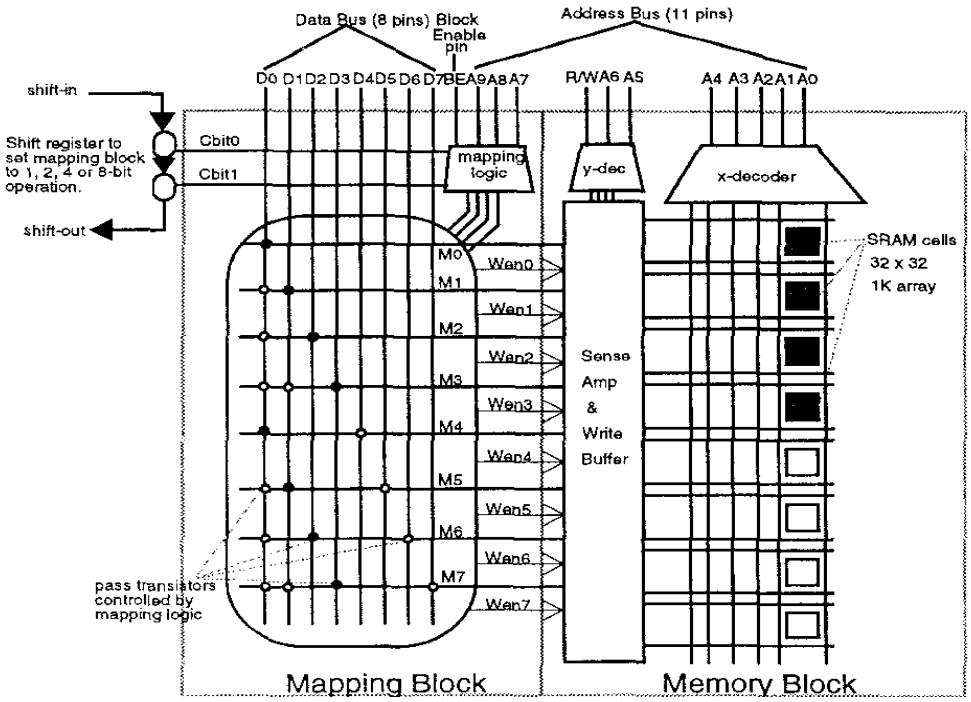

Fig.3. Block diagram of BMB

III. EVALUATING AND IMPLEMENTING MEMORY BLOCKS

This section describes about the comparison of area ,flexibility and speed. We can do this by taking all the circuits that contains memory. We then need to map the architecture of each to their circuits ,this can be success or not depends on architecture.

We can measure flexibility of this system by considering the architecture which is successfully mapped to each of it and the higher flexibility is one that has highest count in the architecture. Memory implementation can be done by accessing time and area of the chip. We have a problem in this approach i.e it has few memory logic[8]. Since this issue is there we will consider the logic blocks which has enough memory locations in it in some hundreds. There is some problem in the memory configuration because it cannot gather all the circuits together.

So by considering this drawback we can overcome this by using logical memory configuration generator that can generate randomly the memory, the parameter set is shown in the table 3 which shows parameter value which shows result.We can implement these logic circuits in the following steps as explained below:

Firstly we need to choose memories and here we will not be taking particular memory it is chosen any one randomly. Then we need to select width and depth where we will be choosing it between minimum and maximum values for both. And we will be using a parameter alpha that will indicate the proportion for power of two which is of generated dimension. Here we choose alpha value at 80 percentage where same value of percentage is used for depth and width which is generated as power of two which does not effect minimum and maximum value of width and depth.Once we get all bits generated from maximum number of logic memory these are compared to maximum number of bits and if this value is large we will be choosing completely new value of logic memory is chosen. Until we get less number of bits per configuration we should do this process. Now we need to map logic memory to architecture so we need some array that assigns values for buses like data bus , address bus to each logic memory required. If the memory that is mapped is populated and then we will connect external bus to the mapping memory . However the architecture shown in figure 4 has mapping block similar to this which make task less straightforward ness so this algorithm is developed.

As we know now flexibility is very much needed factor . mapping of logical memory may or may not be successful. There may be some reasons for which it is not successful i.e not be enough bits in architecture or no more data lines or also the blocks which are used for mapping will not be flexible to combine the array in that way that can be mapped to configuration, or in array the bits might be wasted.So we can define the flexibility as ratio ofNumber of configurations successfully mapped to Number of configurations attempted[4] .

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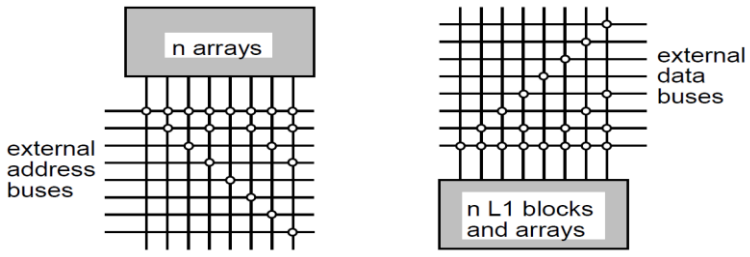
$$\text{Flexibility} = \frac{\text{Number of configurations successfully mapped}}{\text{Number of configurations attempted}}$$

So we can generate higher flexibility from this architecture.

Parameter	Meaning	Setting
b generated	Maximum number of bits per configuration	65536
n generated	Maximum number of logical memories	4
Width minimum	width of each logical memory	1
Width maximum	Maximum width of each logical memory	64
Depth minimum	depth of each logical memory	16
Depth maximum	Maximum depth of each logical memory	65536
Alpha	Proportion of dimensions that are a power of two	0.8

Table 3: List of Parameters of workload generator[4]



a) address mapping block width of each bus = $\log_2 b$

b) L2 data mapping block width of each bus = w

Fig.3. L2 Topology for mapping data and address

IV. SIMULATION RESULTS

Until now we have discussed about the effects that are varying which many memory of array and also topology for mapping of data on time , flexibility and also chip area.

V. CONCLUSION AND FUTURE WORK

Later we need to do some more developments on this FCM by comparing with other devices as we compared with FPGA and expanding for engineering development as the research respond to requirements for these memories are concerning FCM design we except these to include:

A. Advancing in the existing FCM and to use in the applications like data path circuits, DSP applications, limited state machines .

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B. The advancement of FCM frameworks for copying, increasing speed, and fast prototyping.

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BIOGRAPHY

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