ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 11, November 2015

Survey on Operations of Different Circuits of Analogue Comparator in CMOS Technology

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ABSTRACT *:* Comparator is one of the most essential analog circuits required in many analog integrated circuits. It is used for the comparison between two similar or different electrical signals with reference. The design of Comparator becomes an essential issue when technology is scaled down. Due to the non-linear behavior of threshold voltage (VT) when the scale of technology is reduced, performance of Comparator is affected. Many versions of comparator are proposed to acquire enticing output in sub-micron and deep sub-micron technologies. The selection of particular topology is dependent upon the requirements and application. In this we will simulate all types mentioned types of comparators and analyze them on the basis of different characteristics of comparator like : power dissipation , offset voltage , delay, speed and no. of transistor used. The simulated in HSPICE.

KEYWORDS: Double Tail Latch Type Comparator, Dynamic Comparator , Pre Amplifier Based Comparator , Dual Tail Double Rail Type Comparator, power dissipation, offset voltage, delay, speed, no. of transistors used ,low power analogue design.

I. INTRODUCTION

In electronics, Operational amplifier is designed to be used with negative feedback. It can be also used as comparator in open loop configuration. On the other hand, Comparator is especially designed for open loop configuration without any feedback. Hence it is the second most widely used device in electronic circuits after Opamp. Comparators are mostly used in analog-to-digital converter (ADCs). In the conversion process, the sampled signal is applied to a number of comparators to determine the digital equivalent of the analog value. Apart from that, comparators are used in peak detectors, zero crossing detectors, BLDC operating motors, switching power regulators

II. DEFINITION

Comparators are the device that compares two analogue voltages or currents and switches it output to indicate which one is larger.

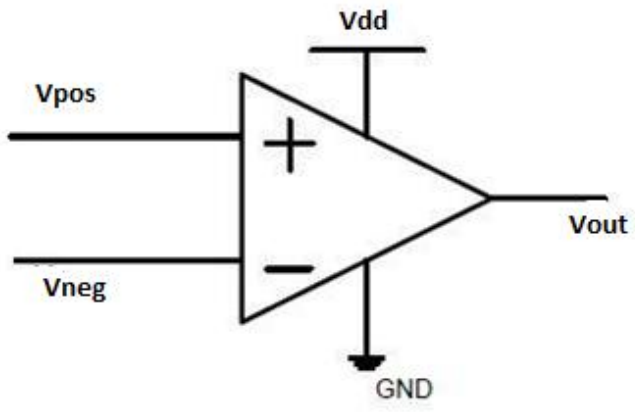

Fig. 1 Opamp Based Comparator

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If Vpos is at a greater potential than Vpos, then the output Vout of the comparator is logic 1 and when Vpos is at a potential less than Vneg, then the output is at logic 0.
If we apply a pulse voltage at Vpos and a DC reference voltage at Vneg, the output is logic 1 when the pulse amplitude is greater than the reference voltage. The figure is shown below. Thus a comparator compares two input analog value and gives binary output. In ideal case, binary signals can have two values at any point. But actually there is a transition region between the two binary states. For a comparator, it is important to pass quickly through that transition region. Basically comparators can be divided into two types. First are the Open loop comparators, which are nothing but OPamps. The second type is regenerative comparators. Regenerative comparators use positive feedback for the comparison of magnitude between two signals
Nowadays, where demand for portable battery operated devices is increasing, a major importance is given towards low power methodologies for high speed applications. Also we have to minimize the power consumption by using smaller feature size processes. However when we move towards power consumption minimization, the process variations and other parameters will greatly affect the overall performance of the device. Now comparators are used in ADCs and ADCs.

In this project paper .preparing a table of comparators which give information of all types of comparator, which can help designer to choose better comparator for their design‘s parameter and there requirements. The different parameter has compared as per information collected., along with comparing the comparator, the designing of low power comparator designed and simulated in HSPICE.

III. LITERATURE REVIEW

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2 Pedro M.Figueiredo, Joao C.Vital, *“***Kickback Noise Reduction Techniques for CMOS Latched Comparator***”*, IEEE Transactions on Circuits and Systems, vol.53, no.7, pp.541-545, July 2006.

3 B. Murmann et al., "I**mpact of scaling on analog performance and associated modeling needs**," IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 2160-2167, Sep. 2006.

4 Jun He, Sanyi Zhan, Degang Chen, and R.L. Geiger, *“***Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators***,”* IEEE Trans. Circuits Syst. I: Reg. Papers, vol. 56, pp. 911-919, May 2009.

5 Amin Nikoozadeh, Student Member, IEEE, and Boris Murmann, Member, IEEE”**An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch**” IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 53, NO. 12, DECEMBER 2006

6 ApisakWorapishet “**Speed and Accuracy Enhancement Techniques for High-Performance**.

7 Bernhard Goll “**A Comparator with Reduced Delay Time in 65-nmCMOS for Supply Voltages Down to 0.65 V**” IEEE transactions on circuits and systems—ii: express briefs, vol. 56, no. 11, november 2009.

IV. DIFFERENT COMPARATOR

A. *Pre Amplifier Based Comparator*

Operation: The figure shows the preamplifier based comparator. The comparator has three stages: 1)the input preamplifier stage, 2)a latch stage, and 3)an output buffer stage.
The preamplifier stage is fundamentally a differential amplifier with active loads . The Pre amp stage (or stages) amplifies the input signal to improves the comparator sensitivity and keep apart the input of the comparator from switching noise or kickback noise so it reduces noise coming from the regenerative feedback stage. It also can decrease input offset voltage. The sizes of Mosl and Mos2 are set by taking into account the diff-amp transconductance and the input capacitance. The transconductance schedules the gain of the stage

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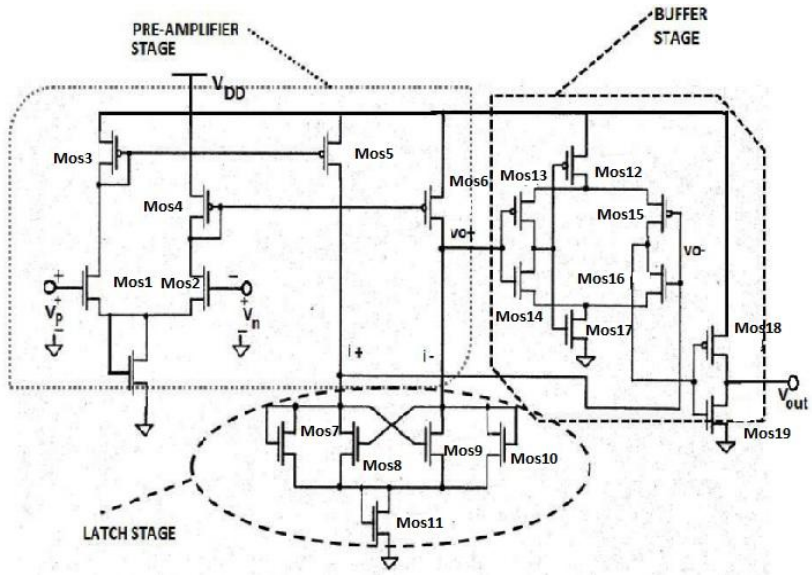

Fig.2. Pre amplifier based comparator

.While the size of Mosl and Mos2 determines the input capacitance of the comparator. Here gm1= gm2. The regenerative feedback latch stage is applied to determine which of the input signals are larger and extremely amplifies their difference. It takes regenerative feedback from the cross gate connection of Mos8 and Mos9. Consider i+ >> i- so that Mos7 and Mos9 are ON and Mos8 and Mos10 are OFF. Here also β of Mos7= β of Mos10=βa and β of Mos8= β of Mos9=βb for which vo- slightly equals to 0V and v0+ is If we start to increase current i- and decrease current i+, when drain to source voltage of Mos9 is equal to the threshold voltage, Vt of Mos8, switching occurs. At this point Mos8 takes current away from Mos7 which reduces drain to source voltage of Mos7 and Mos9 goes off. If we assume that maximum value of v+ or v- is equal to 2Vt, then under these situations Mos8 and Mos9 operate in cut-off or triode region in steady state conditions . Then voltage over Mos9 becomes Vt and Mos9 goes to saturation and current of Mos9 this is the point at which switching occurs; that is Mos9 turns off and Mos8 goes on. If βa= βb , then switching occurs when , i+ and i-, are be equal. A same type of analysis of enhancing current i+ reducing current i- results in the output buffer, the final product of this comparator, it gives a full scale digital level output (logic 0 or logic 1) from the output of latch stage .

B. *Double-Tail Latch Type Comparator*:

The figure 3 shows the schematic of the Double-Tail Latch type Voltage Sense Amp.

Double-Tail designed from the fact that the comparator uses one tail for input to the comparator and another for enable latching stage. It has less stacking and can operate at lower supply voltages. Large in size of the transistor Mos14 empowers large amount of current at latching stage which is free from common mode voltages at inputs and small in size of transistor Mos1 gives lower supply voltages resulting lower offset.

Operation: During rest phase when clk=0V, M4 and M5 charges to VDD which in turn charges Ni nodes to VDD. Hence Mos6 and Mos9 goes on and discharges output nodes to Ground. In evaluation phase when clk=VDD, the tail current of transistors Mos1 and M12 goes ON. On Ni nodes common mode voltage reduces and one input which is dependents on differential mode voltage generates. Mos6 and Mos9 pass this differential mode voltage to the latch stage. The inverters start to regenerate the voltage difference when the common-mode voltage at the Di nodes is no longer high enough for Mos6 and Mos11 to hold the outputs to ground . Mos6 and Mos9 also provide extra isolation and protection between the input and output which in turn reduces switching noise.

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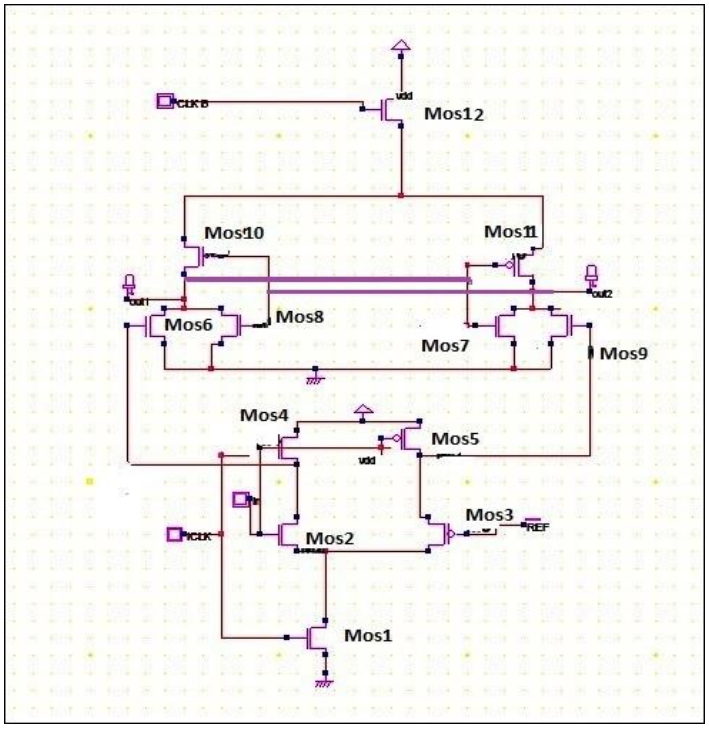

Fig.3. Double-Tail Latch Type Comparator:

C. *Dynamic Comparator*

Operation: The figure IV shows the Self- evaluating Dynamic type Comparator. This comparator fixed the above said problem by changing clkb signal with Ni nodes. But it enhanced delay by reason of Mos15/Mos16 use Ni node voltages as their input signal which gives slow exponential decay shape and due to current ability of driving the output node reduces. The input of latch offset is also decreased, in this arrangement of transistors due to the fact that output latch circuit takes load from the Mos8/Mos10 and Mos15/Mos16. Maximum drive current of the output node also reduced to 1/2th of current because of the supply voltage VDD has been divided into two transistors.

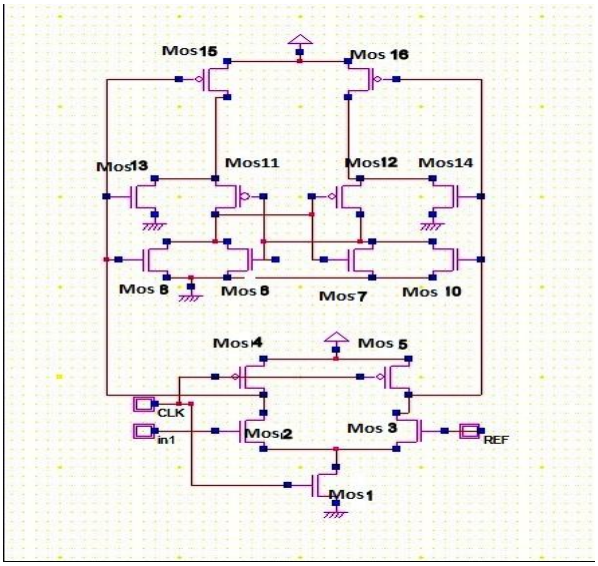

Fig.4. Dynamic Comparator

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

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Vol. 3, Issue 11, November 2015

D. *Double -Tail Dual-Rail Dynamic Latched Comparator*

Operations: The diagram (Figure V) shows the schematic of the Double-Tail Dual-Rail Dynamic Comparator .This comparator eliminated the dual clock system which is very difficult to control for positive and negative. Due to \synchronization is no needed between clock and clock B. Due to this, comparator shows lesser power dissipation than the all other comparators but it gives slower output then other comparators

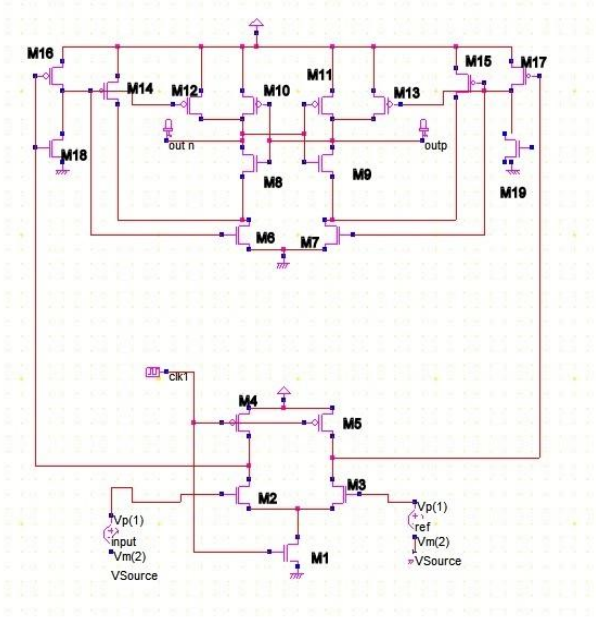

Fig.5 Double-Tail Dual-Rail Dynamic Latched Comparator

V. COMPARATIVE ANALYSIS

This table is prepared after simulation of each comparator in HSPICE , by which power dissipation is calculated and output of comparators are analysed so as in table , Double Tail Dual Rail Comparator consumes less power as compare to all other comparators

TABLE I
SUMMARY RESULT

Topology	**Parameters of comparator**	
	No. of transistor	**Power dissipation (µW)**
Pre amplifier based comparator	20	102.5
Double Tail Latch Type Voltage Sense Amplifier	22	64.7
Dynamic comparator	23	19
Double tail dual rail comparator	27	10.2

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VI. SIMULATION RESULTS

Input specification is comparator which consumes less power is given here on this table,In this table simulation level describes about parameter of NMOS & PMOS used in circuit. In this simulation (double tail dual rail dynamic comparator) when clock positive then it evaluate the applied signal .

Input specifications

Supply voltage	.9v
EDA Tool	HSPICE A -2008 .03
Simulation Level	54
Clock Voltage	0V -.9V
Reference Voltage	.2V - .9V

Transient Analysis

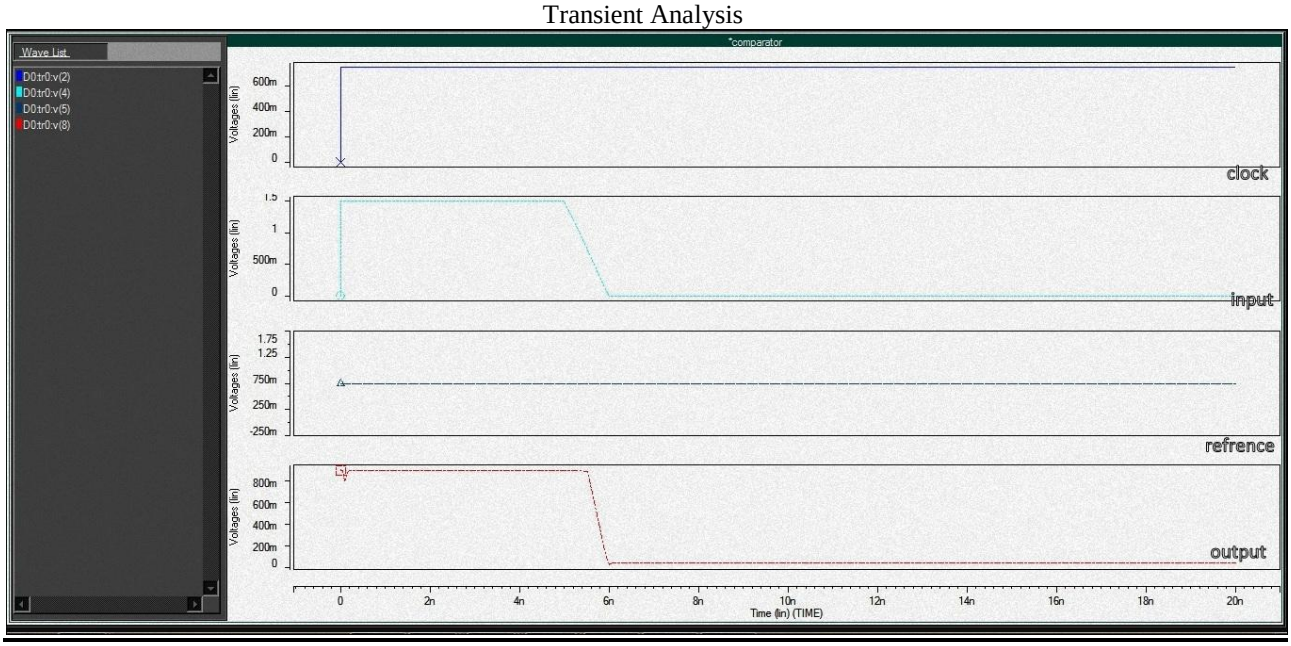

Fig.6. Simulation Result

VII. CONCLUSION AND FUTURE WORK

This paper explains operation of different comparators and its design. It help designer to analyze different comparator. It give brief knowledge about the comparator. The comparative analysis of comparator on the basis of power consumed by comparator which has simulated in HSPICE .so we can conclude that double tail dual rail dynamic type comparator consumes lesser power than other comparator.

In future offset voltages and its optimization of the circuits . finding application specific comparators con e other topic

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BIOGRAPHY

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