# Design and Implementation of Low power High speed and Area efficient FAM Operation

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**ABSTRACT**: Power consumption and small area is very important for fabricating DSP system and high performance system, requirement of present scenario computer system is dedicated for very high speed and low power unique multiplier unit for signed and unsigned number. Therefore in this paper focus on both signed and unsigned number by using modified booth multiplier. We introduce a structured and efficient recoding technique and explore three different schemes by incorporating them in FAM designs. the proposed technique yields considerable reductions in terms of critical delay, hardware complexity and power consumption of the FAM unit.The proposed SAM operate is designed by using VHDL and is implemented in Spartan 3E FPGA.

**KEYWORDS**: modified booth multiplier, partial product, VHDL, Xilinx

## I. INTRODUCTION

Multiplication is one of the basic functions used in digital signal processing (DSP). It requires more hardware resources and processing time than addition and subtraction. In fact,8.72% of all instructions in a typical processing unit are multiplier instructions. In computers, a typical central processing unit devotes a considerable amount of processing time in implementing arithmetic operations, particularly multiplication operations. Most high performance digital signal processing systems rely on hardware multiplication to achieve high data throughput. Multiplication is an important fundamental arithmetic operation. Multiplication-based operations such as Multiply and Accumulate (MAC) are currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform (FFT), filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still that dominant factor in determining the instruction cycle time of a DSP chip. The multiplier is a fairly large block of a computing system.

Recent research activities in the field of arithmetic optimization have shown that the design of arithmetic components combining operations which share data, can lead to significant performance improvements.Several architectures have been proposed to optimize the performance of the MAC operation in terms of area occupation, critical path delay or power consumption. Based on the observation that an addition can often be subsequent to a multiplication the Multiply-Accumulator (MAC) and Multiply -Add (MAD) units were introduced leading to more efficient implementations of DSP algorithms compared to the conventional ones, which use only primitive resources.
Except the MAC/MAD operations, many DSP applications are based on Add-Multiply (AM) operations. Targeting an optimized de-sign of AM operators, fusion techniques are employed based on the direct recoding of the sum of two numbers in its Modified Booth (MB) form. Although the direct recoding of the sum of two numbers in its MB form leads to a more efficient implementation of the fused Add-Multiply (FAM) unit.

We propose a new recoding technique which decreases the critical path delay and reduces area and power consumption The proposed *S-MB* algorithm is structured, simple and can be easily modified in order to be applied either in signed or un-signed numbers.

## II. LITERATURE SURVEY

Multiplier architectures fall generally into two categories i.e., "tree" multipliers and "array" multipliers. Tree multipliers add as many partial products in parallel as possible and therefore, are very high performance architectures.

Unfortunately, tree multipliers are very irregular, hard to layout and hence large. Array multipliers, on the other hand, are very regular, small in size, but suffer in latency and propagation delay.

Array multiplier is well known due to its regular structure. Multiplier circuit is based on add and shift algorithm. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit [2]. Here X is the multiplicand and Y is the multiplier. The partial products obtained by multiplying the four bits of the multiplicand with each bits in the multiplier.

Trees are an extremely fast structure for summing partial-products. Tree structures require only order log N stages to reduce N partial products by performing parallel additions. The tree multiplication algorithm can reduce the number of partial products by employing multiple input compressors capable of accumulating several partial products concurrently. Tree multiplier can handle the multiplication process for large operands. This is achieved by minimizing the number of partial product bits in a fast and efficient way by means of a CSA tree constructed from 1-bit full adders.

A fast process for multiplication of two numbers was developed by Wallace. In 1964, C.S. Wallace observed that it is possible to find a structure, which performs the addition operations in parallel, resulting in less delay. Wallace introduced a different way of parallel addition of the partial product bits using a tree of carry save adders, which is known as "Wallace Tree".

Andrew D. Booth proposed the Booth recoding, or Booth algorithm in 1951. This method can be used to multiply two 2"s complement number without the sign bit extension. Booth observed that when strings of '1' bits occur in the multiplicand the number of partial products can be reduced by subtraction.

### III. PROPOSED SYSTEM

AM units which implement the operation $Z = X(A+B)$. The conventional design of the AM operator (Fig3. 1(a)) requires that its inputs $A$ and $B$ are first driven to an adder and then the input $X$ and the sum $Y = A+B$ are driven to a multiplier in order to get $Z$. The fused Add -Multiply (FAM) component contains only one adder at the end (final adder of the parallel multiplier). As a result, significant area savings are observed and the critical path delay of the recoding process is reduced.
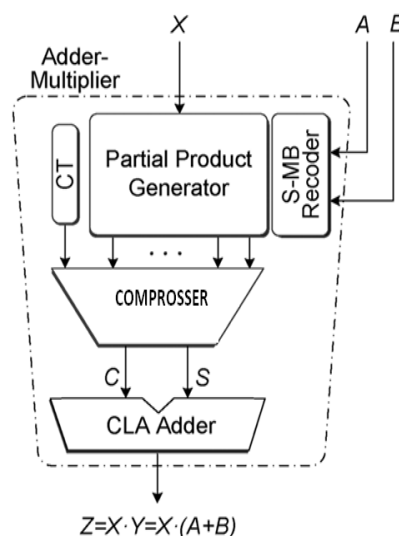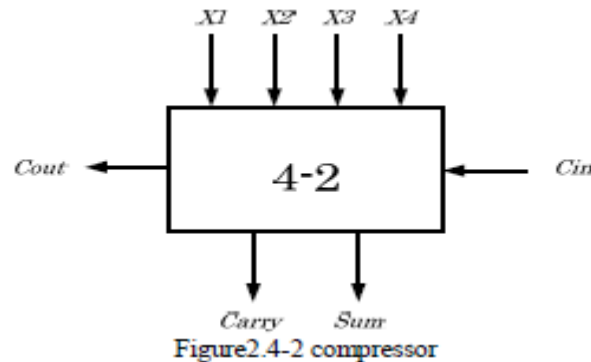


Fig. 1 Proposed FAM operator

Figure2.4-2 compressor

The characteristics of the 4:2 compressors:
1. The outputs represent the sum of the five inputs, so it is really a 5 bit adder
2. Both carries are of equal weighting
3. To avoid carry propagation, the value of Cout depends only on A,B,C and D. It is independent of Cin.
4. The Cout signal forms the input to the Cin of a 4:2 of the next column.

In order to transform the two aforementioned pairs of bits in MB form we need to use signed-bit arithmetic. For this purpose, we develop a set of bit-level signed Half Adders (HA) and Full Adders (FA) considering their inputs and outputs to be signed. We use two types of signed HAs which are referred as HA*and HA**, and two types of full adders which are FA*and FA**.

We use both conventional and signed HAs and FAs. In order to design and explore three new alternative schemes of the *S-MB* recoding technique. In the scheme can be easily applied in either signed (2's complement representation) or unsigned numbers which consist of odd or even number of bits. In all schemes we consider that both inputs A and B are in 2's complement form and consist of 2K bits in case of even or 2K+1 bits in case of odd bit-width.

A. *S-MB1 RECODING:*

The recording scheme is referred to as S-MB1 and it is obtained for both odd and even number of bit width of input numbers. The encoding of the modified booth is based on both digits $S_{2j+1}$ and $S_{2j}$ are extracted from the j recoding cell.The first scheme of the proposed recoding technique is referred as *S-MB*1 and is illustrated in detail in Fig.3.

B. *S-MB2 RECODING:*

The recoding technique is S-MB2 is described for even and odd bit-width of input numbers. Onside the initial values c0,1. The inputs of the FA are $a_{2j}, b_{2j}$ and $c_{2j}$.The bit$c_{2j,1}$ is the output carry of a conventional HA which is part of the (j-1) recording cell and has the bits $a_{2j-1}, b_{2j-1}$,as inputs. The HA*is used in order to produce the negatively signed sum and its outputs.

C. *S-MB3 RECODING*

The third recoding technique is S-MB3.we use a conventional FA to produce the carry $c_{2j+1}$ and the sum$s_{2j}$..The bit $c_{2j,1}$ is now the output carry of HA* which belongs to the (j-1) recoding cell and has the bits $a_{2j-1}, b_{2j-1}$ as inputs.
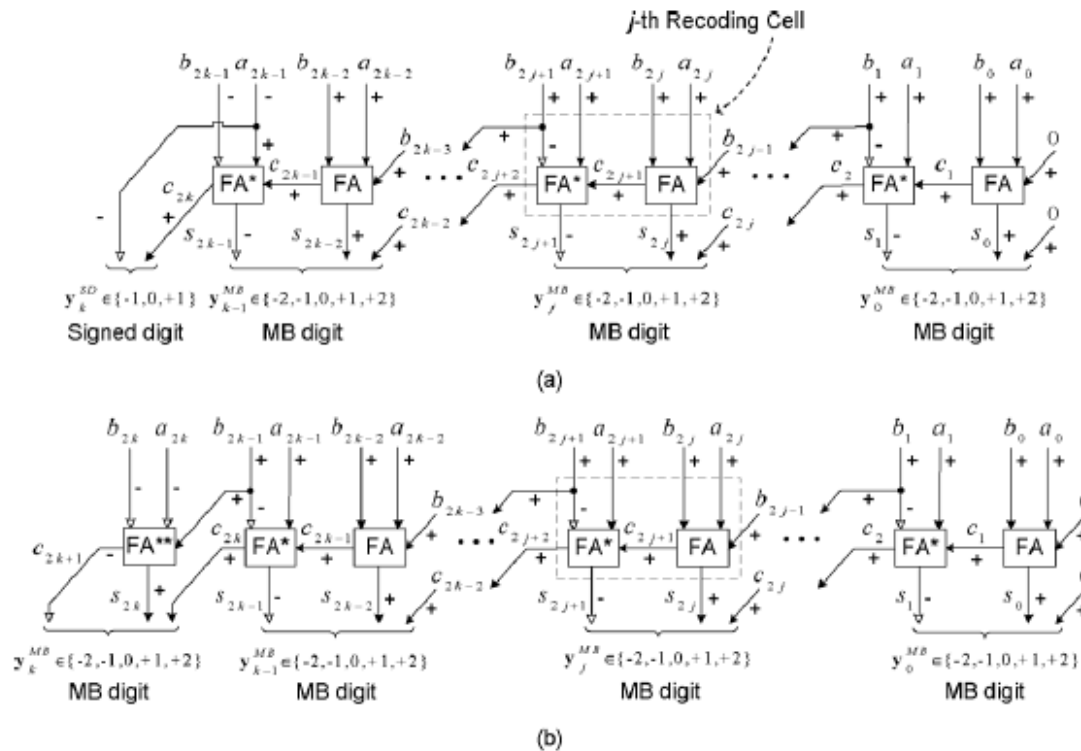
**Figure3 S-MB1 Technique for (a) even and (b) odd number of bits**

IV. **SIMULATION AND IMPLEMENTATION RESULTS**

The proposed design is developed using VHDL and synthesized using XILINX 13.2 and is simulated in ISim for Spartan-3E FPGA series. Simulation result ofS-MB1 is shown in Fig. 4 (even) and Fig 5 (odd) Table 2 shows the comparison of area, delay and power.
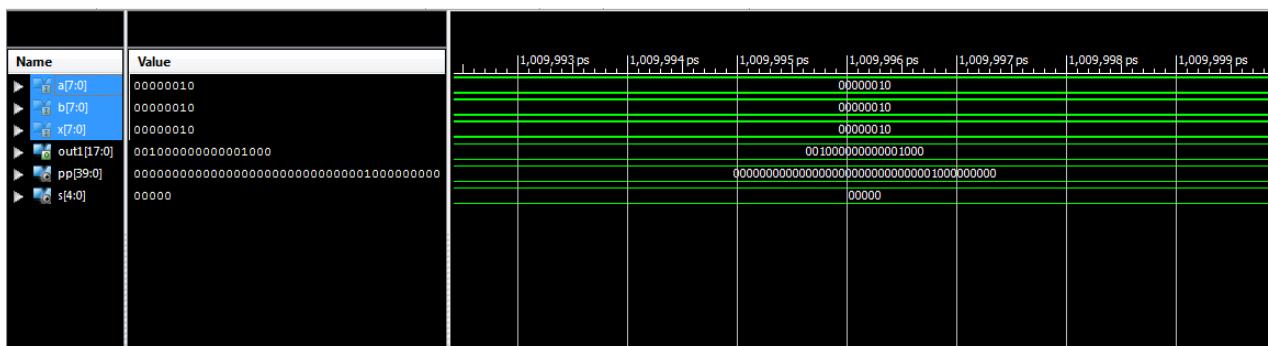


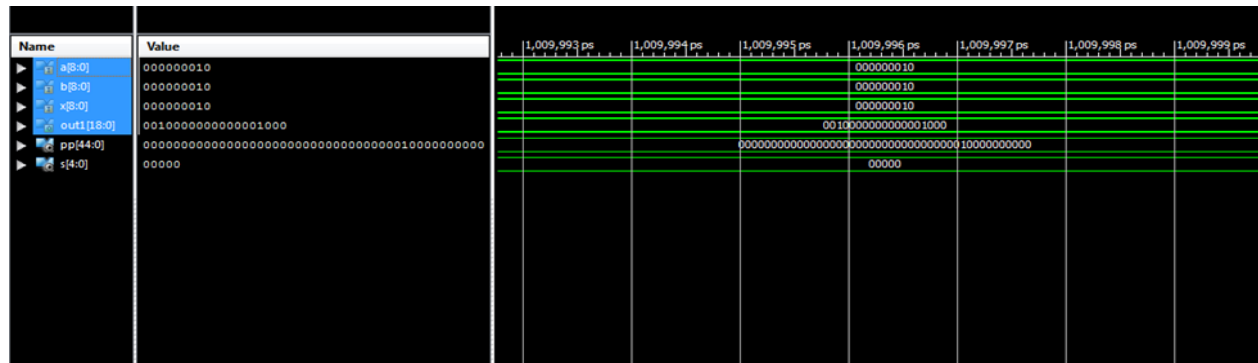Fig. 4. Simulation Result of S-MB1 recoding for even number of bits

Fig. 5. Simulation Result of S-MB1 recoding for odd number of bits

| Design | Bits | Area (No. of Slices) | Delay (ns) | Total Power (mw) |
|---|---|---|---|---|
| Conventional FAM | 8 | 95 | 28.762 | 156 |
| SMB1 | 8 | 92 | 26.935 | 153 |
| Area-delay-power efficient SMB1 | 8 | 44 | 22.727 | 151 |

Table 1 comparison of conventional FAM, SMB1, proposed SMB1 technique

## V.  CONCLUSION

Power, delay and area are the constituent factors in VLSIdesign that limits the performance of any circuit. This workpresents a simple approach to reduce the area, delay andpower of FAM operator.The design of sum –product are used to implement the direct recoding of the sum of two numbers in its modified booth form. The proposed S-MB recoding technique  has low power, less delay and reduced area than existing S-MB recoding technique

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### BIOGRAPHY

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