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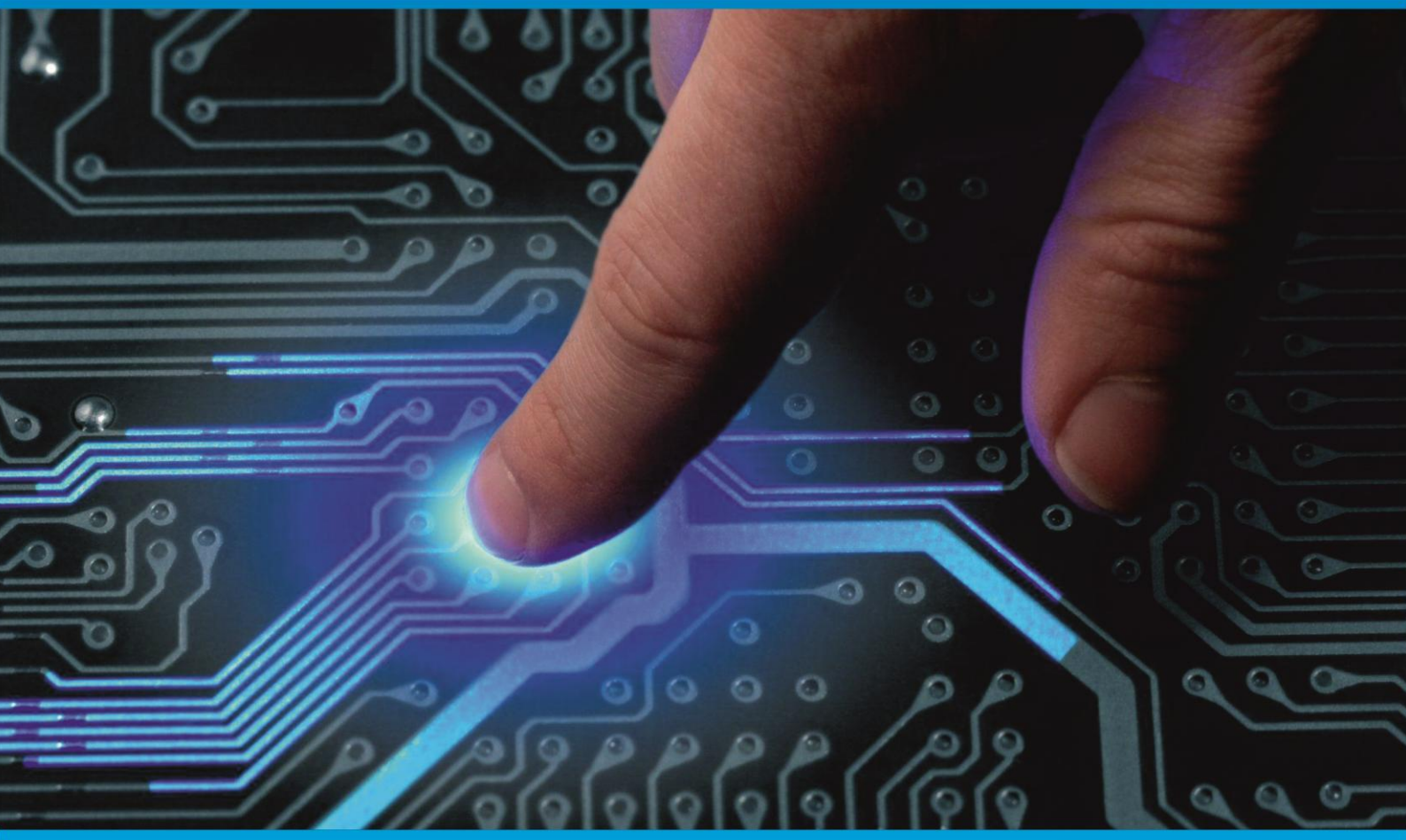

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A High Performance and Energy Capable FIR Robust Filter Using Relative Assigned Arithmetic Circuits

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ABSTRACT: Adder and multipliers are used in many processors to accomplish fast arithmetic function. Many different adder architecture designs have been developed to increase the efficiency of the adder. A filter is used to pass a specific band of frequency. Depending on the response of the system, digital filters can be classified into Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). Digital filters are widely used in many digital signal processing applications. Therefore digital filtering is one of the basic need of digital signal processing. In traditional fir filter consumes more power and area because of multipliers usage to avoid this disadvantage in this paper designs a new approach to design a fir filter by using distributive arithmetic method in lutless method. In this paper fir with traditional adder is existed design and fir filter using parallel prefix adder is the proposed design. Parallel prefix adder are the good adder for fast execution it is reduce the complexity of the multiplication process, it causes to reduce the power and area of the design Performance of all adder designs. And this project implemented for 64 bit lut less fir structure , These structures are synthesized on Xilinx 12.3 ISE tool.

KEYWORDS: Finite Impulse Response (FIR), Infinite Impulse Response (IIR)

I. INTRODUCTION

Filter is a frequency selective network. It passes a band of frequencies while attenuating the others. Filters are classified as analog and digital depending on nature of inputs and outputs. Filters are further classified as finite impulse response and infinite impulse response filters depending on impulse response. This chapter gives a brief about the types of filters.

1.1 Analog Filters : Analog filters can be passive or active. Passive filters use only resistors, capacitors, and inductors. Passive designs tend to be used where there is a requirement to pass significant direct current (about 1mA) through low pass or band stop filters. They are also used more in specialized applications, such as in high-frequency filters or where a large dynamic range is needed. (Dynamic range is the difference between the background noise floor and the maximum signal level.) Also, passive filters do not consume any power, which is an advantage in some low-power systems. The main disadvantage of using passive filters containing inductors is that they tend to be bulky. This is particularly true when they are designed to pass high currents, because large diameter wire has to be used for the windings and the core has to have sufficient volume to cope with the magnetic flux.

Very simple analog low pass or high pass filters can be constructed from resistor and capacitor (RC) networks. In the low pass case, a potential divider is formed from a series resistor followed by a shunt capacitor, as illustrated in Figure 1.1. The filter input is at one end of the resistor and the output is at the point where the resistor and capacitor join. The RC filter works because the capacitor reactance reduces as the frequency increases. It should be remembered that the reactance is 90" out of phase with resistance. At low frequencies the reactance of the capacitor is very high and the output voltage is almost equal to the input, with virtually no phase difference. At the cutoff frequency, the resistance and the capacitive reactance are equal and the filter's output is l / f i of the input voltage, or -3 dB. At this frequency the output will not be in phase with the input: it will lag by 45" due to the influence of the capacitive reactance.

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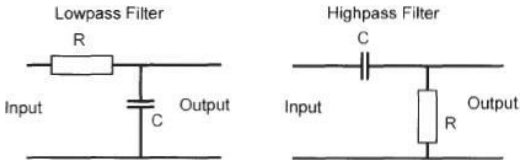

Figure 1.1 Low pass and High pass RC Networks

At frequencies above the 3 dB attenuation point, the output voltage will reduce further. The rate of attenuation will be 6 dB per doubling of frequency (per octave). As the frequency rises, the capacitive reactance falls and the phase shift lag approaches 90". the attenuation and phase shift decrease. Low pass and high pass RC networks are illustrated in **Figure 1.1.**

Integrated circuit (IC) filters are now quite common because they can be much smaller than active filters using op-amps and very much smaller than passive filters. Their small size supports the general trend to miniaturize equipment. The IC filters fall into two categories: continuous time and switched capacitor. Continuous time filters use a number of op-amp circuits within the IC, and often integrating resistors and capacitors too. The filter response is selected by the addition of further resistors or capacitors around the IC. Continuous time filters tend to have a limited frequency range because of the integrated component values that have been provided.

Switched capacitor IC filters use the principle of rapidly charging and discharging a capacitor to replace a resistor, as shown in Figure 1.2. The effective resistor value depends on the rate of switching of the charge and discharge cycle. As the switching speed is changed, the effective resistance of the circuit also changes. The filter can thus be tuned by changing the switch clocking frequency. This type of filter generates signals at the switching frequency, and they tend to be generally noisy. Most switched capacitor filters are low pass types and are limited in their frequency range to below 100 kHz.

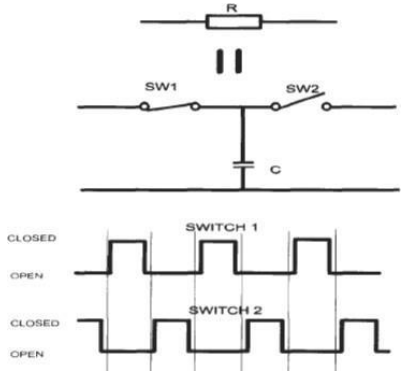

Figure 1.2 Switched Capacitor "Resistor Equivalent"

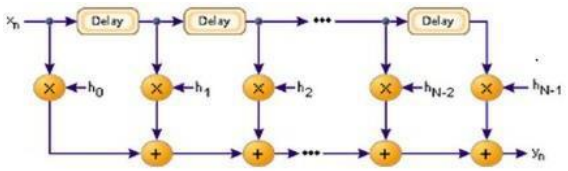

Figure 1.3 Logical Structure of FIR Filter

$$y[n] = \Sigma\, h(n)\, x(n-k) \qquad 1$$
$$k=0$$

Here y[n] is output signal
X(n) input signal
H(n) filter coefficient
N number of samples

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II. INTRODUCTION TO VLSI

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors.

2.1 Overview

The first semiconductor chips held one transistor each. Subsequent advances added more and more transistors, and, as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as "small-scale integration" (SSI), improvements in technique led to devices with hundreds of logic gates, known as large-scale integration (LSI), i.e. systems with at least a thousand logic gates. Current technology has moved far past this mark and today's microprocessors have many millions of gates and hundreds of millions of individual transistors.

2.2 VLSI and systems

These advantages of integrated circuits translate into advantages at the system level:

- Smaller physical size. Smallness is often an advantage in itself-consider portable televisions or handheld cellular telephones.
- Lower power consumption. Replacing a handful of standard parts with a single chip reduces total power consumption.
- Reduced cost. Reducing the number of components, the power supply requirements, cabinet costs, and so on, will inevitably reduce system cost.

2.3 Applications

- Electronic system in cars.
- Digital electronics control VCRs
- Transaction processing system, ATM
- Personal computers and Workstations
- Medical electronic systems.

III. EXISTED DESIGN

3.1 FIR FILTER USING CARRY SKIP ADDER BASED ON LUT-LESS DA METHOD

In LUT - Less DA technique, multiplexers substitute LUT traditional DA architecture. This reduces the area and energy usage of the design. The implementation of the 4-tap FIR filter based on LUT - Less DA is shown in Figure

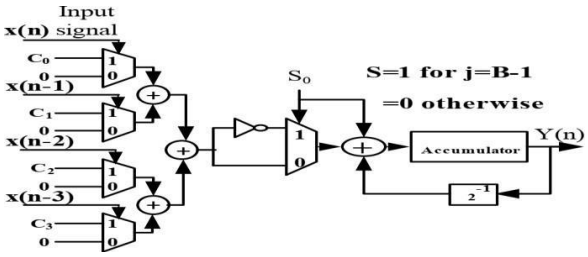

Figure 3.1 : LUT-less DA architectures for a 4-tap FIR filter

3.2 CARRY SKIP ADDER

A carry-skip adder (also known as a carry-bypass adder) is an adder implementation that improves on the delay of a ripple-carry adder with little effort compared to other adders. The improvement of the worst-case delay is achieved by using several carry-skip adders to form a block-carry-skip adder. The worst case for a simple one level carry-ripple-adder occurs, when the propagate-condition is true for each digit pair (ai,bi). Then the carry-in ripples through the n-bit adder and appears as the carry-out after For each operand input bit pair (ai ,bi) the propagate-conditions pi=(ai xor bi). are determined using an XOR-Gate (see). When all propagate-conditions are *true*, then the carry-in bit c0 determines the carry-out bit.

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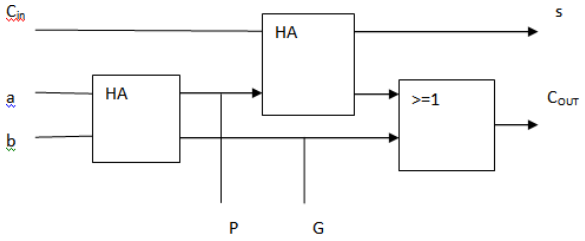

Figure 3.2: Single bit Carry Skip Adder

The critical path of a carry-skip-adder begins at the first full-adder, passes through all adders and ends at the sum-bit sn-1. Carry-skip-adders are chained (see block-carry-skip- adders) to reduce the overall critical path, since a single n-bit carry-skip-adder has no real speed benefit compared to a n-bit carry-ripple-adder.

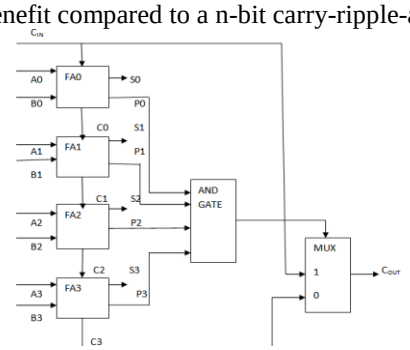

Figure 3.3 :Carry Skip Adder

IV. PROPOSED DESIGN

4.1 FIR FILTER USING BRENT KUNG ADDER IN LUT LESS DA METHOD :

In this paper proposes FIR filter with inexact speculative adder by LUT less method. Here x(n) is the input signal which is stored in shift register and h(n) is the only filter coefficient as shown in the figure 6. When shifting is happens lsb bit of each shifting is the selected line to the multiplexers and the number of multiplexers used in the design is depends up on the length of the input signal. If the length of the input signal is 64 then multiplexers used in the design is 64,and the each multiplexer is based on equation 1.

$$mi = h[i] \; when \; Rout[i] = 1$$
$$= 0 \; other \; wise \qquad (1)$$

Here mi is multiplexer output

h[i] is filter coefficient

Rout[i] is register output

The add operation was performed after completion of multiplexing by different levels ,these levels also depends on the length of the input signal, if the length of input signal is 2n then n-1 number of levels were done in that particular design. The output of adders in those levels are addf, adds ,addt,…addfinal.

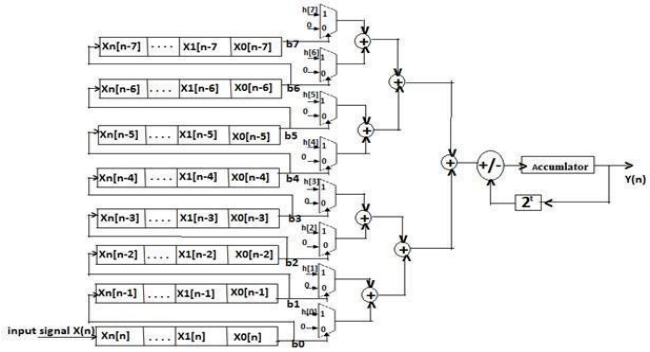

Figure 4.1 : LUT-less DA architectures

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4.2 BRENT-KUNG ADDER

The Brent-Kung adder is a parallel prefix adder. The Brent-Kung adder was developed by Brent and Kung which they published in 1982. Brent-Kung has maximum logic depth and minimum area. The number of cells is calculated by using 2(n-1) -Log2n .The 4-bit and 32 bit Brent- Kung adder figures shown below.

The main drawback in ripple carry adder is delay in carry calculation i.e., the time required to generate the carry by the adder block.Brent Kung adder is one of the parallel prefix adders. It is the most popular adder that is used to increase the speed of operation. These adders are designed by using carry look ahead adders structure.

Working of Brent Kung adder:

It consists of three stages Pre-processing

Generating the carry propagation (p) and carry generation (g) signals. Calculation of the sum value by using carry generation and propagation signals.

In the pre-processing stage carry propagate and generate equations are found by using the generalized equation

Pi = Ai XOR Bi

Gi = Ai AND Bi

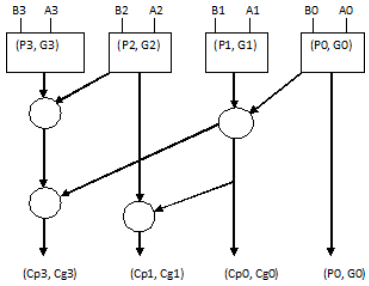

Figure 4.2: 4-bit Brent kung adder

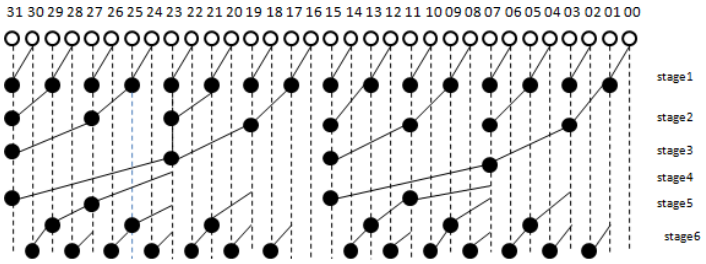

Figure 4.4 : 32-bit Brent kung adder

V. SOFTWARE USED

Xilinx

Xilinx software is used by the VHDL/VERILOG designers for performing Synthesis operation. Any simulated code can be synthesized and configured on FPGA. Synthesis is the transformation of VHDL code into gate level net list. It is an integral part of current design flows.

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VI. RESULTS

6.1 EXISTED DESIGN RESULTS :

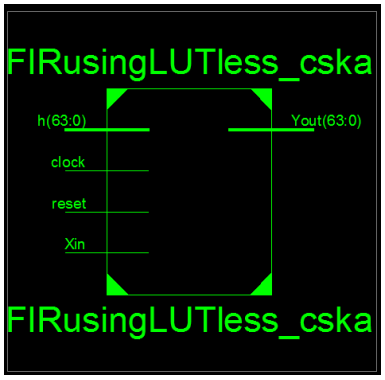

Figure 6.1: RTL schematic

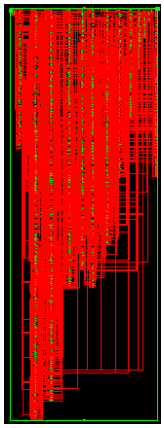

Figure 6.2: View Technology Schematic

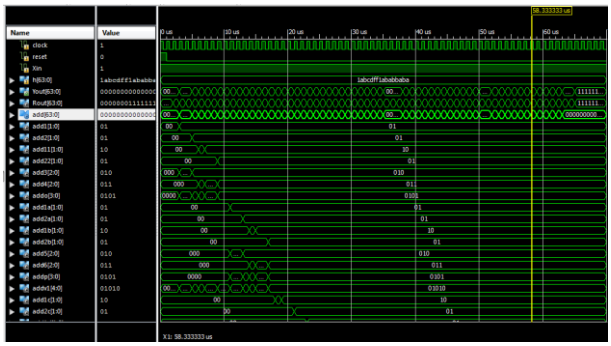

Figure 6.3 : simulated wave forms

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6.2 PROPOSED DESIGN RESULTS:

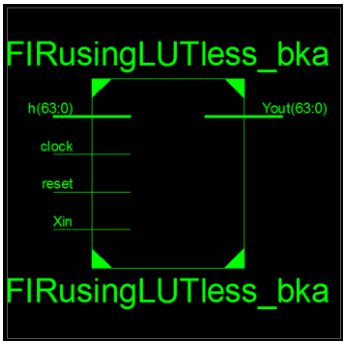

Figure 6.4 : RTL Schematic

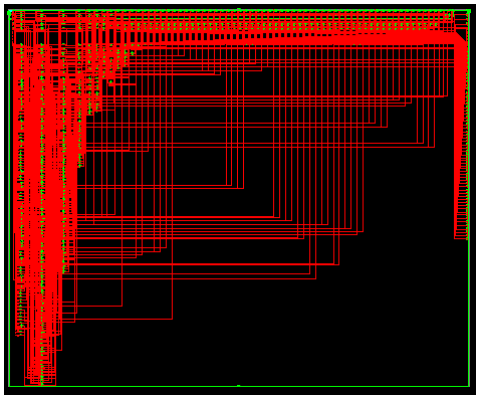

Figure 6.5: View Technology Schematic

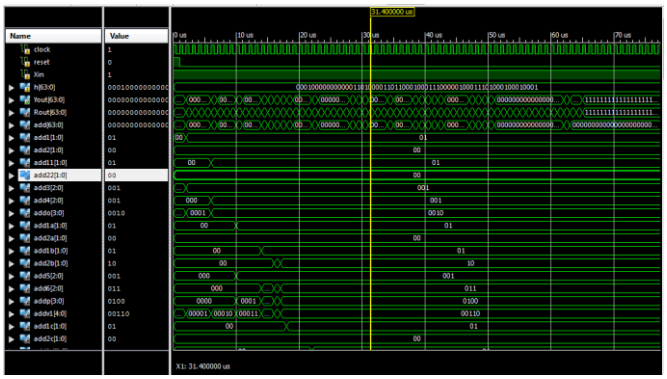

Figure 6.6 : simulated wave forms

Parameter	FIR with CSKA	FIR with BKA
No of LUTs	554	401
Power(m Watt)	4.521	3.272

Table 6.1 : parameter comparison table

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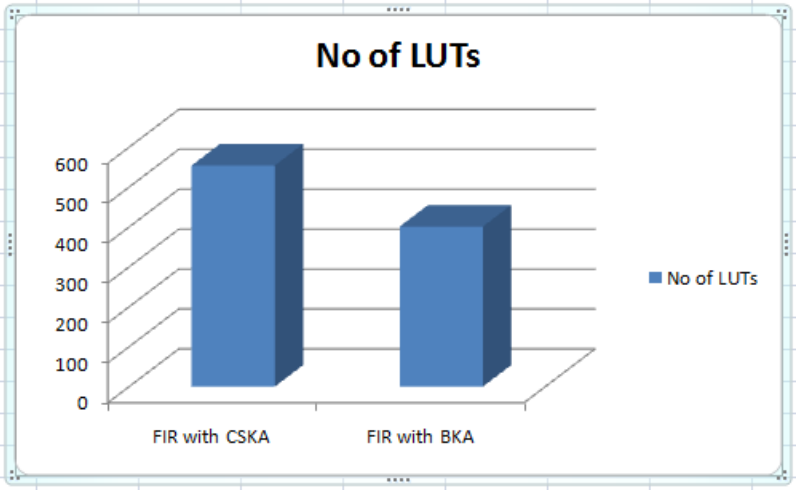

Figure 6.7 : LUT comparison bar graph

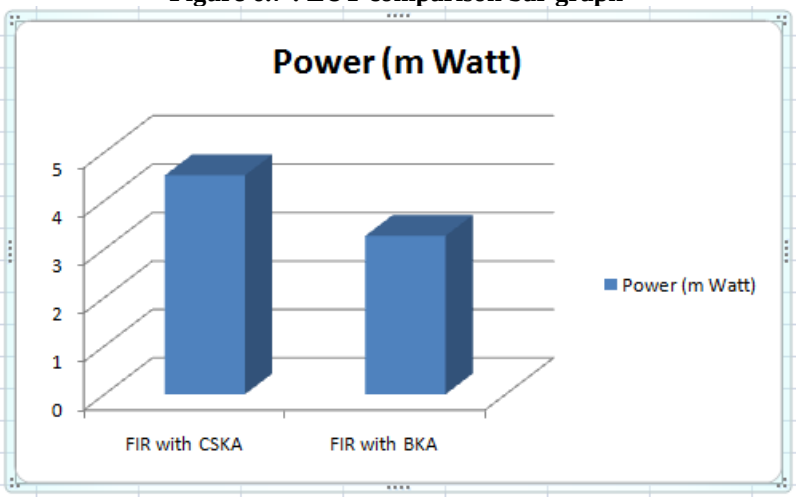

Figure 6.8 : power comparison bar graph

VII. CONCLUSION

In the last two decades, much architectures have been introduced for the design of low complexity fir operation. But there is no such improvement in the FIR design. This project gives the solution for that type of requirements. In traditional filter design methodologies consumes much power due to multiplier .To avoid this disadvantage this introduces distributive arithmetic method .From the table it can be concluded that the FIR with Brent kung adder structure occupies less area, and consumes less power compare with the FIR with carry skip adder structure, and the experimental results were verified in Xilinx 12.3 ISE Tool. So from this project it has a chance to use the corresponding structure based on the industrialrequirements. In future there may be a chance to develop the layouts for the structures.

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