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Analysis of High Speed Energy-Efficient Carry Skip Adder High-Speed Skips Logic at Different Levels

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ABSTRACT: A carry skip adder (CSKA) structure has the high speed and very low power consumption. The speed of the structure is achieved by concatenation of all the blocks. The incrimination blocks are used to improve the efficiency of the carry skip adder structure. In existing method multiplexer logic is used, the proposed structure uses the AND-OR-Invert (AOI) and OR-AND-Invert (OAI) for the skip logic. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture. The speed enhancement is achieved by combining concatenation and incrementation schemes to conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size (FSS) and variable stage size (VSS) styles, wherein the latte r further improves the speed and energy parameters of the adder. Finally

KEYWORDS: Carry skip adder (CSKA), energy efficient, high performance, hybrid variable latency Adders, voltage scaling

I. INTRODUCTION

There are many ways to improve the performance of digital circuits; one of the easiest way is to reduce the supply voltage. This depends on the fact that the switching energy has a quadratic dependence on supply voltage. Depending on the supply voltage reduction, when the device is in the ON state, it works in super threshold, near threshold or sub threshold regions. In these three regions of operation, the near threshold region provides fair tradeoffs between power consumption and delay. In additional to the knob of supply voltage, one can choose from a variety of adder families. One of the effective techniques to lower the power utilization of digital circuits is to reduce the supply voltage because of quadratic dependence of the switching energy on the voltage. Moreover, the sub threshold current, that is the main leakage element in OFF devices, has an exponential dependence on the supply voltage level through the drain-induced barrier lowering impact. Depending on the amount of the supply voltage reduction, the operation of ON devices may reside in the super threshold, near-threshold, or sub threshold regions. Working in the super threshold region provides us with lower delay and better switching and leakage powers compared with the near/sub threshold regions. In the sub threshold region, the gate delay and leakage power exhibit exponential dependences on the supply and threshold voltages. Moreover, these voltages are (potentially) subject to process and environmental variations in the nano-scale technologies. The variations increase uncertainties in the said performance parameters. Additionally, the small sub threshold current causes a large delay for the circuits operating in the sub threshold region. Adders are fundamental arithmetic components in many computer systems, since addition is the most common arithmetic operation in a wide variety of important applications [1, 2]. Consequently, several adder implementations, including ripple carry, Manchester carry chain, carry skip, carry look-ahead, carry select, conditional sum, and various parallel prefix adders are available to satisfy different area, delay, and power requirements. Descriptions of each of these adder architectures

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are given in [2]. Comparisons between different types of adders in terms of area, delay, and power dissipation are provided in [3-5].

Design of area and power efficient high speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the last position. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage because of quadratic dependence of the switching energy on the voltage. Moreover, the sub threshold current, that is the main leakage component in OFF devices, has an exponential dependence on the supply voltage level through the drain-induced barrier lowering impact. Depending on the amount of the supply voltage reduction, the operation of ON devices might reside in the super threshold, near-threshold, or sub threshold regions. Working in the super threshold region provides us with lower delay and higher switching and leakage powers compared with the near/sub threshold regions. In the sub threshold region, the gate delay and leakage power exhibit exponential dependences on the supply and threshold voltages. Moreover, these voltages are (potentially) subject to process and environmental variations in the nano-scale technologies. The variations increase uncertainties in the said performance parameters. Additionally, the small sub threshold current causes a large delay for the circuits operating in the sub threshold region.

II. THEORY

A. *MULTIPLEXERS*

A Multiplexer is a device that allows one of several analog or digital input signals which are to be selected and transmits the input that is selected into a single medium. Multiplexer is also known as Data Selector. A multiplexer of 2n inputs has n select lines that will be used to select input line to send to the output. Multiplexer is abbreviated as Mux. MUX sends digital or analog signals at higher speed on a single line in one shared device. It recovers the separate signals at the receiving end. The Multiplexer boosts or amplifies the information that later transferred over network within a particular bandwidth and time. This article gives an overview of what is multiplexer and types of multiplexer.

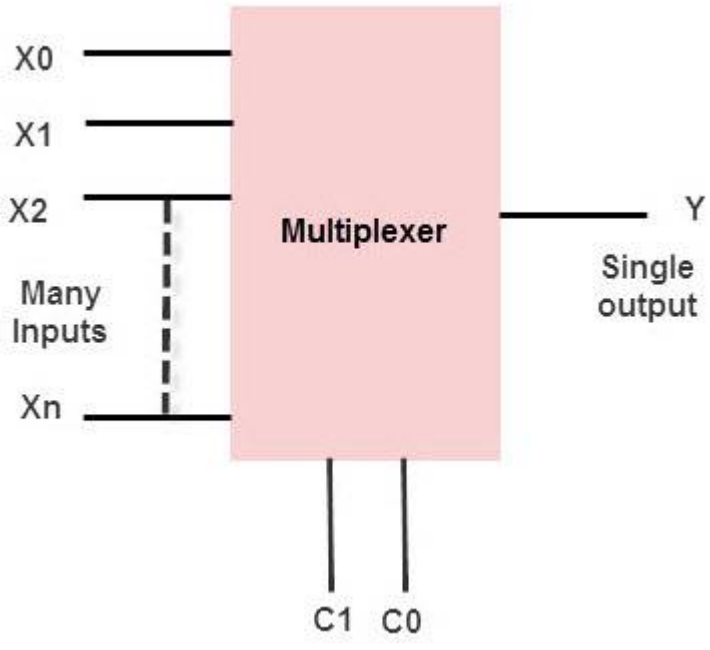

Fig. 1 Multiplexer

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The Multiplexer acts as a multiple-input and single-output switch. Multiple signals share one device or transmission conductor such as a copper wire or fibre optic cable. In telecommunications, the analog or digital signals transmitted on several communication channels by a multiplex method. These signals are single-output higher-speed signals. A 4-to-1 multiplexer contains four input signals and 2-to-1 multiplexer has two input signals and one output signal.

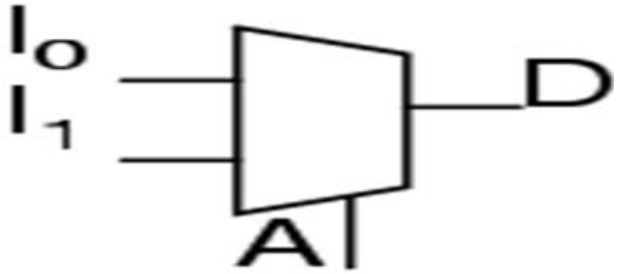

Fig 2 Schematic Symbol for Multiplexer

Table 1:- Truth Table for 2 to 1 Multiplexer

I_1	I_0	A	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

B. CONVENTIONAL CARRY SKIP ADDER

The structure of an *N*-bit Conv-CSKA, which is based on blocks of the RCA (RCA blocks), is shown in Fig. 1. In addition to the chain of FAs in each stage, there is carry skip logic. For an RCA that contains *N* cascaded FAs, the worst propagation delay of the summation of two *N*-bit numbers, *A* and *B*, belongs to the case where all the FAs are in the propagation mode. It means that the worst case delay belongs to the case where

$$P_i = A_i \oplus B_i = 1 \text{ for } i = 1, \ldots, N$$

Where *Pi* is the propagation signal related to *Ai* and *Bi*. This shows that the delay of the RCA is linearly related to *N* [1]. In the case, where a group of cascaded FAs are in the propagate mode, the carry output of the chain is equal to the carry input. In the CSKA, the carry skip logic detects this situation, and makes the carry ready for the next stage without waiting for the operation of the FA chain to be completed. The skip operation is performed using the gates and the multiplexer shown in the figure. Based on this explanation, the *N* FAs of the CSKA are grouped in *Q* stages. Each stage contains an RCA block with *Mj* FAs (j= 1. . . *Q*) and skip logic. In each stage, the inputs of the multiplexer (skip logic) are the carry input of the stage and the carry output of its RCA block (FA chain). In addition, the product of the propagation signals (*P*) of the stage is used as the selector signal of the multiplexer.

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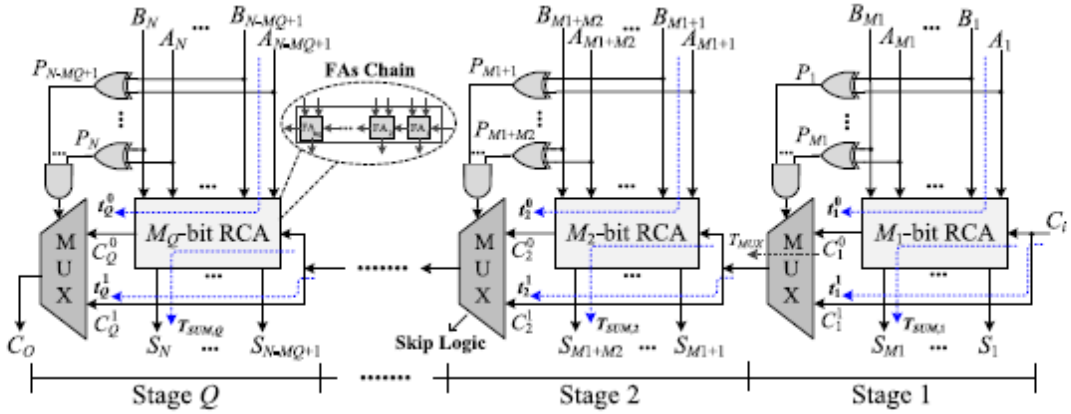

Fig 3. Conventional structure of the CSKA

III. METHOD

A. CARRY LOOK AHEAD ADDER (CLA)

The carry look ahead adder (CLA) solves the carry delay disadvantage by calculative the carry signals before, based on the input signals. It's based on the particular fact that a carry signal are generated in two cases:

(1) Once each bits a_i and b_i are one, or

(2) Once one of the two bits is one and so the carry-in is one.

Thus, one will write.

$$c_{i+1} = a_i.b_i + (a_i \oplus b_i).c_i$$
$$s_i = (a_i \oplus b_i) \oplus c_i$$

The above two equations can be written in terms of two new signals p_i and g_i , which are shown in Figure 4:

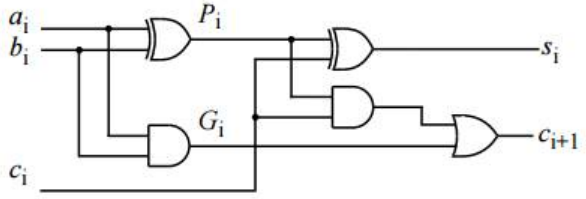

Fig 4: Full adder at stage i with p_i and g_i shown

A carry-look ahead adder (CLA) or fast adder could be a variety of adder utilized in digital logic. A carry-look ahead adder improves speed by reducing the quantity of time needed to determine carry bits. It will be contrasted with the easier, however usually slower, ripple carry adder that the carry bit is calculated alongside the total bit, and every bit should wait till the previous carry has been calculated to start calculative its own result and carry bits (see adder for detail on ripple carry adders). The carry-look ahead adder calculates one or additional carry bits before the total that reduces the wait time to calculate the results of the larger value bits.

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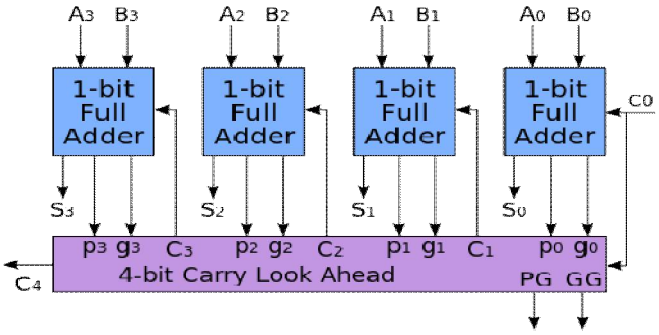

Fig. 5 Carry Look Ahead

This structure is formed by combining concatenation and the incrimination schemes with the Conv-CSKA structure, which is shown in fig.3 and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates (Fig. 6). The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented. Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).

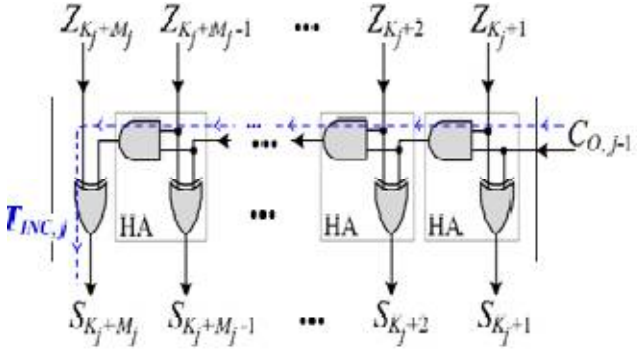

Fig 6: CI-CSKA Structure

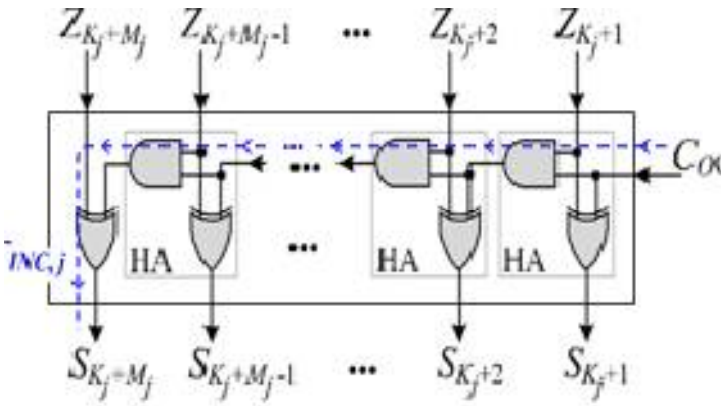

Fig.7:Incrementation block structure.

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IV. RESULT

The result analyses of the CSKA and simulation results of the projected system are shown in following figure. The design planned in this paper has been developed victimization MODEL machine. ADDERS are a main building block in ALUs (arithmetic and logic units).Low power arithmetic circuits turn into very necessary in VLSI industry. Adder circuit is that the main building block in DSP processor.

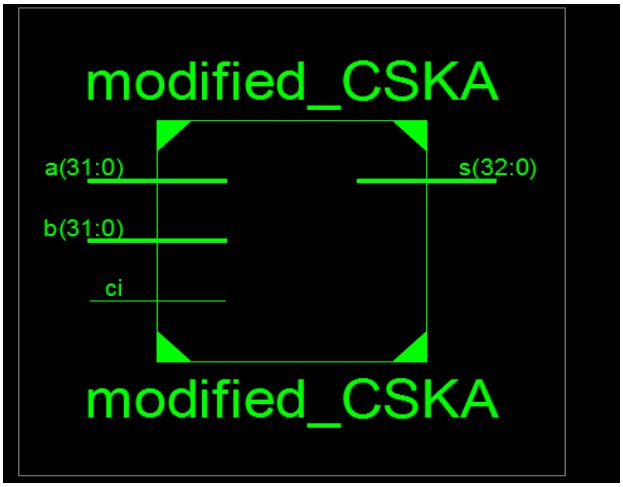

Fig. 8 Block diagram of modified CSKA

Block diagram representation of the Hybrid or proposed model of the CSKA system shown in Figure 8 in which we see three input and two output which is represented in as a sum and carry of the model which is represented as a S and C_o.

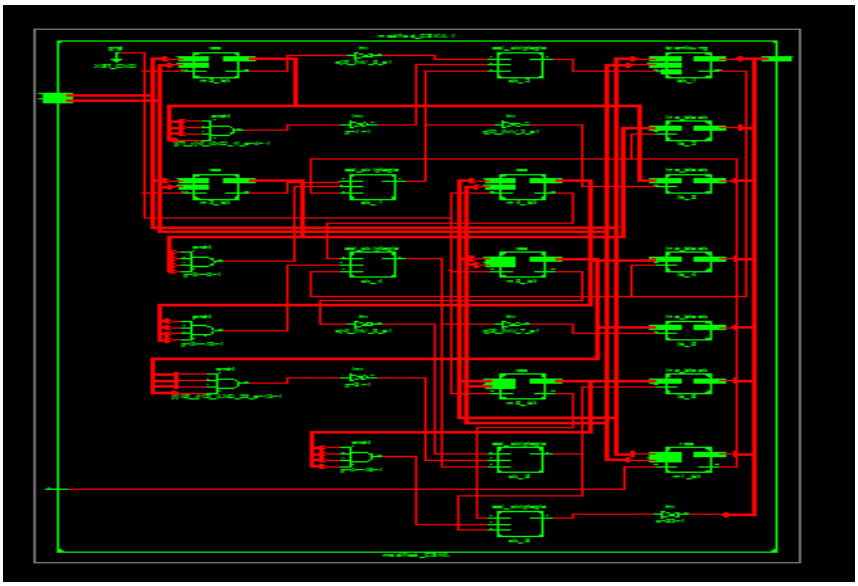

Fig.9 RTL schematic

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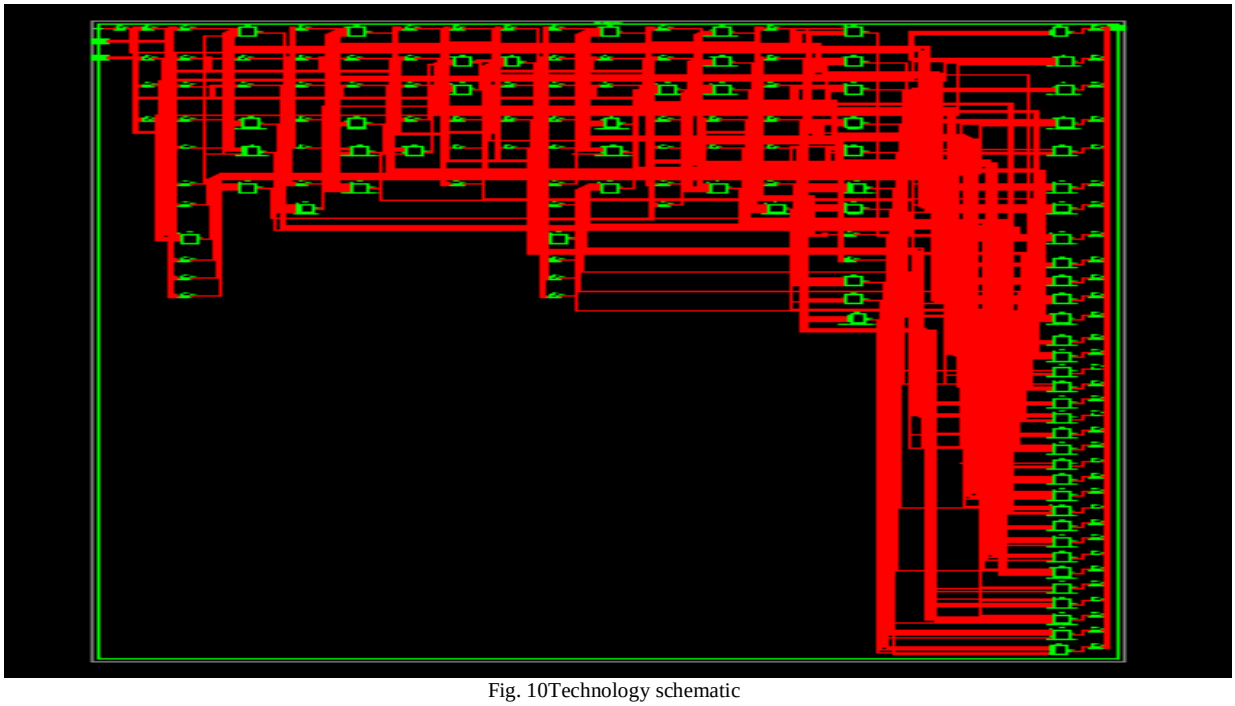

Fig. 10Technology schematic

In the above figure we can see the schematic representation of the applied technique in the CSKA technique. Which represents an applied AND, XOR logic gates.

Fig. 11 Simulation results

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Figure 11 represents the simulation results come after the applied schematic digram as all Parameters applied on it. Simulation result is comes out by the use of Xilinx software.

V. CONCLUSION

In this paper, a static CMOS CSKA structure known as CI-CSKA was proposed, that exhibits a higher speed and lower energy consumption compared with those of the conventional one. In addition, AOI and OAI compound gates were exploited for the carry skip logics. The efficiency of the proposed structure for both FSS and VSS was studied by comparing its power and delay with those of the Conv-CSKA, RCA, CIA, SQRT-CSLA, and KSA structures. The results revealed considerably lower PDP for the VSS implementation of the CI-CSKA structure over a wide range of voltage from super-threshold to near threshold. The results also suggested the CI-CSKA structure as a very good adder for the applications where both the speed and energy consumption are critical. In addition, a hybrid variable latency extension of the structure was proposed.

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