ISSN(Online): 2320-9801
ISSN (Print) : 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 3, March 2016

Efficient Fault Detection and Dyad Routing Algorithm for 3D Network on Chip

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ABSTRACT: NOC is the ability to detect fault and failures in the architecture. It is scalable and flexible communication architecture. In this paper, we propose detection of data packet and routing algorithm errors. Both presented mechanism is used to determine permanent and transient errors and localize accurately the position of faulty blocks in the routers, to preserving throughput and data packet latency. The proposed method is based on new error detection mechanism suitable for dynamic NOCs, where the number and position of processor elements vary during runtime. This paper gives the traffic load variations on average latency and power for DYAD routing algorithm, this algorithm having both deterministic and adaptive routing algorithm. This algorithm is used to determine the path of a packet from source to the destination. The best performances of routing algorithm in the NOC architectures are minimum latency, minimum power and maximum throughput. The aim is to reduce the transmission delay and to ensure the priority to the shortest path routing of data. The simulation result explains the effectiveness of DYAD routing algorithm under different traffic patterns.

KEYWORDS: Network on chip, fault detection, Adaptive routing, Deterministic routing, Improved DYAD.

I. INTRODUCTION

NOC architecture is based on packet switched network. The performance and the efficiency of the NOC heavily depends on communication

infrastructure. The design of efficient, high performance routers represents a critical problem for the success of the NOC approach. On chip transistor density has increased the integration of dozens of intellectual property on a single die to form system on chip.The communication in these system, shared buses should be replaced by interconnection networks. It provides a ready architecture for scalable on-chipcommunication. The NOCs proposed a new paradigm for realizing complex SOCs.In on-chip communication the NOC scale have better performance and efficiently to detect fault tolerant characteristics. To determine the path of packet from source to destination by using routing algorithm.The routers in the network is classified into deterministic and adaptive. Deterministic routing is also called oblivious routing; the path is completely determined by the source and the destination. A routing technique is called as adaptive routing, if the source and destination addresses are given the path taken by a particular packet and its depends on dynamic network conditions. In Dynamic Adaptive and Deterministic (DyAD) routing algorithm has both the characteristics of XY and OE routing model. The development of XY routing algorithm is simple but is not able to balance the load across the link in non-uniform condition. If the link or router failure means the OE routing algorithm provide tolerance and to improve the network performance. The network traffic in the NOC is divided into two categories; Guaranteed Throughput (GT) and Best Effort (BT) traffics.GT acts like a circuit switched network and works with routing algorithm. In BE traffic there is no guarantees that BE packets will ever reach the receiver. The worst case packet can be lost in the BE traffics. In this paper, we present a routing scheme which combines the advantage of both deterministic and adaptive routing algorithm and is based on the current network congestion. This packet injection rate increases, deterministic routers suffer from throughput degradation, so they cannot respond to network congestion. In adaptive routers have some of the alternative paths, so they avoid network congestion and to get higher throughput. A router for the mesh topology has four inputs and four outputs from(or) to other routers.InDyADrouting, each router continuously monitors its local network load and make decision based on this

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information. If the DyAD routers work in the deterministic mode means the network is not congested. In contrast, when the network is congested, the DyAD router back to the adaptive routing mode.To propose a valid approach and show how to avoid deadlock and livelock in the network. In this paper we have to choose minimal odd-even routing as the adaptive routing for on chip routers.The minimal routing is used to reducing the energy consumption of communication, but also to keep the network free from livelock. Routing algorithm can be fault tolerant algorithm like backtracking. Most of the algorithm sends packets only in the direction. To overcome this problem by using DyAD routing algorithm.

II.RELATED WORK

NOC design methodology and 3D Integration are expected to overcome many of the challenges. The logical step is to reduce the cost of each required building block. The characterization of vertical interconnects for use in 3D NOCs with respect to physical implementation and Timing requirements. The 3D topologies for 3D NOC considering power an latency cost. A routing technique involves two processes. The first involves the mechanisms that compute feasible path between originator-destination pairs. The feasible path is satisfies the correctness criteria and algorithm of the objective function. A correct path is free of any permanent loops; it represents a true simple path that packets can be forwarded unambiguously from originator to destination. The objective of this paper includes shortest path, minimum delay or maximum residual capacity. The shortest path routing algorithm attempt to minimize the delay to each OD pair and set the correct paths, minimum delay algorithm is used to balance traffic flows in order to achieve global minimum average delay. The second mechanism of routing involves the forwarding of packets along a feasible path. The shortest path routing provides only a single path. When forwarding packets, this process involves determining which interface to use. Here using two possible approaches. Source routing each packet includes a path specification which list subset of the nodes.In this technique each node can either directly extract the identity of which adjacent node to forward the packet. The second approach is hop by hop routing; this algorithm provides multiple routes in the routing table and to select the route additional information or policy to be required. The main focus will be on the aspect of routing that involves the computation of shortest path in the network. The basic objective of this algorithm is to compute the different path and to forward the data packets between OD pairs.

III. DYADROUTING ALGORITHM

Dynamic Adaptive and Deterministic network on chip uses dynamically both deterministic and adaptive routing algorithms to route packets.Fig.1 shows the architecture of DyAD router. Here four types of different mode present in the DyAD router.Each input controller in fig has a separate FIFO is used to buffers the input packets before delivers to the destination.

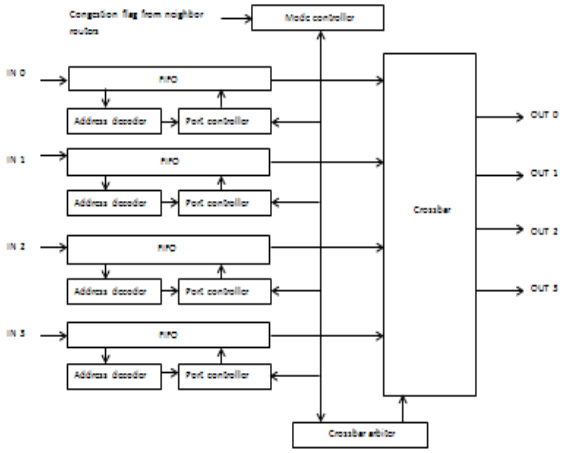

Fig.1 Router architecture

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When a new header flit is received the address decoder processes that flit and then send to the port controller, this determines which one of the packet should be delivered to the destination and the port controller is used to select the direction in which the downstream router has more empty slots in FIFO. The input port controller also monitors the FIFO occupation ratio and the ratio reaches the congestion threshold level, it determines the value of 1 indicates the corresponding congestion flag wire and the value 0 indicates the upstream router. The crossbar arbiter maintains the current crossbar connection and determines which one is grant connection permission to the port controller.There is multi number of input port controller requests in the same available output port; the crossbar arbiter uses the first-come-first-served policy to select which input port to grant the access. The mode controller used to monitors the neighboringcongestion and to determine if the node in deterministic or adaptive. In the neighboring routers any congestion flags are occurs, then the mode controller commands input port controllers to work in adaptive mode, otherwise the switches of the port controller works in deterministic mode. The advantage of DyAD routing algorithm is low latency in congestion free network but still good throughput in congestion network.

3.1 DYAD –XY ROUTING

In this paper, the XY routing is used to representative deterministic routing scheme because its simplicity and popularity.XY routing is a minimal path routing algorithm and to avoid deadlock and livelock in the network. The deterministic routing, the source and destination address are given and the routing path is fixed once. But in the adaptive routing mode multiple routing path exist because adaptive routing offers packets more flexibility in choosing their routing paths. To solve the problem, this may be caused by packets waiting for each other in a cycle. In this routing the packets can be routed in both X and Y directions and this routing algorithm needs a mechanism to guarantee deadlock avoidance. The network has virtual channels, virtual channel in Y dimensions having two sub-networks. Half of the channels in the Y dimensions are +X sub-network and –X sub-network. The packet will be routed through +X sub-network means the destination mode is to the right of the source. If the packet will be routed through –X sub-network means then the destination node is to the left source.

3.2 DYAD-OE ROUTING

In Odd-Even mode the packet can be routed to both output p1 and p2 and it always be routed to p1 in OE-fixed. InFig (2) clearly shows the tradeoff between deterministic (XY) and adaptive(OE) routing. Compared to XY routing the OE routing to achieve much higher saturation throughput. If XY beats the OE routing then the network works in low packet latency. Dyad-OE is able to achieve a throughput of 0.027 packet/cycle. The same traffic pattern and injection rate, DyAD achieves shorter average packet latency.

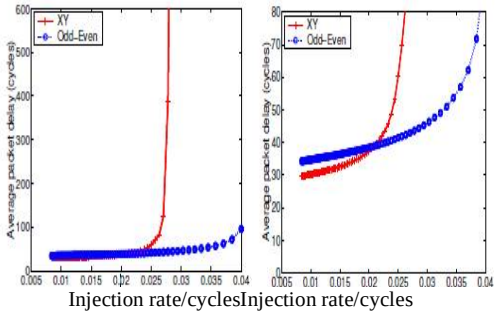

Fig.2 Performance comparison between XY and OE routing

IV. PROPOSED METHOD

Here four types of module used in the proposed architecture. In Fig 3 Error correction code is used to correct the error packets and send the packet to the destination. It's follows,

Design of data transmission module: The data transmission module is the basic module in the smart reliable network on chip.The input data or information is divided into packets and that can be transmitted through the reliable network to the destination address.

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Design and analysis of nodes: The node in the network is designed for establishing the link between the source and destination. The nodes in the network having different node value, to calculate all possible node value before transmit the data to the destination with respect to the node value and choose the reliable path for networking.
Design and analysis of network: The network is designed by make the link between active nodes in the design. To make the reliable operation we use deterministic and adaptive routing algorithm. In this method to detect the faulty nodes in the network and make sure the reliability.
Design the error correction module: This module is designed for detection and correction of errors or faulty node in the reliable network. Here we have to use the effective error correction unit is to make sure that the received data or information at the destination point as error free.

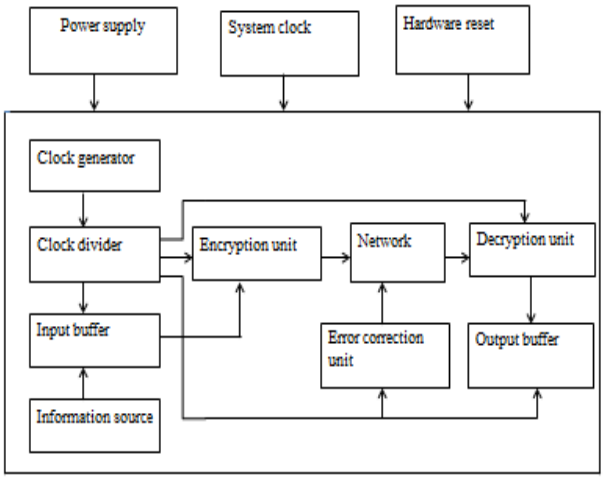

Fig. 3 Proposed architecture

4.1 FAULT TOLERANT AND ERROR DETECTION

In our fault model errors are mainly due to fault concerning the nodes FIFO.These NI components are composed by memory cells and they are affected by both permanent and temporary faults.For implementing these basic components are based on the use of error correcting and detecting codes.Routing path errors registers of the LUT, reducing the probability of the wrong routing path register associated with an input destination address.

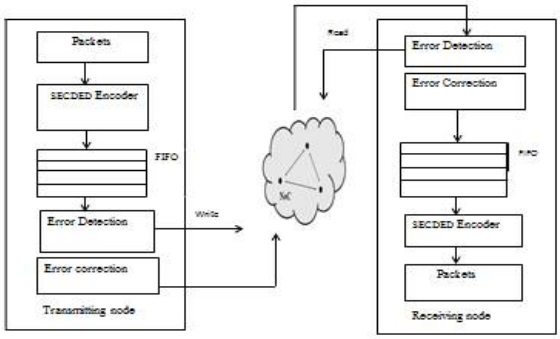

Fig. 4 Integration of the proposed FIFO architecture with an NOC link implementing error correction and detection

The fig(4) shows the integration of the proposed FIFO architecture in an NOC implementing error detection and correcting in the links connecting NOC components.The information is encoded before inserted into the FIFO and checked for errors detected means, the coded information (or) packet is directly sent to the node, in this way the

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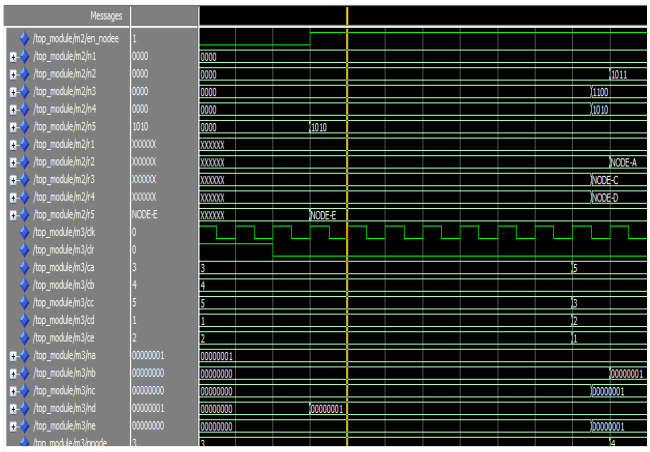
encoding step performed in the case of single error occurs, the coded information is corrected and directly transmitted. At the receiving nodes, flits are checked for errors, corrected and then encoded in the receiving FIFO.The proposed architecture protects the packets from the corruption of the information stored into the FIFO.Functional runtime errors, corrupt data errors, routing path errors and control flow errors and fault in the FIFO slots storing respectively, header flits and control flow information are avoided (or) reduced.To detect and correct the permanent, transient errors by using SECDED Hsiao code. By using this mechanism we are able to provide a graceful degradation of the performance during its operation.The procedure applied when detecting errors in the network. If no permanent faults have been detect in the nodes means the register is properly working. Suppose it is considered partially working when one permanent fault to be detected in it. The register is used for providing corrected routing information to the packet. Where error is detected in the network and no working spare register are available then the whole network to have failed, since the NI is used to provide correct routing information for the packet directed to the NOC node. The detection of double error in a partially working register needs recalculation of the routing path associated with it. The recalculation of the routing path is performed by running algorithm implemented into the NOC for detecting a path to the destination. After the recalculation the information sends to the node and checked again for errors.

IV. EXPERIMENTAL RESULT

The result of this paper presents both minimum latency and to correcting the fault in the NOC design. The packets to be encrypted and then sent to FIFO. In FIFO some of errors to be occurred, to correcting the fault and the data sent to the destination. If the information are not affected means the destination receiving the data without fault occurrence. To implementing the DyAD algorithm and fault detection method in NOC design ,we have to get minimum latency of 0.7382 and maximum throughput. The fig(3) shows the result of encrypted the input data by using SECDED encoding.



V. CONCULUSION

This paper gives the study on the implementation of fault tolerant network interfaces for NOCs. We showed that the occurrence of permanent and transient errors in the network could cause unwanted behavior of that create unrecoverable situations in the NOC, such that live lock and deadlock conditions. So we proposed new architectural solutions based on the use of error correcting and detecting codes and to create a shortest path routing for minimum latency by using DyAD routing algorithm.

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